VLSI TECHNOLOGY, INC.

COMPUTER PRODUCTS DATA MANUAL

MARCH 1989

Logic Products Division

PREFACE

This manual provides the reader with an in-depth technical reference on the VLSI Technology, Inc. families of computer product chip sets and devices. In the body of the text all devices are treated as individuals so that the electrical characteristics of each can be clearly defined. A "Selector Guide" in the front of this manual defines which devices should be selected to form a chip set that meets his or her system performance specifications. If the system designer requires performance or functions not included in this manual, he or she should contact their local VLSI Technology Design Center or Sales office. Most of the devices in this manual were designed with VLSI's tools, and are available for ASIC designs if the designer wishes to design derivative product.

In addition to a detailed hardware description of each device, this manual also contains PC/AT-compatible system schematics to demonstrate a typical system implementation. Since computer technology is extremely fast-moving, it is planned that VLSI's Logic Products Division will revise, update, and publish this manual often. This will allow rapid publication of data on new products, as well as improvements on existing ones. The most current information may also be obtained from your local VLSI Technology, Inc. Sales Office, Representative, or the Logic Products Division in Tempe, Arizona.

Readers are encouraged to send their comments, corrections, or suggestions to:

Manager, Technical Communications
VLSI Technology, Inc.
8375 South River Parkway
Tempe, AZ 85284

CONTENTS

CONTENTS

CONTENTS

CONTENTS

VLSI TECHNOLOGY, INC.

CONTENTS


VLSI TECHNOLOGY, INC.

VLSI TECHNOLOGY, INC.

SECTION 1

INTRODUCTION

Logic Products Division

COMPUTER PRODUCTS DATA MANUAL

GENERAL

The primary business objective of VLSI Technology, Inc., (VLSI) is to provide systems designers with total application-specific integrated circuit (ASIC) solutions. To accomplish this, it has created a unique blend of expert design tools, leading-edge process technologies, state-of-the-art fabrication facilities, and a wide range of products, including a variety of "catalog" devices.

The Logic Products Division of VLSI Technology is responsible for the manufacture and marketing of a diverse logic-based product line that encompasses both innovative and proven, well established catalog devices. This line includes microprocessors and coprocessors, peripheral circuits, and products for data communications and telecommunications applications.

Unlike other suppliers of such devices, however, VLSI is also a recognized leader in ASICs. As such, it not only possesses the design, process, and fabrication capabilities necessary to produce the highest-quality off-the-shelf components, but is also able to treat its logic products as an integral part of a complete solution. The primary vehicles for accomplishing this are the megacell and cores; many of the functions represented by individual devices are implemented as megacells in VLSI's software libraries and used for semicustom circuit design and functions developed as megacells for specific applications can be turned into catalog products. Most other functions are available as high integration cores which can be utilized by VLSI to create variations of these standard products for specific customer requirements.

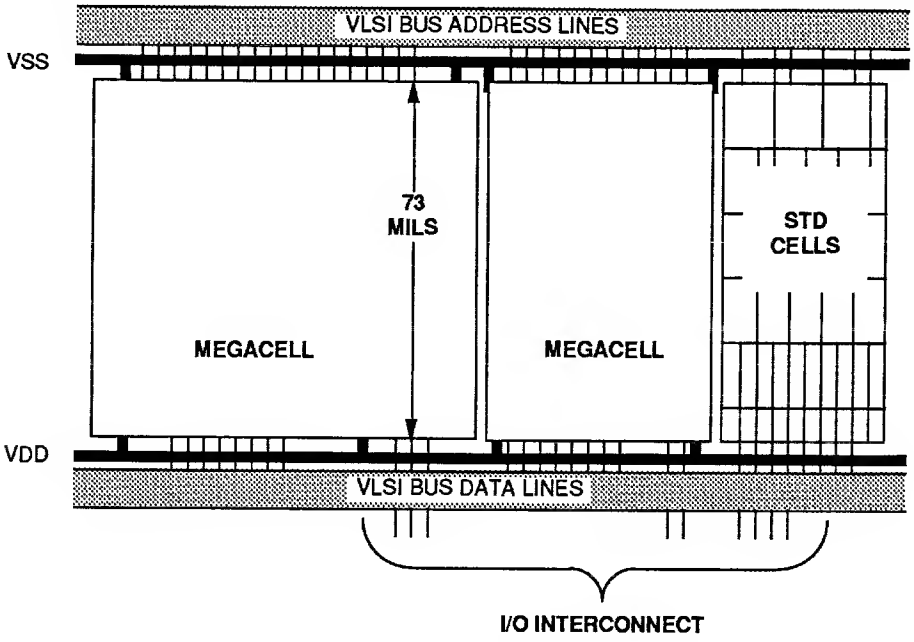
MEGACELLS

The megacell is a relatively new concept in the world of IC and system design. As such ASIC companies as VLSI offer better tools for IC design, simulation, and testing, it becomes necessary for systems manufacturers to design custom ICs to keep up with their competition. Megacells help decrease design time by providing large building blocks that are equivalents of standard off-the-shelf products. By using megacells and VLSI's design tools, manufacturers can have a custom IC design capability without all of the normal custom development costs.

The VLSI Technology family of megacells represents commonly used peripherals that are good candidates for integration as parts of customer-driven designs, which can be either customer-specific or market-specific. In customer-specific designs, it is possible, for example, to combine these integration elements with other megacells and logic to become single-chip equivalents of computer systems that are aireaoy in production. This increased level of integration provides cost and space reduction that can keep the system designs competitive. In a market-specific design, upward-compatible enhancements that meet the needs of many customers can be added and the device offered as a new standard product.

VLSI's megacells are designed to have a fixed height and variable widths, offering the best trade-off between unusable internal space and placement ease. As shown in Figure 1, they can be configured to make a very dense final design with a minimum of wasted silicon real estate.

FIGURE 1. VLSI TECHNOLOGY MEGACELLS ARE OF A FIXED HEIGHT, WITH VARIABLE WIDTHS.



Of equal importance with the physical layout format of the cells is the structure of the interconnect bus. This bus must be generic enough to allow a wide variety of functions to be connected uniformly and efficiently, and must be fast enough to not itself become a limiting factor as system performance increases.

The internal structure of the bus created by VLSI for use with its megacells contains an m-bit data bus and an n-bit address bus, both of which are expandable in width to accommodate changes in system requirements. The bus operates synchronously at a rate of 3 million transfers a second, which is equivalent to the performance of a 10 MHz 8086 or 12 MHz 68000 microprocessor. The bus definition allows for internal access times of 50 ns and cycle times in the 200 ns range. With standard pad drivers, external loads can be driven while supporting a 3 MHz bus frequency; faster speeds can be obtained by using faster pad drivers. To create a standard product from a megacell, an interface circuit is incorporated that exactly matches the slower timing of the external bus to the internal bus.

MEGACELL-BASED DESIGN RATIONALE

There are many reasons why megacells make sense for new designs, including reduced board space, lower power, increased reliability and reduced design times.

Typical applications that can benefit from the use of megacells are those that contain three or four LSI components and a handful of "glue" components. All of these components can be combined into a single component if the functions can be partitioned into logical groups with a reasonable number of I/O pins. In this type of application, the total pin count might be reduced from 300 pins for a discrete solution to less than 100 pins, and the circuit board area reduced from approximately 20 square inches to 2 square inches.

The power consumption of megacell designs can be very small in comparison with the HMOS designs they replace, since all of the VLSI Technology megacell family is implemented in high speed, low power, two-micron and 1.5-micron CMOS technology. In addition, because several functions can be put on one piece of silicon, the interconnect capacitance and inductances are minimized, thereby reducing the power to a fraction of what was needed in previous designs.

The reliability of a megacell-based design is typically better than the collection of discrete components it replaces because there are fewer pins, fewer bonding wires and lower total power consumption. In most systems, the largest contributor to reliability problems is IC pin connections. with such other factors as die temperature and die size being secondary. The more functional blocks that can be combined on a single piece of silicon, the fewer the number of interconnections that have to be bonded to package pins, resulting in higher overall reliability of the component and system using it.

Since megacells can be used as high level building blocks, overall design times can be reduced significantly by taking existing designs using standard products and integrating additional support logic directly onto the chip. An example of this technique would be the integration of a VL68C45 CRT controller with a memory interface and video shift registers to form a single-chip video adapter. An additional option might be to include character ROMs or RAM arrays, although the addition of these commodity components is not always cost effective.

CURRENT FAMILY OF MEGACELLS

Megacells are designed by very carefully studying the data sheets and systems implementations of the original part vendors, but an important part of validating a megacell design is to subject it to many different hardware and software environments. Only after a part has been tested in several applications can a vendor feel confident that the megacell exactly emulates the original function, including all of the undocumented "features". The VLSI Technology philosophy is to offer members of the megacell family as standard products as well as cells so that this validation can take place very quickly after the introduction of the standard product. Since customer-specific design times typically take from two to four months, megacell designs can be started before the standard product validation has been done. This lead time allows customers to get a head start introducing designs.

DESIGNING A CIRCUIT USING MEGACELLS

The design process is started by using a megacell schematic "icon" as part of the schematic entry of the user"s design. Provided with the megacell icon is a data sheet detailing the internal timing requirements of the megacell. The designer works from this data sheet as if using an off-the-shelf standard product, except that the logic and timing of the bus are somewhat easier to use.

ADDITIONAL LOGIC FOR TEST SIMPLIFICATION

In all cases, some additional logic will be necessary to facilitate testing the megacells. This additional logic consists of multiplexers on pins to allow all of the connections of the megacell to be accessed from the periphery of the circuit. This dictates that all designs be contained in packages having at least as many pins as the most pin-intensive megacell used internally. To enable the test mode, an illegal condition on the interface is often used, such as Read Strobe and Write Strobe being asserted together while the chip is selected. This would normally never occur in an application, so it is a safe combination to use. When enabled, the I/O pads of a specific megacell are connected to the I/O pins of the component, and the standard product test program run to verify the functionality of the core.

TEST PROGRAM DEVELOPMENT

Test vectors are provided for all megacells with high fault coverage. These test programs can be integrated with the rest of the chip's test program using VLSIvector. VLSI provides these "canned" test programs with each megacell so that it will not be necessary to spend time trying to develop a test for megacells used in the design. These test programs ensure that he megacells have been fabricated correctly and are functioning within their specifications. They are developed with a focus on very high fault coverage.

In fact, there is no need to simulate these test programs, except for a final verification that the test isolation circuitry has been properly connected. Instead designers can devote additional design verification time to the non-megacell portions of the circuit and the interfaces between the megacell and the rest of the circuit.

COMPLETING THE DESIGN

When simulation is compiete and the design works satisfactorily, the layout process can begin. In most cases, designers are interested in minimizing design time and associated costs, so they pick standard cells for the additional blocks of logic that will surround the megacell cores. Cells are individually compiled, placed and routed to create blocks of logic until the entire non-megacell portion of the design is complete. For the best layout efficiency, the additional logic is either put into a block having the same height as a megacell, or it is put around the megacells to fill in the voids. When each portion of the design is completed, these blocks can be placed and interconnected using a tool called Chip Compiler, which is an automated arbitrary block place and route system. This editor assists in interconnecting blocks of cells and optimizing both the placement and interconnection of cells. The overall goal of placing blocks to form the chip is to get the ratio of the X and Y dimensions (the aspect ratio) as close to 1:1 as possible. The resulting square die gives the packaging engineer the most flexibility in package selection.

When the entire layout process is complete, a netlist of interconnections is extracted from the physical data base to allow comparison of what was intended to be with what actually was implemented. Once the extraction is complete and the netlist comparison between schematic and layout is successful, the device can be resimulated in software with more accuracy, since values of expected capacitance are extracted along with the connectivity information. Finally, the layout is checked for design rule violations using the design rule checker (DRC) program. When all of this has been successfully completed, the data base is sent to a design center, where the actual physical layout of the megacells is included in the data base. When everything checks out properly, a mask set is created and silicon is started. From this point, the fabrication time typically takes eight weeks for the first pass prototypes.

SUMMARY

Megacells offer a way to quickly design chips that replace today's board level function, while at the same time offering competitive costs, increased reliability, increased performance and reduced board space. The design process requires a wide range of design tools, including standard cells, cell compilers, simulators, routers, test program generators, and libraries of designs. VLSI Technology, Inc. specializes in offering these kinds of tools in addition to complete wafer services to provide a total solution to systems designers.

VLSI TECHNOLOGY, INC.

SECTION 2

ORDERING AND PACKAGING INFORMATION

Logic Products Division

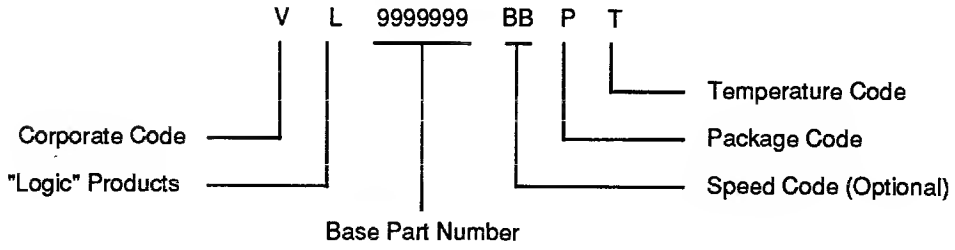

VLSI TECHNOLOGY, INC.

ORDERING AND PACKAGING INFORMATION

GENERAL

VLSI Technology, Inc., Logic Products devices are available in a variety of plastic packages - including flatpacks, chip carriers, and pin grid arrays - and in different temperature ranges. Specific information on the packages and temperature ranges for particular devices is coded into the part number portion of the order information included in each data sheet.

The information is organized as follows:



Package Codes:
- C - Sidebrazed Ceramic
- F - Plastic Flatpack
- G - Pin Grid Array
- L - Leadless Ceramic Chip Carrier
- P - Plastic Dual In-Line
- Q - Plastic Leaded Chip Carrier

Temperature Codes:

A - Automotive	(–40°C to +85°C)
C - Commercial	(0°C to +70°C)
I - Industrial	(refer to spec.)
M - Military	(–55°C to +125°C)

ORDERING AND PACKAGING INFORMATION

PACKAGE CONSIDERATIONS

DUAL IN-LINE PACKAGES

The dual in-line package (DIP) has been in high-volume production for nearly twenty years, and is estimated to have been the package of choice for over 80% of all integrated circuits shipped in 1985. Some 1986 usage estimates are as high as 18 billion units worldwide. Generally, devices in DIPs can be purchased in two types of ceramic (cerdip and side-brazed) and in the very-familiar molded plastic package. Over 85% of all DIPs, or over 12 billion, sold worldwide in 1985 were plastic.

The ceramic side-brazed package is relatively expensive and is frequently imported. It has excellent mechanical characteristics, including the ability to survive extreme temperatures, salt water, and corrosive atmospheres. However, as the cost of the integrated circuit it houses becomes less and less expensive, the relative cost of the ceramic DIP becomes a major concern. In a large number of applications, this package is several times more expensive than the chip within it. As would be expected, this package is very popular in military electronics and in other potentially harsh mechanical environments. The side-brazed package, while representing less than 2% of all DIP packages shipped in 1985, represents a higher percentage of DIP revenue, due to its comparatively high average selling price (ASP).

The cerdip is a "sandwich" of two ceramic parts that are joined together by a cement-like epoxy. The die itself is mounted on a lead frame, and enjoys many of the cost economies associated with this approach. The cerdip has some of the mechanical advantages of the side-brazed ceramic at a lower cost. The cerdip represented about 14% of all DIP shipments in 1985.

The plastic DIP has been the catalyst for the computer revolution. The dramatic reduction in the cost of microprocessors, microprocessor peripherals, communications devices, and memories has been passed along to the manufacturers and the final users because plastic packaging has remained extremely inexpensive. In addition, reliable automated 16-pin and 14-pin DIP insertion equipment has dramatically reduced manual "board stuffing" costs of DIPs. The plastic DIP itself is easy to manufacture. The die is mounted on a copper-alloy lead frame and the plastic material is molded around it. It is usually branded by a printing method with an epoxy-based ink but, recently, laser-scribing the number into the plastic body is gaining popularity, reducing costs even further.

Mechanically, the DIP has proven to be an extremely utilitarian package in most applications. Its short, stiff leads on 2.54 mm (0.1 inch, or 100 mil) centers allow reasonably easy insertion for both test and production by both manual and automatic techniques. While more expensive DIPs are placed in sockets, the overwhelming majority are soldered directly into the printed circuit board. The 64-pin DIP, the largest DIP in high-volume production, is used to house VLSI's VL2010 and VL2044 Multiplier/Accumulators. DIP configurations with higher pin counts tend to exhibit unacceptable mechanical problems, such as extremely high insertion and extraction forces.

DIPs are available, in even-pin-count steps, in packages as low as two pins. A variation of the DIP that has gained some acceptance is the SIP, or single in-line package. The SIP, mounted lying on its edge, uses very little printed circuit board space and frequently contains a number of memory die in high-density memory applications. However, as desirable as the SIP may seem, it is not the major evolutionary path of the DIP. The SIP allows little air circulation for cooling, is hard to handle, and is not generally accepted as a standard. The DIP evolution lies in surface mounting the device.

SMALL-OUTLINE INTEGRATED CIRCUITS

The small-outline integrated circuit (SOIC) is a descendant of the DIP. Sometimes called the "Swiss" outline integrated circuit in honor of its country of origin, this package solves many of the problems of the DIP, while retaining many of its advantages. The gull-wing lead rests on top of the printed circuit board rather than going through it. For most types, its leads are exactly half the length that the DIP's are, and it maintains the same basic rectangular package aspect ratio of the DIP. This, however, becomes a disadvantage in high-pin-count applications. For more than 28 pins, many designers prefer the square aspect of the plastic leaded chip carrier (PLCC) to the SOIC. The small package mass of the SOIC does not allow the same thermal dissipation that can be expected in a standard DIP, which becomes a minor problem as more chips are made in the generally lower power consuming CMOS process. Most importantly, the SOIC consumes only about 30% of the real estate consumed by the standard DIP. It is estimated that nearly 1.5 billion SOIC units will be shipped in 1986.

CHIP CARRIERS

Chip carriers have been around for several years in various forms, and are just now coming into widespread usage. Generally, the terminal spacing of chip carriers is 1.27 mm (50 mils), but several special types have 1.0 mm (40 mil) spacing for use by companies engaged in the pocket pager business. Some variations are available in 0.64 mm (25 mils) also. The ceramic versions of chip carriers have become very popular in military applications for the same reason the ceramic side-brazed DIP has: their mechanical ruggedness. Frequently, ceramic leadless chip carriers (LCCs) are soldered in; others use connectors, while still others have their own leads and are inserted as a leaded device. Due to the dissimilar coefficient of expansion of materials (package alumina and printed circuit board fiberglass) and the lack of pins on the leadless versions to provide flexibility or compliance, the ceramic leadless chip carriers should be soldered to a material that has the same thermal expansion characteristics as they have. This has become very popular

in military applications where weight and space are at a premium and, generally, cost is not the primary consideration.

The plastic leaded chip carrier (PLCC) has very quickly become the most popular of all the chip carriers. The PLCC represented about 61% of the chip carriers shipped in 1985 (approximately 400 million units). Although there is debate on the issue of board space consumption, the PLCC and SOIC consume about the same amount of board space in the 24- to 28-pin configurations. In lower pin count applications, the SOIC seems to be more space-effective; when over 24 pins or so, the PLCC seems to have the edge in most applications. In applications over 28 pins, the PLCC is the surface-mount package of choice. Its square aspect ratio allows many chip placements that the highly rectangular package of the SOIC does not. In addition, there are rectangular PLCCs to accommodate such rectangular die, such as memories.

CHIP-ON-BOARD MOUNTING

The ultimate in low-cost chip mounting is achieved by the chip-on-board (COB) technology, in which no discrete package is actually employed. The die is soldered onto a copper pad on a printed circuit board. Bonding wires connect the die to smaller bonding pads around the die. The die and wires are then covered by a dollop of epoxy. This technique, while inexpensive, is not generally accepted in industrial or business equipment. It has been extensively employed in video game cartridges, and seems to work quite well there.

PIN GRID ARRAY

The pin grid array (PGA), or "bed of nails," has only been around for ten years, but had a usage of about 5 million in 1985, and its popularity is growing rapidly. This major package variation allows very high pin counts in relatively small spaces with excellent mechanical and thermal characteristics. The 149-pin VL82C389 Message Passing Co-processor (MPC) for Multibus® II systems is a prime example of PGA high-density trends. The major disadvantage of the PGA is its high cost. Virtually all of the 5 million PGA units shipped in 1985 were ceramic. Plastic pin grid arrays are well along in development, and will provide reliable, inexpensive packaging for the many high-pin-count ASIC, memory, and other circuits coming into wide usage.

FLATPACK

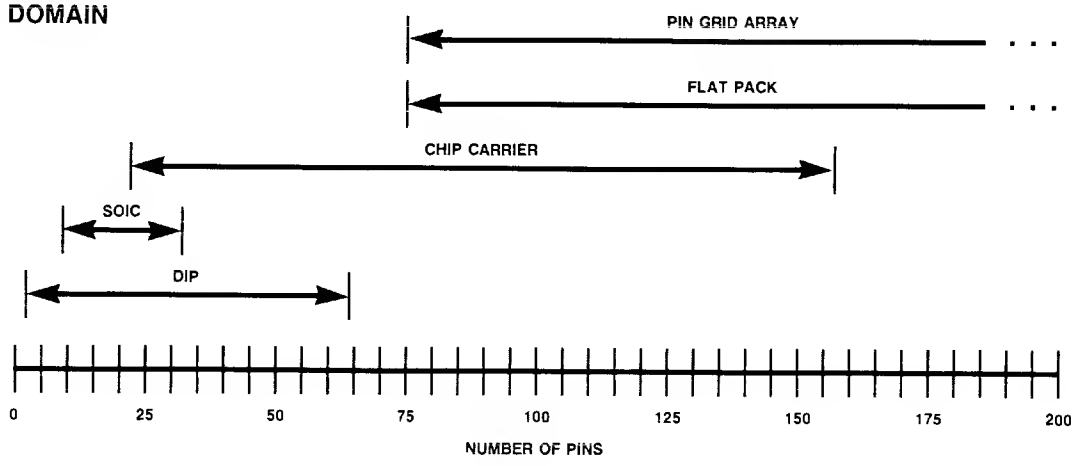
The flatpack holds less than 1% of the IC package market. True to its name, it is flat, small, and has flat leads usually in the same plane as the package body. It is generally harder to handle and test than the other package types, but provides a surface mounting alternative to the pin grid array in very-high-pin-count applications. It is usually surface mounted, "socketed," or suspended through a cut-out hole in the printed circuit board.

SYSTEM CONSIDERATIONS

In the extremely competitive computer market that now exists, every repetitive cost, no matter how small, comes under close scrutiny. Drilling a hole in a printed circuit board costs about $0.001, a fairly small amount until it is multiplied by the thousands of holes that frequently occur in each board. This becomes a significant consideration at the system level. Even though re-tooling costs are high, many companies are converting (some at least partially) to surface-mounting equipment. Surface mounting allows more chips in a much smaller area, but not all functions are yet available in surface-mount packages. Some companies have solved this problem by designing both through-the-board and surface-mount devices onto the same board. Others continue to use the older technology until they can re-tool for 100% surface mount.

Application-specific integrated circuits (ASICs) and their support devices are requiring packages with ever-increasing pin counts. The pin count domain diagram graphically depicts the typical domain of pin counts for five basic package types. While there is a good deal of overlap, chip carriers and pin grid arrays will become the package of choice in future systems containing devices of high pin count. Since the PGA device

PIN COUNT DOMAIN



®Multibus is a registered trademark of Intel Corporation.

ORDERING AND PACKAGING INFORMATION

does not support surface-mount technology, chip carriers or flatpack technology will have to be implemented as pin counts exceed 170 using surface-mount systems.

CONCLUSION

There will be no panacea package that will exclude the use of all others in the future. While there are several criteria for the system designer, Table 1 examines some of the characteristics of packages that will probably occupy the overwhelming majority of printed circuit boards in the future. Leadless chip carriers will be especially popular in military and harsh industrial applications. The DIP, with many billions already in use, will not disappear, but its percentage of market will decrease steadily. Pin grid arrays will remain and increase in popularity as very large devices become more popular and plastic PGAs become readily available. Surface mounting is definitely a wave of the future for many systems. SOIC packaging will increase rapidly for devices of 28 terminals and under, while the mid-range and higher terminal count devices will be housed in PLCCs or flatpacks.

THERMAL CONSIDERATIONS

The devices in this data book have undergone thorough evaluation and characterization to ensure their operation over the specified temperature ranges. While safety margins are used for all parametric tests over the temperature range, the designer should not exceed the temperature limits, even for extremely short intervals. The following notes are presented to ensure a reliable, long-lived system using VLSI's products:

1. While few designs subject devices to extreme cold, such conditions may cause the devices to operate outside of their normal specified ranges. Therefore, the minimum operating temperature specification must be observed as well as the maximum operating temperature.
2. The ambient temperature (TA) specification refers to the air on the surface of the device. The printed circuit board design should be open enough to permit free air flow around the devices.
3. Avoid layouts that place NMOS, HMOS, or CMOS devices near such heat sources as power regulators and devices requiring heat sinks. If the design demands such proximity, ensure that the specified temperature range is not exceeded.
4. Ensure that the power supply voltage is within the specified range. Both low and high voltages beyond the specified limits may cause device overheating.

TABLE 1. PACKAGE CHARACTERISTICS

	JEDEC Leadless Chip Carriers			DIP				
Feature	**A**	**B**	**C**	**Ceramic**	**Plastic**	**SOIC**	**PLCC**	**PGA**
Uses Socket or Connector	Yes	Yes	No	Yes	Yes	No	Yes	Yes
Directly Solderable	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Minimum Usual Terminal Count	14	14	14	6	6	8	16	40
Maximum Usual Terminal Count	156	156	156	64	64	28	156	225
Pin Spacing mm (mils)	1.27 (50)	1.27 (50)	1.27 (50)	2.5 (100)	2.5 (100)	1.27/1.0 (50/40)	1.27/1.0 (50/40)	2.5 (100)
Relative Cost (1 = Most Costly)	3	4	5	2	8	7	6	1

VLSI TECHNOLOGY, INC.

SECTION 3

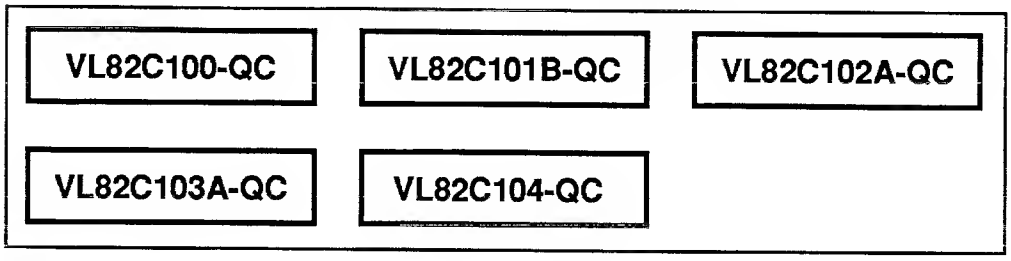
SELECTOR GUIDE

Logic Products Division


VLSI TECHNOLOGY, INC.

VLSI'S POPULAR 12 MHz CHIP SET

VL82CPCAT-QC (12 MHz 0/1 WS) SEE SCHEMATIC, PAGE 7-9

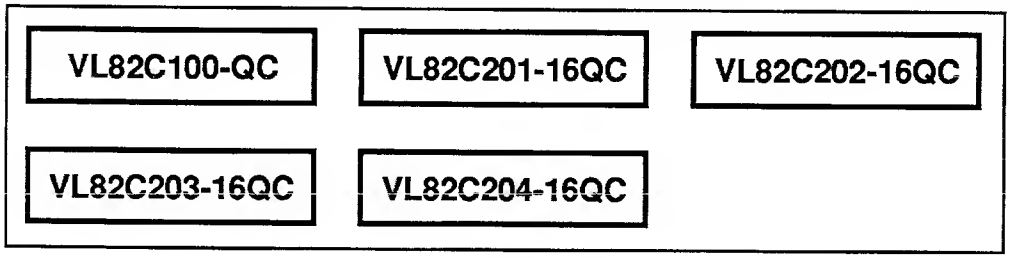


FEATURES

- 100% PC/AT-Compatible
- 1 ws/120 ns DRAM, 0 ws/80 ns DRAM
- 8 MHz Backplane with External Clock Modulation PAL

VLSI'S FASTER 16 MHz CHIP SET

VL82CPCAT-16QC (16 MHz, 0/1 WS) SEE SCHEMATIC, PAGE 7-27 , 386SX/387SX INTERFACE, PAGE 7-3

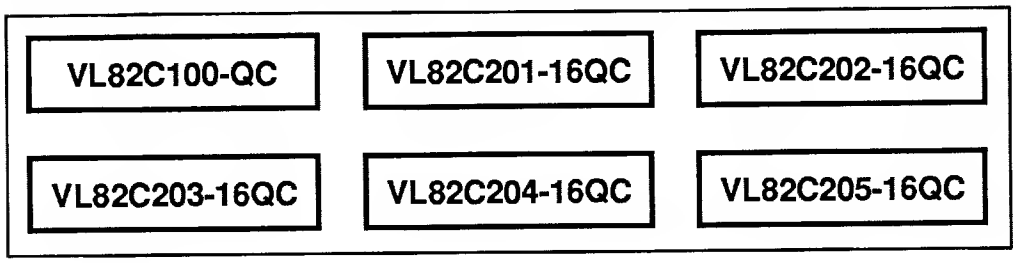


FEATURES

- 100% PC/AT-Compatible
- 1 ws/80 ns DRAM, 0 ws/60 ns DRAM
- Shadow RAM Feature
- 8 MHz Backplane I/O Operation
- On-board EMS 4.0 Memory

VLSI'S FASTER ENHANCED 16 MHz CHIP SET

VL82CPCPM-16QC (16 MHz, PAGE-MODE) SEE 386SX/387SX INTERFACE, PAGE 7-3

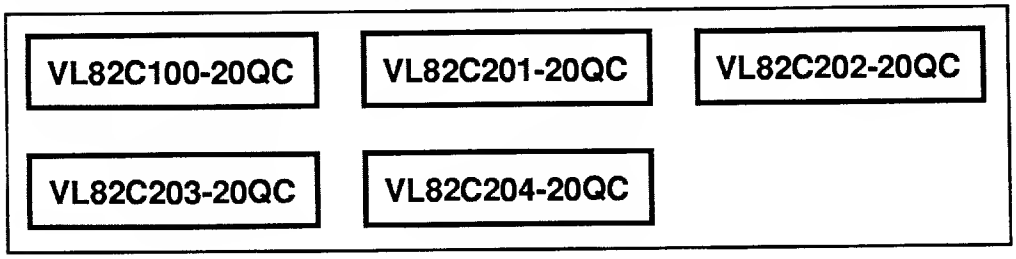


FEATURES

- 100% PC/AT-Compatible
- Page-mode 0.6 ws with 100 ns DRAM
- Shadow RAM Feature
- 8 MHz Backplane I/O Operation
- On-board EMS 4.0 Memory

VLSI'S HIGH-SPEED 20 MHz CHIP SET

VL82CPCAT-20QC (20 MHz, 0/1 WS) SEE 386SX/387SX INTERFACE, PAGE 7-3



FEATURES

- 100% PC/AT-Compatible
- 1 ws/80 ns DRAM
- Shadow RAM Feature
- 10 MHz Backplane I/O Operation
- On-board EMS 4.0 Operation

VLSI'S HIGH-SPEED ENHANCED 20 MHz CHIP SET

VL82CPCPM-20QC (20 MHz, PAGE-MODE) SEE 386SX/387SX INTERFACE, PAGE 7-3

VL82C100-20QC	VL82C201-20QC	VL82C202-20QC
VL82C203-20QC	VL82C204-20QC	VL82C205-20QC

FEATURES

- 100% PC/AT-Compatible
- 0.6 ws/80 ns DRAM
- Shadow RAM Feature
- 10 MHz Backplane I/O Operation
- On-board EMS 4.0 Operation

VLSI'S HIGH-INTEGRATION PC/AT-COMPATIBLE DEVICES

COMBO

(RTC, KEYBOARD CONTROLLER, DUAL UART, CENTRONICS, IDE INTERFACE) PAGE 6-89

VL82C106-QC

UART PAGE 6-3

VL16C450-QC

PAGE 6-63

VL16C550-QC

UART/CENTRONICS PAGE 6-23

VL16C451-QC

PAGE 6-43

VL16C452-QC

PAGE 6-85

VL16C552-QC

Note: In addition to the commercial (QC) temperature range, TA = 0°C to +70°C, the 16 MHz and 20 MHz PCAT-compatible chip sets are also available in the industrial (QI) temperature range of TA = –40°C to +85°C.

VLSI TECHNOLOGY, INC.

SECTION 4

PC/AT-COMPATIBLE DEVICES

Logic Products Division


VLSI TECHNOLOGY, INC.

VL82C100

PC/AT-COMPATIBLE PERIPHERAL CONTROLLER

FEATURES

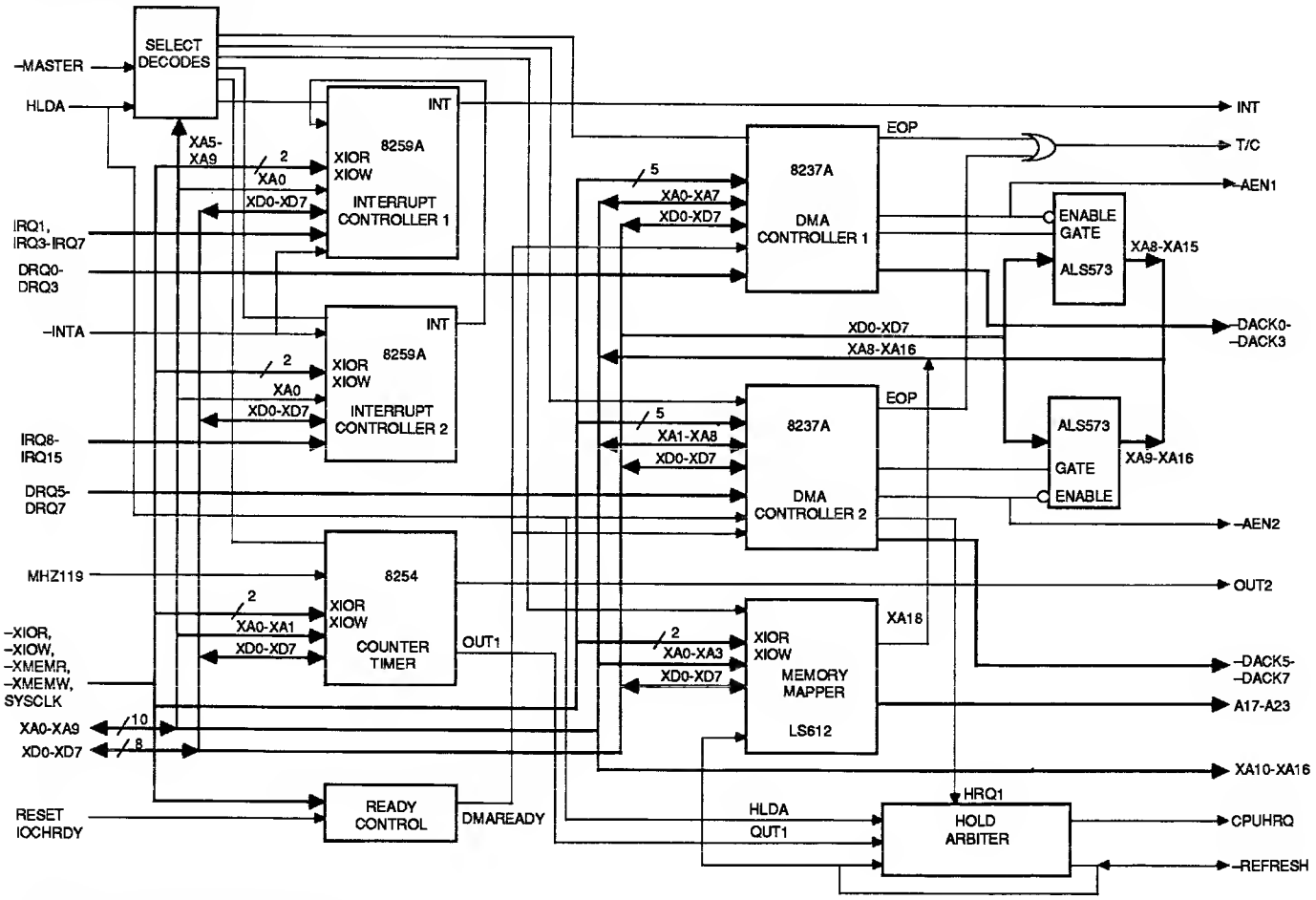
- Fully compatible with IBM PC/AT-type designs
- Replaces 19 logic devices
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Seven DMA channels
- 14 external interrupt requests
- Three timer/counter channels
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C100 PC/AT-Compatible Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74ALS573 Octal Three-State Latches, a 74ALS138 3-to-8 Decoder, and five other less-complex integrated circuits. Using this internal functionality, the VL82C100 provides all 24 address bits for 16M bits of DMA address space. It also interfaces directly to the CPU to handle all interrupts. Timing for refresh cycles, and arbitration, between refresh and DMA hold requests, are also controlled by the VL82C100.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C100 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM

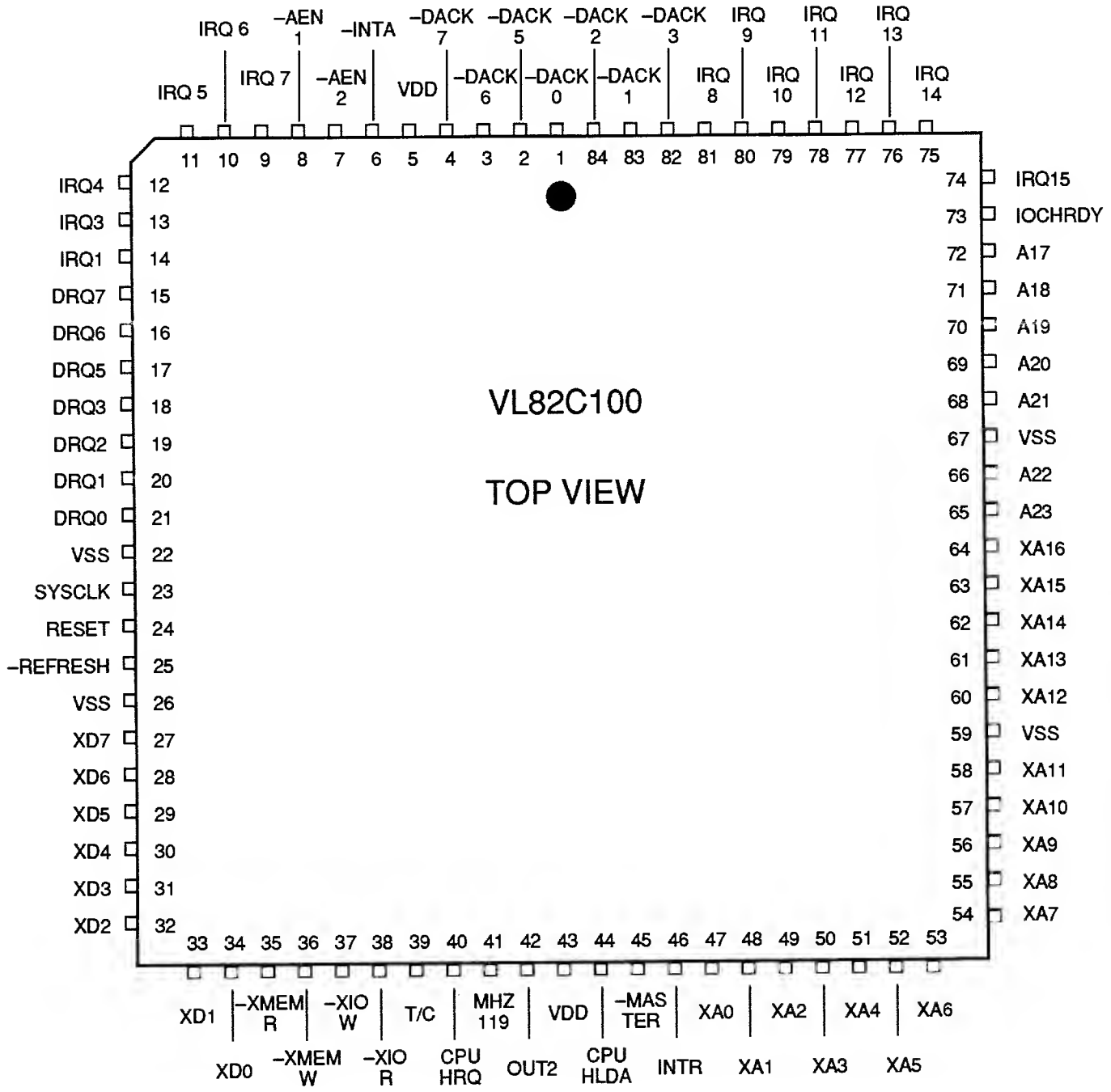


ORDER INFORMATION

Part Number	Clock Freq.	Package
VL82C100-QC VL82C100-QI	12/16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C100-20QC VL82C100-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

PIN DIAGRAM


VL82C100
TOP VIEW
1 IRQ 5
2 IRQ 7
3 –AEN 2
4 VDD
5 –DACK 6
6 –DACK 0
7 –DACK 1
8 IRQ 8
9 IRQ 10
10 IRQ 12
11 IRQ 14
12 IRQ4
13 IRQ3
14 IRQ1
15 DRQ7
16 DRQ6
17 DRQ5
18 DRQ3
19 DRQ2
20 DRQ1
21 DRQ0
22 VSS
23 SYSCLK
24 RESET
25 –REFRESH
26 VSS
27 XD7
28 XD6
29 XD5
30 XD4
31 XD3
32 XD2
33 XD1
34 –XMEMR
35 –XIOW
36 T/C
37 MHZ 119
38 VDD
39 –MASTER
40 XA0
41 XA2
42 XA4
43 XA6
44 XA5
45 XA3
46 XA1
47 INTR
48 CPU HLDA
49 OUT2
50 CPU HRQ
51 –XIOR
52 –XMEMW
53 XD0
54 XA7
55 XA8
56 XA9
57 XA10
58 XA11
59 VSS
60 XA12
61 XA13
62 XA14
63 XA15
64 XA16
65 A23
66 A22
67 VSS
68 A21
69 A20
70 A19
71 A18
72 A17
73 IOCHRDY
74 IRQ15
75 IRQ 14
76 IRQ 13
77 IRQ 12
78 IRQ 11
79 IRQ 10
80 IRQ 9
81 –DACK 3
82 –DACK 2
83 –DACK 5
84 –DACK 7
1 –INTA
2 –AEN 1
3 IRQ 6

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
SYSCLK	23	I	System Clock Input - This pin is divided by two internally to generate DMACLK for the 8237 DMA controllers. It is also used in the hold request arbiter. SYSCLK can be driven at a frequency of up to 20 MHz.
RESET	24	I	Reset - An active high input used to clear the DMA controller megacells and hold request arbiter.
XD0-XD7	34-27	I/O	Peripheral Data Bus Bits 0-7 - These lines are three-state bidirectional signals connected to the peripheral data bus. (X data bus in PC/AT-type designs.)
XA0-XA9	47-56	I/O	Peripheral Address Bus Bits 0-9 - The ten least significant address bits on the XA bus are bidirectional. They are outputs during DMA cycles and are inputs all other times. As inputs they are used to generate chip selects for the megacells and address internal registers within each megacell.
XA10, XA11 XA12-XA16	57, 58 60-64	O	Peripheral Address Bus Bits 10-16 - The seven most significant address bits on the XA bus are three-state outputs only. They actively drive the XA bus during DMA cycles.
A17-A21 A22, A23	72-68 66, 65	O	CPU Address Bus Bits 17-23 - These address bits are connected to the CPU's address bus and are driven from the LS612 memory mapper any time CPUHLDA is active (high) and –MASTER is inactive (high). They are in a three-state condition during all other times.
–XIOW	37	I/O	I/O Write – This is a bidirectional active low three-state line. It is an output during a DMA cycle and will be an input at all other times.
–XIOR	38	I/O	I/O Read - This is a bidirectional active low three-state line. It is an output during a DMA cycle and will be an input at all other times.
–XMEMW	36	I/O	Memory Write - This is a bidirectional active low three-state line. It is an output during a DMA cycle and will be an input at all other times. In the input mode –XMEMW is used to enable the hold request arbiter after an interrupt acknowledge cycle.
–XMEMR	35	O	Memory Read - This is a three-state output which will be active during a DMA cycle.
IRQ1, IRQ3-IRQ7 IRQ8-IRQ15	14, 13-9, 81-74	I	Interrupt Request Bits 1, 3-7, 8-15 - These are asynchronous inputs and are the interrupt request inputs to the 8259 megacells. IRQ2 and IRQ0 are not available as inputs to the chip. IRQ2 is used to cascade the two 8259's together and IRQ0 is connected to the output of the 8254 counter 0.
INTR	46	O	Interrupt Request - INTR is an output used to interrupt the CPU and is generated whenever a valid IRQ is received.
–INTA	6	I	Interrupt Acknowledge - This input is used to enable the 8259 interrupt controllers to vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
DRQ0-DRQ3 DRQ5-DRQ7	21-18 17-15	I	DMA Request Bits 0-3, 5-7 - These input signals are the individual asynchronous requests for DMA service connected to the 8237 megacells. DRQ0 through DRQ3 support transfers from 8 bit I/O adapters to/from 8 or 16 bit system memory. DRQ5 through DRQ7 support transfers from 16 bit I/O adapters to/from 16 bit system memory. DRQ4 is not available as it is used to cascade the two DMA controllers together.
–DACK0- –DACK3 –DACK5- –DACK7	1, 83, 84, 82, 2-4	O	DMA Acknowledge Bits 0-3, 5-7 - These output signals are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is programmable and is set to active low on reset.

4

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
CPUHRQ	40	O	CPU Hold Request - This output is the hold request to the CPU and is used to request control of the system bus. It can be issued by a request from the DMA controllers or the timer when it is time for a refresh cycle.
CPUHLDA	44	I	CPU Hold Acknowledge - This input from the CPU indicates that it is acknowledging the hold request and is no longer driving the system bus. It indicates that the VL82C100 can now drive the address and control buses.
–AEN1	8	O	Address Enable 1 - This active low signal indicates when DMA Controller 1 is enabling addresses onto the peripheral address bus for a DMA transfer.
–AEN2	7	O	Address Enable 2 - This active low signal indicates when DMA Controller 2 is enabling addresses onto the peripheral address bus for a DMA transfer.
T/C	39	O	Terminal Count - Indicates one of the DMA channels terminal count has been reached.
–MASTER	45	I	Master - An external device will pull this input low to disable the DMA controllers and get access to the system bus. It indicates an I/O channel controls the system buses.
IOCHRDY	73	I	I/O Channel Ready - An input used to extend the memory read and write pulses from the 8237 to accommodate slow devices.
MHZ119	41	I	This is the 1.19 MHz clock input for the 8254 counter.
OUT2	42	O	Out 2 - The output of counter 2 in the 8254 megacell.
–REFRESH	25	I/O	Refresh - This I/O signal will be pulled low by the VL82C100 whenever the 8254 counter 1 issues a CPUHRQ to the CPU and a hold acknowledge is received from the CPU. It is used internally to select a location in the memory mapper which drives the upper address bus A17-A23. –REFRESH can also be used as an input if the refresh timing is to come from a source other than the 8254 channel 1 counter. –REFRESH is an open drain output capable of sinking 20 mA and requires an external pull-up resistor.
VDD	5, 43		System Power: 5 V
VSS	22, 26, 59, 67		System Ground

FUNCTIONAL DESCRIPTION

The VL82C100 Peripheral Controller integrates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer and a 74LS612 equivalent along with support logic onto a single chip. The peripheral controller will replace all the logic on the X bus of an AT-compatible design except the keyboard controller and real time clock.

The VL82C100 is broken up into five major subsections. The megacell chip select subsection consists of decodes of the signals –MASTER, CPUHLDA, and the address bus XA0-XA9. This decode is used to generate the chip select signals to each of the megacells within the VL82C100.

The DMA subsection consists of two 8237 megacells, two 8 bit latches to hold the middle range address bits during a DMA cycle and a 74LS612 equivalent megacell to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to force all DMA cycles to have one wait state inserted and some logic to delay the leading edge of the –XMEMR signal for one DMA clock cycle. These groups of logic are used to maintain AT-compatibility. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8 bit I/O adapters and the other three are used for 16 bit I/O adapters. All channels are capable of addressing all memory locations in a 16 megabyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to allow for 15 possible interrupt sources. One of these interrupt request lines is used internally, so there are a total of 14 possible external interrupts.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters run off a common clock input. The output of Counter 0 is routed to the interrupt controller subsection to be

TABLE 1. ADDRESS DECODE FOR CHIP SELECTS

XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range	Chip Select Generated
0	0	0	0	0	X	X	X	X	X	000-01F	DMA Controller 1 (8237)
0	0	0	0	1	X	X	X	X	X	020-03F	Int. Controller 2 (8259)
0	0	0	1	0	X	X	X	X	X	040-05F	Counter/Timer (8254)
0	0	0	1	1	0	X	X	X	1	061	Port B (TMGAT2)
0	0	1	0	0	X	X	X	X	X	080-09F	DMA Page Reg. (74LS612)
0	0	1	0	1	X	X	X	X	X	0A0-0BF	Int. Controller 2 (8259)
0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA Controller 2 (8237)

used as interrupt request 0. The output from Counter 1 is routed to the hold request arbiter to initiate refresh cycles. Counter 2's output is available as an external pin. The counter/timer subsection also contains a flip-flop which can be written to with an –XIOW command to control the gate input to Counter 2.

The hold request arbiter and refresh subsection is used to arbitrate between a possible hold request from the DMA subsection or Counter 2 of the counter/timer subsection. This block of logic also controls the –REFRESH output signal.

MEGACELL CHIP SELECTS

Address bits XA0-XA9 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

For all the address decodes shown the chip selects are disabled if both CPUHLDA and –MASTER are high.

The address decode at address 061 hex goes to a single flip-flop used to clock in the value of TMGAT2 in an AT-compatible design. This flip-flop will clock in the value on XD0 on the rising edge of –XIOW whenever that address decode is valid. The output of the flip-flop is used to gate counter 2 in the 8254 megacell on and off. This is the only bit of Port B in the VL82C100 and it cannot be read externally. The entire Port B is located in the Memory Controller Device of the chip set. Bit 0 is duplicated in the VL82C100 only to save an input pin.

DMA SUBSECTION

The DMA subsection controls DMA transfers between an I/O channel and on-board or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged the DMA controller will drive all 24 address bits for a total addressing capability of 24 megabytes, and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA controllers are 8237 compatible, internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus, and the function of a 74LS612 memory mapper is provided to generate the upper address bits.

DMA CONTROLLERS

The VL82C100 supports seven DMA channels using two 8237 equivalent megacells capable of running at a 10 MHz DMA clock (20 MHz SYSCLK) rate. DMA Controller 1 contains channels 0 through 3. These channels support 8 bit I/O adapters. Channels 0 through 3 are used to transfer data between 8 bit peripherals and 8 or 16 bit memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data in 64 kilobyte pages.

DMA Controller 2 contains channels 4 through 7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5 through 7 support 16 bit I/O adapters to transfer data between 16 bit I/O adapters and 16 bit system memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data in 128 kilobyte pages. Channels 5, 6, and 7 are meant to transfer 16 bit words only and cannot address single bytes in system memory.

DMA CONTROLLER REGISTERS

The 8237 megacells can be programmed any time CPUHLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA 2 are for the 16 bit DMA channels and DMA 1 corresponds to the 8 bit channels. When writing to a channel's address or word count register the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16 bit registers. The value on the data bus is written into the upper byte or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the Clear Byte Pointer Flip-Flop command. After this command the first read/write to an address or word count register will read/write to the low byte of the 16 bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count

FIGURE 1. DMA SUBSECTION

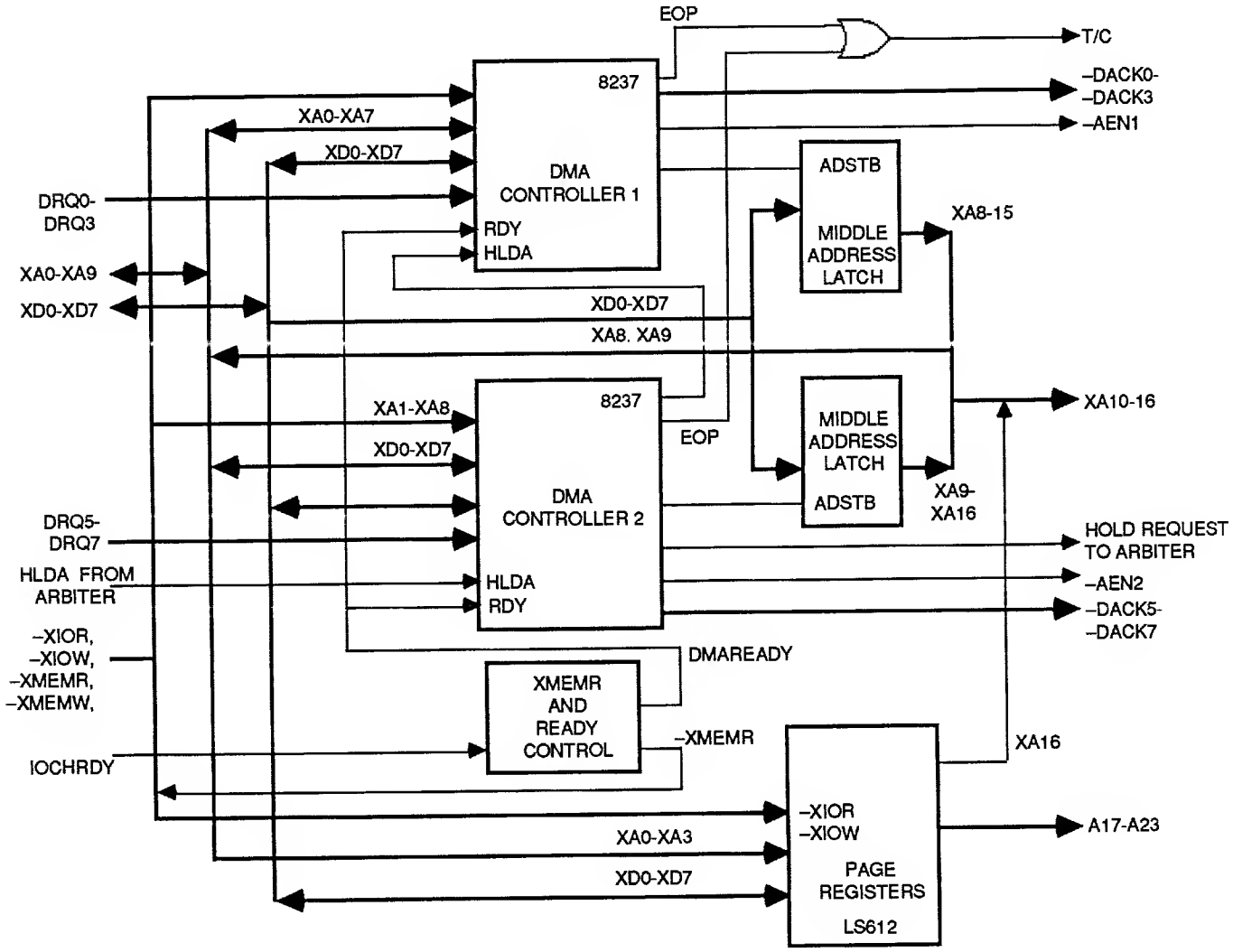


TABLE 2. DMA CONTROLLER REGISTERS ADDRESSES

Hex Address		
DMA2	DMA1	Register Function
0C0	000	Channel 0 Base and Current Address Register
0C2	001	Channel 0 Base and Current Word Count Register
0C4	002	Channel 1 Base and Current Address Register
0C6	003	Channel 1 Base and Current Word Count Register
0C8	004	Channel 2 Base and Current Address Register
0CA	005	Channel 2 Base and Current Word Count Register
0CC	006	Channel 3 Base and Current Address Register
0CE	007	Channel 3 Base and Current Word Count Register
0D0	008	Read Status Register/Write Command Register
0D2	009	Write Request Register
0D4	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-Flop
0DA	00D	Read Temporary Register/Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

register will read/write to the high byte of the 16 bit register and the byte pointer flip-flop will toggle back to a zero. Refer to the 8237 data sheet for more information on programming the 8237 megacell.

The 8237 DMA controller megacells allow the user to program the active level (low or high) of the DRQ and –DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DRQ signals active high and the –DACK signals active low.

When programming the 16 bit channels (channels 5, 6, and 7) the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16 bit channels is the number of 16 bit words to be transferred, not the number of bytes as is the case for the 8 bit channels.

It is recommended that all internal locations, especially the mode registers, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

MIDDLE ADDRESS BIT LATCHES

The middle address bits of the 24 bit address range are held in two sets of 8 bit registers, one register for each DMA controller. The DMA controller will drive the value to be loaded onto the data bus and then issue an address strobe signal to latch the data bus value into these registers. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8 bit address increments across the 8 bit subpage boundary during block transfers. These registers cannot be written to or read externally. They are loaded only from the address strobe signals from the megacells and the outputs go only to the XA8-XA16 pins.

PAGE REGISTERS

The equivalent of a 74LS612 is used in the VL82C100 to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8 bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16 bit channels (channels 5, 6, and 7) are every 128 kilobytes. There are a total of 16 eight bit registers in the 74LS612 megacell. The page registers are in the I/O address space as shown.

Page Register	Hex I/O Address
DMA channel 0	087
DMA channel 1	083
DMA channel 2	081
DMA channel 3	082
DMA channel 5	08B
DMA channel 6	089
DMA channel 7	08A
Refresh	08F

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 080 and 08F that are not shown, are not used by the DMA channels but can be read or written to by the CPU. Address 08F is used to drive a value onto the upper address bits A17-A23 of the CPU's address bus during a refresh cycle.

ADDRESS GENERATION

The DMA addresses are setup such that there is an upper address portion, used to select a specific page, a middle address portion, used to select a block within the page, and a lower address portion.

The upper address portion is generated by the page registers, in the 74LS612 equivalent megacell. The page registers for each channel must be setup by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8 bit channels (channels 0 through 3) and 128 kilobytes for 16 bit channels (channels 5, 6, and 7). The

TABLE 3. ADDRESS SOURCE GENERATION

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8 Bit DMA Address Bits	16 Bit DMA Address Bits
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			XA16	
	D7		XA15	XA16
	D6		XA14	XA15
	D5		XA13	XA14
	D4		XA12	XA13
	D3		XA11	XA12
	D2		XA10	XA11
	D1		XA9	XA10
	D0		XA8	XA9
		A7	XA7	XA8
		A6	XA6	XA7
		A5	XA5	XA6
		A4	XA4	XA5
		A3	XA3	XA4
		A2	XA2	XA3
		A1	XA1	XA2
		A0	XA0	XA1
		VSS		XA0

DMA page register values are output on A17-A23 and XA16 for 8 bit channels, and A17-A23 for 16 bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are 256 bytes for 8 bit channels (channels 0 through 3) and 512 bytes for 16 bit channels (channels 5, 6, and 7). This middle address portion is output by the 8237 megacells onto the data bus during state S1. The internal middle address bit latches will latch in this value. The middle address bit latches are output on XA8-XA15 for 8 bit channels, and XA9-XA16 for 16 bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on XA0-XA7 for 8 bit channels, and XA1-XA8 for 16 bit channels. XA0 is forced low during 16 bit DMA operations.

Table 3 is shown to illustrate the source for all address bits during both 8 and 16 bit transfers.

READY CONTROL

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. To maintain an AT-compatible design, the VL82C100 ready control logic forces one wait state on every DMA transfer. The external signal IOCHRDY goes into the ready control logic to extend transfer cycles to longer than one wait state if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock during the forced wait state. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time before the second phase of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4 (see timing diagrams).

XMEMR DELAY

To maintain an AT-compatible design, the VL82C100 inserts a DMA clock cycle delay in the falling edge of the –XMEMR signal. –XMEMR will go low one DMA clock (two SYSCLK's) later than the –MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time the –MEMR signal from the megacell goes high.

EXTERNAL CASCADING

An external DMA controller or bus master can be attached to an AT-compatible design through the VL82C100's DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in cascade mode. That channel's DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding –DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the VL82C100's seven channels is programmed in cascade mode and that channel is acknowledged the VL82C100 will not drive the data bus, the command signals, or the XA address bus. However, the upper address bits A17-A23 will be driven with the value programmed into the page register for the channel programmed in cascade mode.

An external device can become a bus master and control the system address, data, and command buses in much the same manner. One of the DMA channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's –DACK line goes active, the external device can then pull the –MASTER signal low to force the system buses to a high impedance state. As in the DMA controller cascading, the VL82C100 will not drive the X buses while the cascaded channels –DACK signal is active. Also, the VL82C100 will force the upper address bits A17-A23 to a high impedance state while –MASTER is held low.

INTERRUPT CONTROLLER SUBSECTION

The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally on the VL82C100 and one of the interrupt request inputs is internally connected to an output of the 8254 counter/timer megacell. This allows a total of 14 external interrupt requests.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the –INTA pulses from the CPU. On the first –INTA cycle the

4

FIGURE 2. INTERRUPT CONTROLLER SUBSECTION

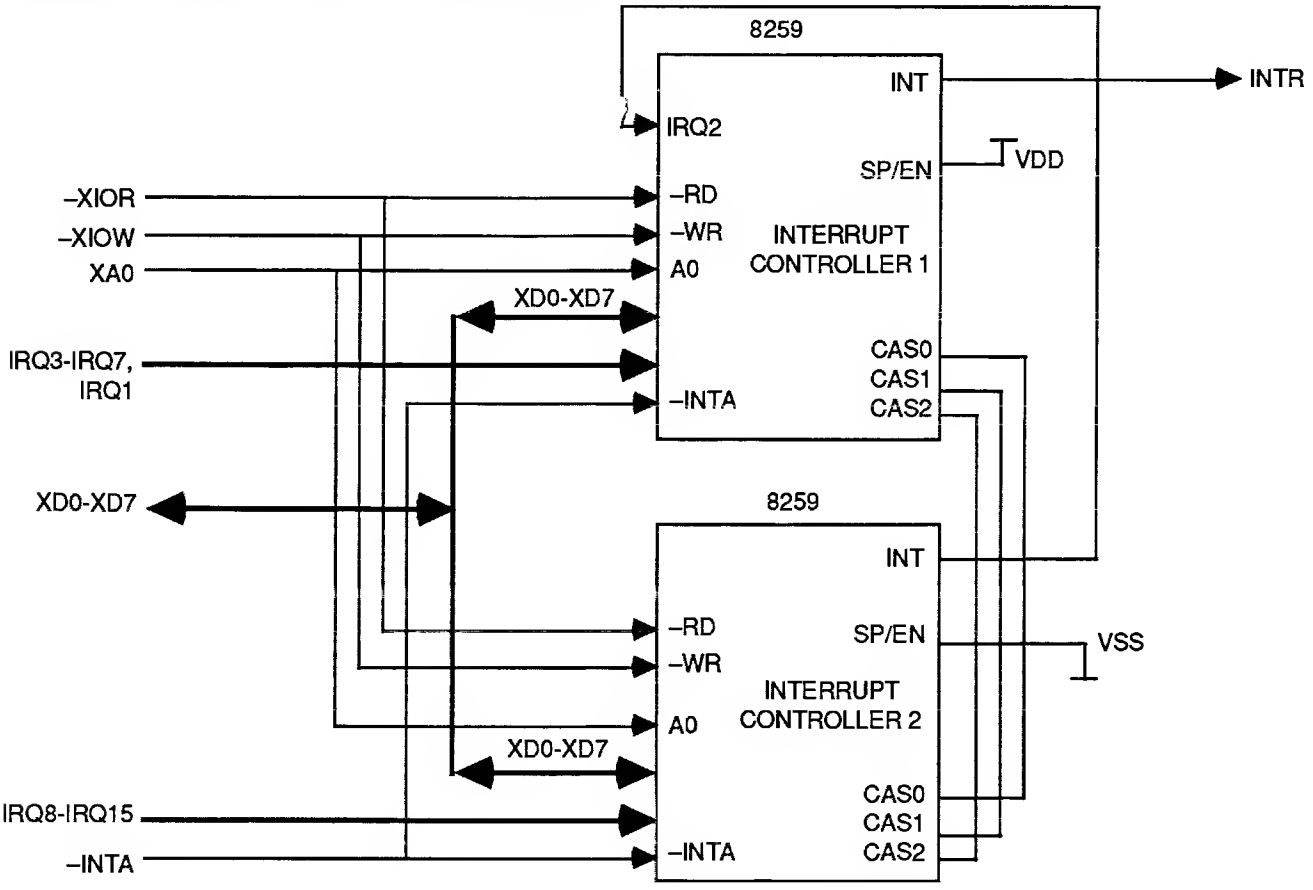


TABLE 4. WRITE OPERATIONS

Hex Address				
INT1	INT2	XD4	XD3	Register Function
020	0A0	1	X	Write ICW1
021	0A1	X	X	Write ICW2
021	0A1	X	X	Write ICW3
021	0A1	X	X	Write ICW4 (If Needed)
021	0A1	X	X	Write OCW1
020	0A0	0	0	Write OCW2
020	0A0	0	1	Write OCW3

TABLE 5. READ OPERATIONS

Hex Address		
INT1	INT2	Register Function
020	0A0	Interrupt Request Reg., In-Service Reg., or Poll Command
021	0A1	Interrupt Mask Register

cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second –INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the VL82C100, they should never be programmed to operate in the buffered mode.

INTERRUPT CONTROLLER INTERNAL REGISTERS

The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 4 shows the correct addressing for each of the 8259 registers.

Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 8259 megacell ICW3 is optional. But since the two 8259's in this chip are cascaded together, they should always be programmed in cascade mode and ICW3 will always be needed. Refer to the 8259 data sheet for more information on programming the 8259 megacell.

When reading at address 020 or 0A0 hex, the register read will depend on how Operation Control Word 3 was setup prior to the read.

TIMER/COUNTER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in the diagram. The clocks for each of the three internal counters are tied to the single input pin MHZ119. The gate inputs of Counters 0 and 1 are tied high to enable those Counters at all times. The gate input of Counter 2 is tied to the output of a flip-flop inside the

FIGURE 3. TIMER/COUNTER SUBSECTION

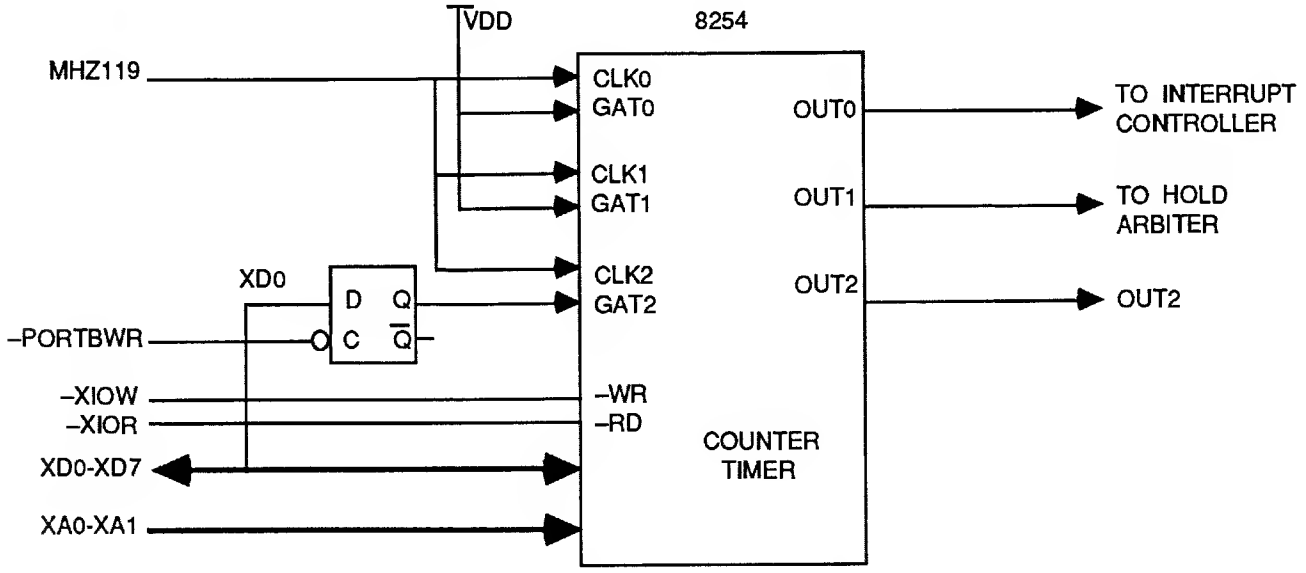


TABLE 6. TIMER/COUNTER REGISTERS

Hex Address	-XIOR	-XIOW	Register Function
040	1	0	Write Initial Count to Counter 0
040	0	1	Read Latched Count or Status from Counter 0
041	1	0	Write Initial Count to Counter 1
041	0	1	Read Latched Count or Status from Counter 1
042	1	0	Write Initial Count to Counter 2
042	0	1	Read Latched Count or Status from Counter 2
043	1	0	Write Control Word
043	0	1	No Operation

VL82C100. This flip-flop will clock in the value on XD0 during an I/O write to Port B. The output of the flip-flop is used to gate Counter 2 in the 8254 megacell on and off.

Only one of the 8254 megacell counter outputs is directly available at an external pin. Counter 0's output is connected to the IRQ0 input of interrupt controller 1. Counter 1's output goes to the hold request arbiter and refresh subsection to initiate a refresh cycle. Finally, Counter 2's output goes directly to the output pin OUT2.

TIMER/COUNTER INTERNAL REGISTERS

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 6 shows the correct addressing for each of the 8254 registers.

The write control word at address 043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

HOLD REQUEST ARBITER AND REFRESH SUBSECTION

The hold request arbiter and refresh subsection is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller 2 issues a hold request or when the output of counter 1 in the 8254 megacell makes a low to high transition. To provide equal weight to these two possible sources for a hold request, the hold request from the DMA controller is sampled on the rising edge of the internal DMA clock and the request from the counter/timer is sampled on the falling edge of the internal DMA clock. The request which is clocked in first will be granted by the arbiter and the other request inhibited until the first request is finished.

At the end of a hold request from either source the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter will give an acknowledge signal to that source and leave the CPUHRQ line active. This will continue as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the CPUHRQ signal and return control back to the CPU.

In the case of the DMA controller's hold request winning in the arbiter, the arbiter will assert the CPUHRQ output and wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause a hold acknowledge to be sent to the DMA controller. When the DMA controller is finished it will negate its hold request signal to the arbiter. The arbiter will then switch to a –REFRESH cycle, if a hold request is pending from the 8254 counter/timer, or negate the CPUHRQ line and return control to the CPU.

In the case of a refresh cycle winning the arbitration, the CPUHRQ output will be asserted and the arbiter subsection will wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause the VL82C100 to pull the –REFRESH pin low. –REFRESH will remain low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK the –REFRESH pin will go to a high impedance state enabling it to be pulled up by an external resistor, and the CPUHRQ signal will be negated. If the hold request arbiter has a hold request from the DMA controller pending on the fourth rising edge of SYSCLK, the –REFRESH cycle is extended for one more SYSCLK cycle (see waveforms). The hold request arbiter will then acknowledge the hold request of the DMA controller.

Refresh cycles can be extended by an external source by forcing the IOCHRDY input low a setup time before the third rising edge of SYSCLK. –REFRESH will remain low until IOCHRDY is returned high.

The pin –REFRESH is a bidirectional open drain I/O pin and requires an external pull-up. It can also be used as an input if a refresh cycle is to be initiated from an external source.

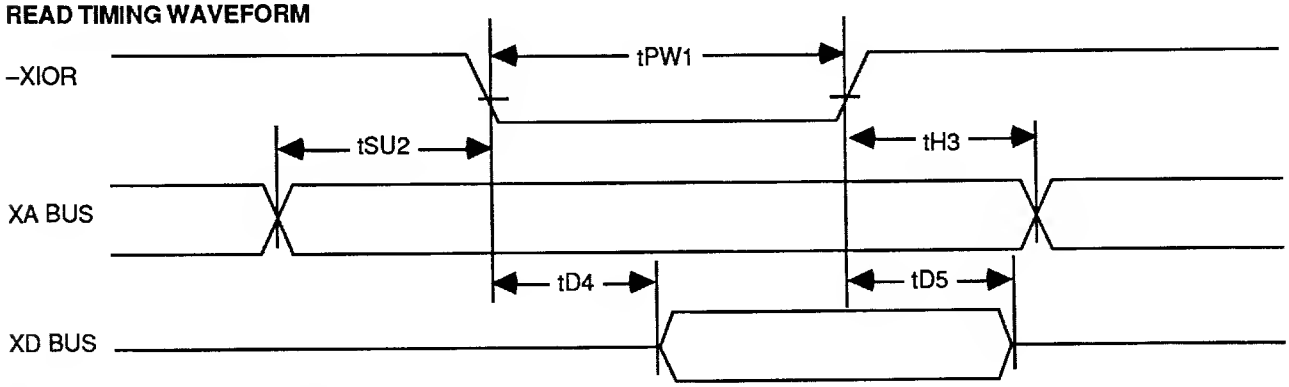
4

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

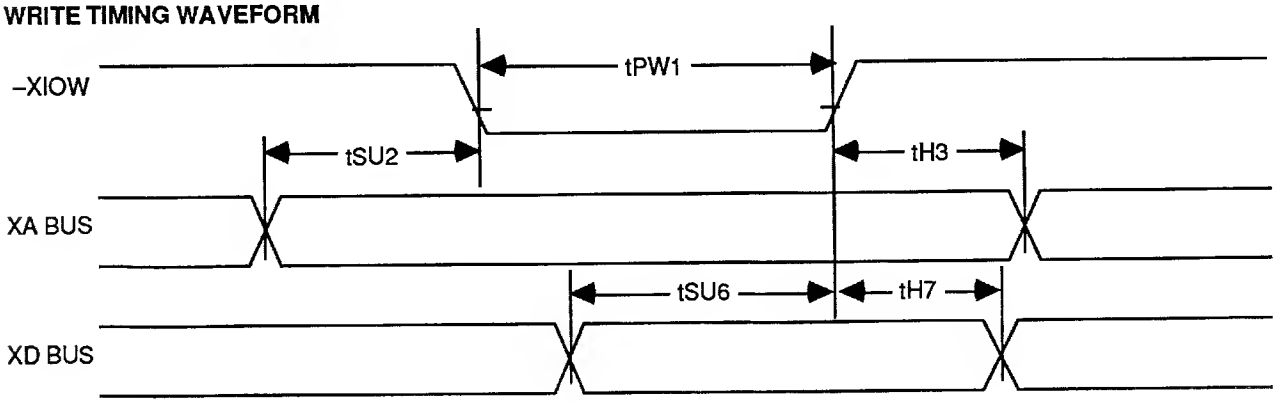
READ/WRITE MODE TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tPW1	–XIOR or –XIOW Pulse Width Low	180		150		ns	
tSU2	XA Address Valid to –XIOR or –XIOW Low Setup Time	30		25		ns	
tH3	XA Address from –XIOR or –XIOW High Hold Time	15		15		ns	
tD4	XD Data Valid Delay from –XIOR Low		120		110	ns	
tD5	XD Data Float Delay from –XIOR High	0	80	0	75	ns	
tSU6	XD Data Valid to –XIOW High Setup Time	110		100		ns	
tH7	XD Data Valid from –XIOW High Hold Time	15		15		ns	
tPW8	RESET Pulse Width High	250		250		ns	
t9	RESET Inactive to first –XIOR or –XIOW Command	4		4		TCY	
tD10	Command Recovery Time Between Successive –XIOR or –XIOW Pulses	250		200		ns	

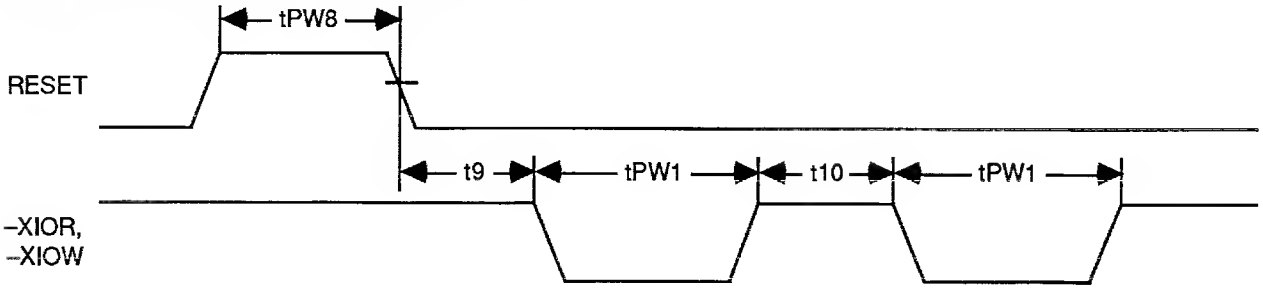
READ TIMING WAVEFORM



WRITE TIMING WAVEFORM



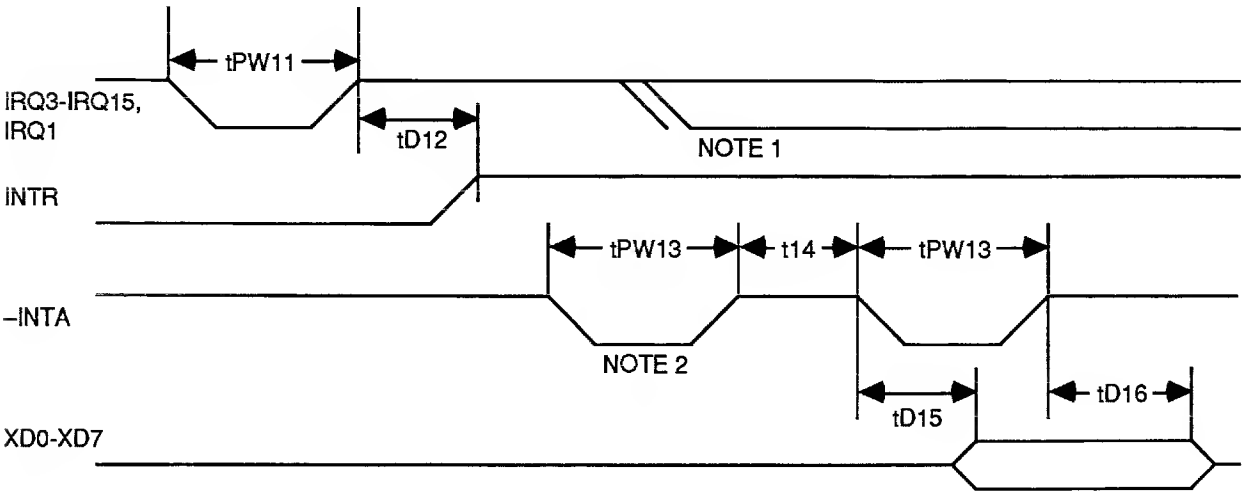
COMMAND AND RESET TIMING WAVEFORM



INTERRUPT MODE TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tPW11	Interrupt Request Pulse Width Low	90		90		ns	
tD12	Interrupt Output Delay	130		130		ns	
tPW13	–INTA Pulse Width Low	180		180		ns	
t14	End of –INTA Pulse to next –INTA Pulse	180		180		ns	
tD15	XD Data Valid Delay from –INTA Low		120		110	ns	
tD16	XD Data Float Delay from –INTA High	0	50	0	45	ns	

INTERRUPT TIMING WAVEFORM

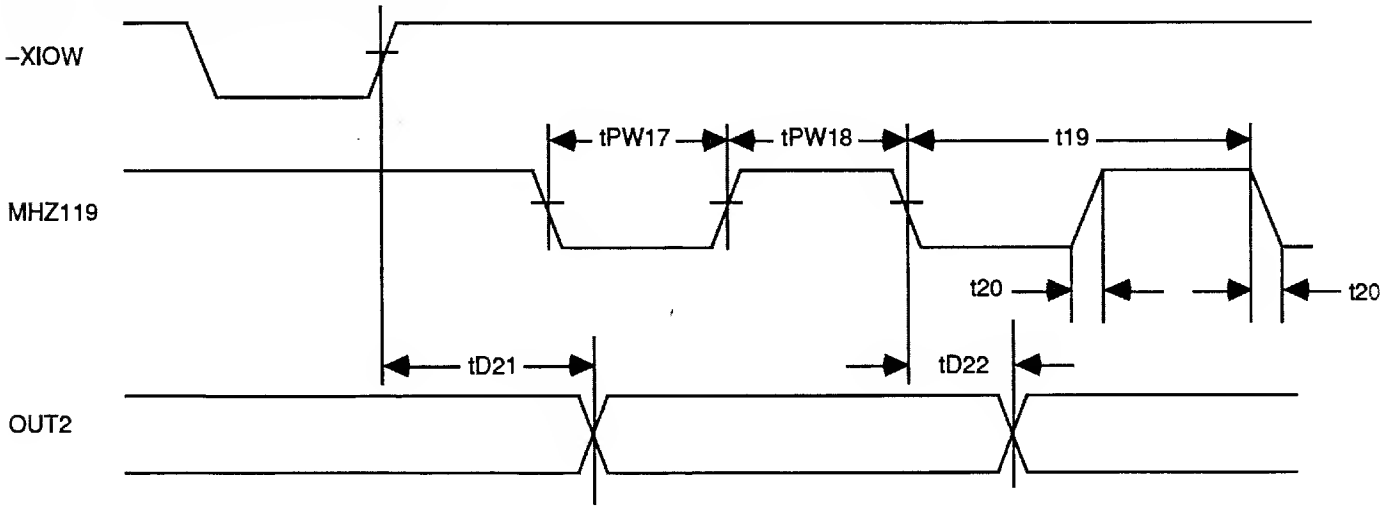


Notes: 1. IRQ must remain active until first –INTA pulse.
2. Cascade priority is resolved on this –INTA cycle.

TIMER/COUNTER TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tPW11	MHZ119 Clock Pulse Width High	55		55		ns	
tPW18	MHZ119 Clock Pulse Width Low	55		55		ns	
t19	MHZ119 Clock Cycle Time	180		180		ns	
t20	MHZ119 Clock Rise/Fall Time	20		20		ns	
tD21	OUT2 Valid from –XIOW High Delay Time when writing to Counter 2 Mode Register or TMGATE2 in Port B		100		100	ns	
tD22	OUT2 Valid from MHZ119 Low Delay Time		100		100	ns	

TIMER/COUNTER TIMING WAVEFORM



DMA MODE TIMING

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU23	DRQ to SYSCLK High Setup Time	0		0		ns	Note 1
tD24	CPUHRQ Valid from SYSCLK High Delay Time		70		70	ns	
tSU25	CPUHLDA to SYSCLK High Setup Time	25		25		ns	
tD26	–AEN1 Valid from SYSCLK High Delay Time		80		80	ns	
tD27	–DACK Valid from SYSCLK High Delay Time		100		100	ns	
tD28	XD Bus Valid from SYSCLK High Delay Time		110		110	ns	
tD30	A17-A23 Float from CPUHLDA High Delay Time	1	40	1	40	ns	
tD31	Upper Address Bits Valid from SYSCLK High Delay Time		130		115	ns	Note 2
tD32	A17-A23 Float from CPUHLDA Low Delay Time	1	25	1	25	ns	
tD33	Middle Address Bits Valid from SYSCLK High Delay Time		125		115	ns	Note 3
tD34	Lower Address Bits Valid from SYSCLK High Delay Time		90		90	ns	Note 4
tD35	XA Address Bus Float from SYSCLK High Delay Time	1	70	1	70	ns	8 Bit Cycles Only
tD36	–READ and –WRITE Active from SYSCLK High Delay Time		85		80	ns	
tD37	–READ and –WRITE Valid from SYSCLK High Delay Time		90		85	ns	
tD38	–READ and –WRITE Float from SYSCLK High Delay Time	1	70	1	70	ns	8 Bit Cycles Only
tD39	T/C Valid from SYSCLK High Delay Time		90		85	ns	8 Bit Cycles Only

Notes: 1. The DRQ signals are asynchronous inputs. Setup times are shown to assure recognition at a specific clock edge for testing.

2. Upper address bits are defined as A17-A23 for 16 bit DMA cycles, and A17-A23 plus XA16 for 8 bit DMA cycles.
3. Middle address bits are defined as XA9-XA16 for 16 bit DMA cycles and XA8-XA15 for 8 bit DMA cycles.
4. Lower address bits are defined as XA0-XA8 for 16 bit DMA cycles and XA0-XA7 for 8 bit DMA cycles.

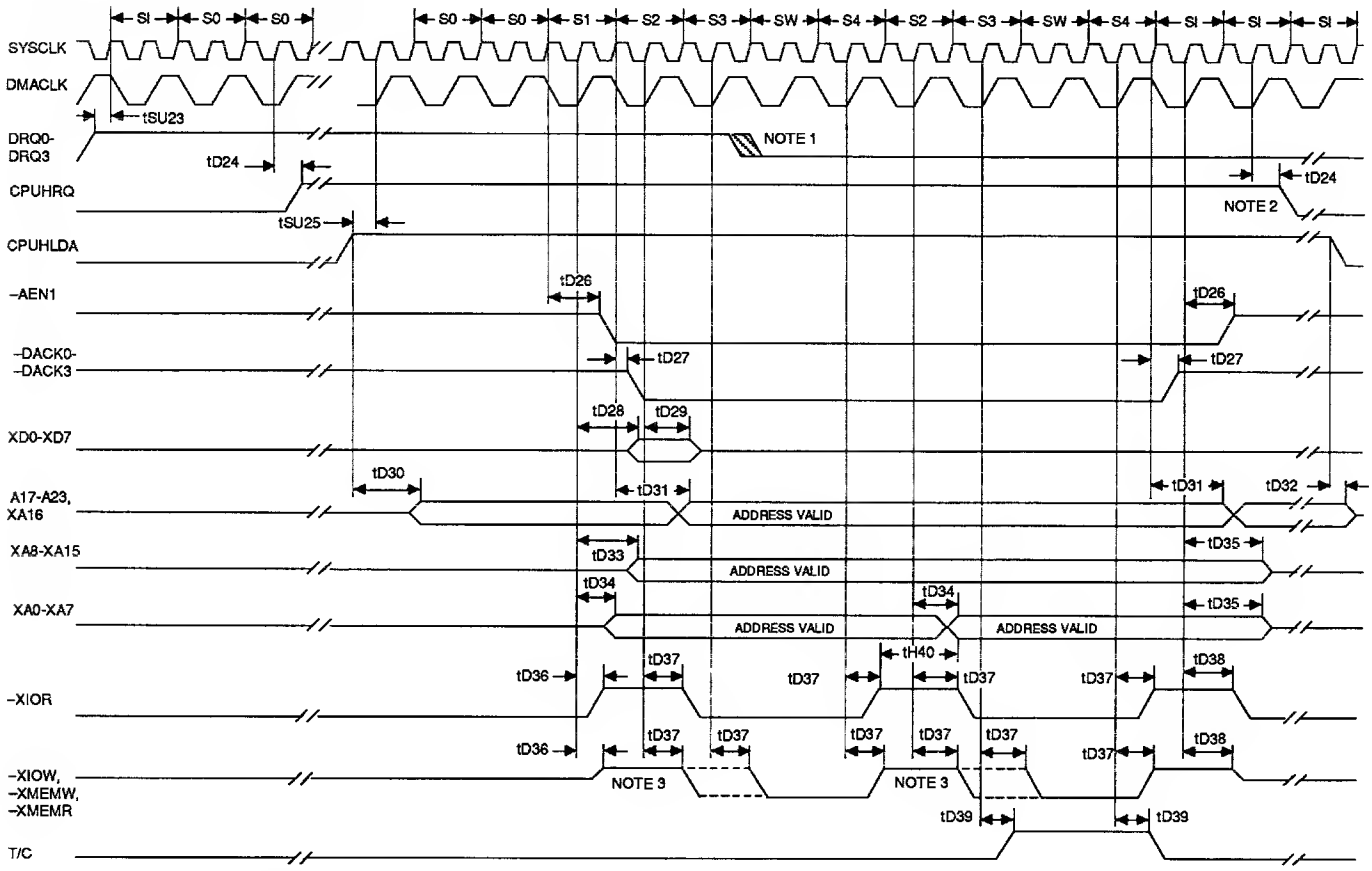
DMA MODE TIMING (Cont.)

Symbol	Parameter	12/16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tH40	XA Address from –READ or –WRITE High Hold Time	2 TCY –50		2 TCY –50		ns	TCY = SYSCLK Cycle Time
tD41	–AEN2 Low from SYSCLK High Delay Time		80		80	ns	
tD42	–AEN2 High From SYSCLK High		150		150	ns	
tD43	XA Address Bus Float from SYSCLK High Delay Time		140		140	ns	16 Bit DMA Cycles Only
tD44	–READ or –WRITE Float from SYSCLK High Delay Time		140		140	ns	16 Bit DMA Cycles Only
t45	–READ or –WRITE Float from –READ or –WRITE High at end of DMA Cycle	5		5		ns	16 Bit DMA Cycles Only
tSU46	IOCHRDY Valid to SYSCLK High Setup Time	25		20		ns	
tH47	IOCHRDY from SYSCLK High Hold Time	10		10		ns	
tD48	A17-A23 Float from –MASTER Low Delay Time	1	25	1	25	ns	
tD49	A17-A23 Float from –MASTER High Delay Time	1	40	1	40	ns	
tD50	–REFRESH Low from CPUHLDA High Delay Time		70		60	ns	
tD51	–REFRESH Inactive from SYSCLK High Delay Time		50		50	ns	Note 5
tSU52	–REFRESH Low to SYSCLK High Setup Time	25		25		ns	Note 6
tD53	A17-A23 Valid from –REFRESH Valid Delay Time		80		80	ns	
t54	SYSCLK Cycle Time	62		50		ns	
tPW55	SYSCLK Pulse Width Low	25		20		ns	
tPW56	SYSCLK Pulse Width High	25		20		ns	
t57	SYSCLK Rise/Fall Time	10		7		ns	

Notes: 5. –REFRESH is an open drain output. This specification is the time until the output is in an inactive state. Rise time of the external signal will depend on the external pull-up value and capacitive load.

6. When used as an input, –REFRESH is an asynchronous signal. Setup times are shown to assure recognition at a specific clock edge for testing.

8 BIT DMA TIMING WAVEFORM



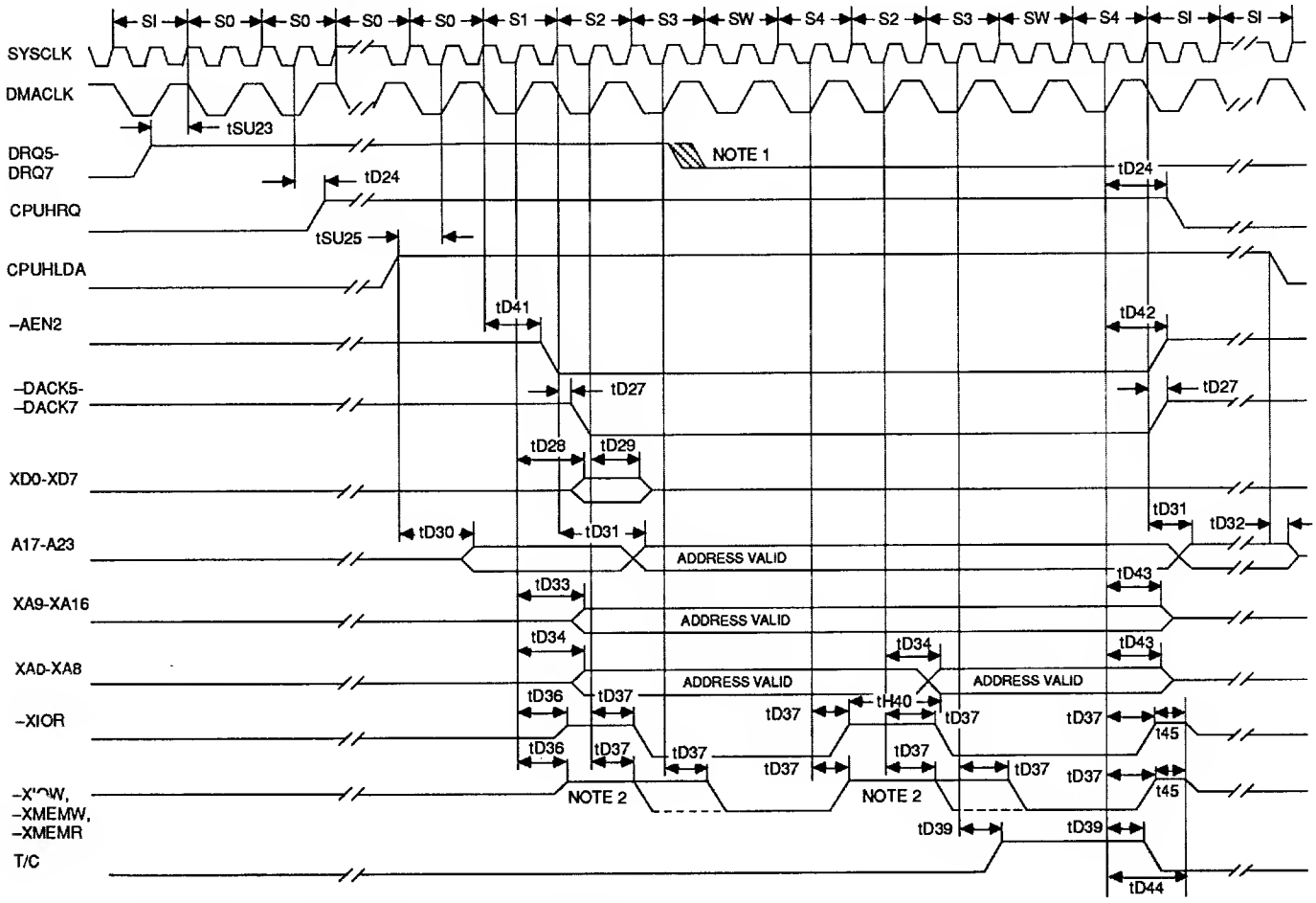
Notes: 1. DRQ should be held active until –DACK is returned.

2. The falling edge of CPUHRQ could occur one clock cycle earlier or later depending on how many bytes are transferred.

3. The first high to low transition shown here is for extended –XIOW and –XMEMW. The second high to low transition shown is for –XMEMR and late write on –XIOW and –XMEMW.

4

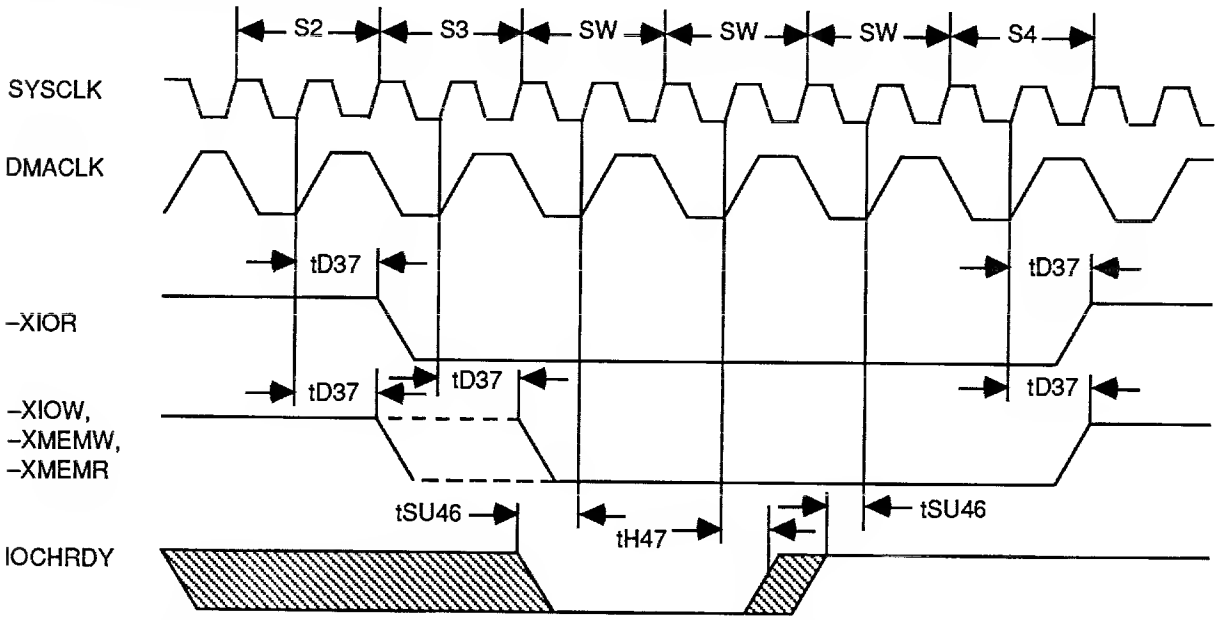
16 BIT DMA TIMING WAVEFORM



Notes: 1. DRQ should be held active until –DACK is returned.

2. The first high to low transition shown here is for extended –XIOW and –XMEMW. The second high to low transition shown is for –XMEMR and late write on –XIOW and –XMEMW.

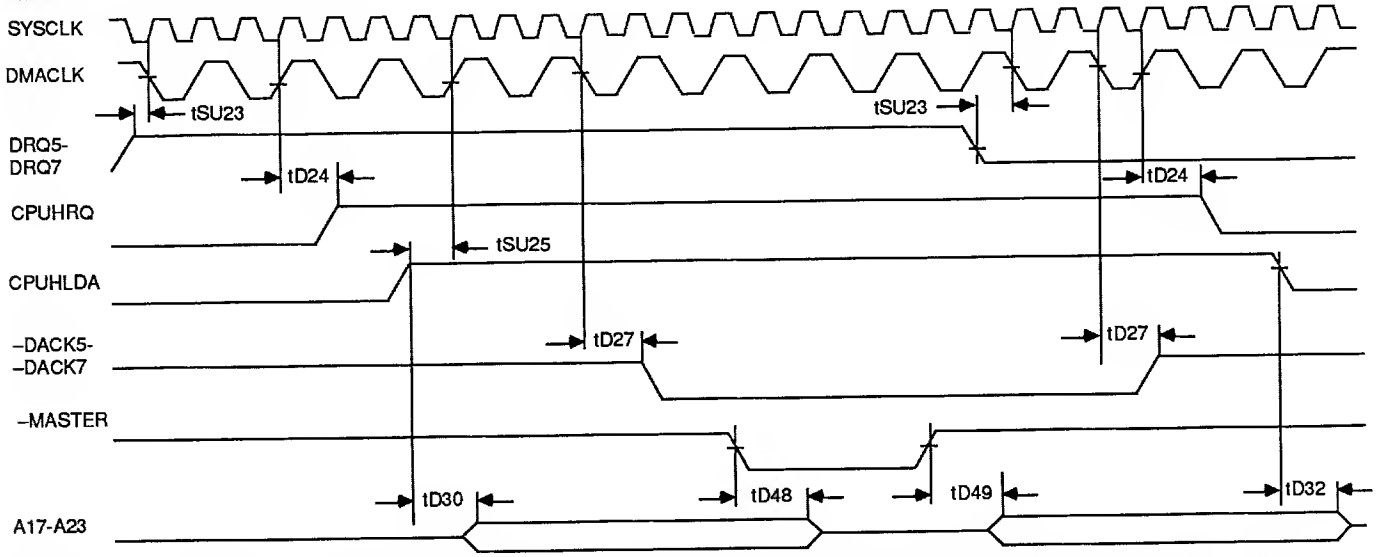
IOCHRDY TIMING WAVEFORM



Note: The first wait state is inserted by internal circuitry in the VL82C100 for all DMA cycles. Any additional wait states must be inserted using IOCHRDY.

4

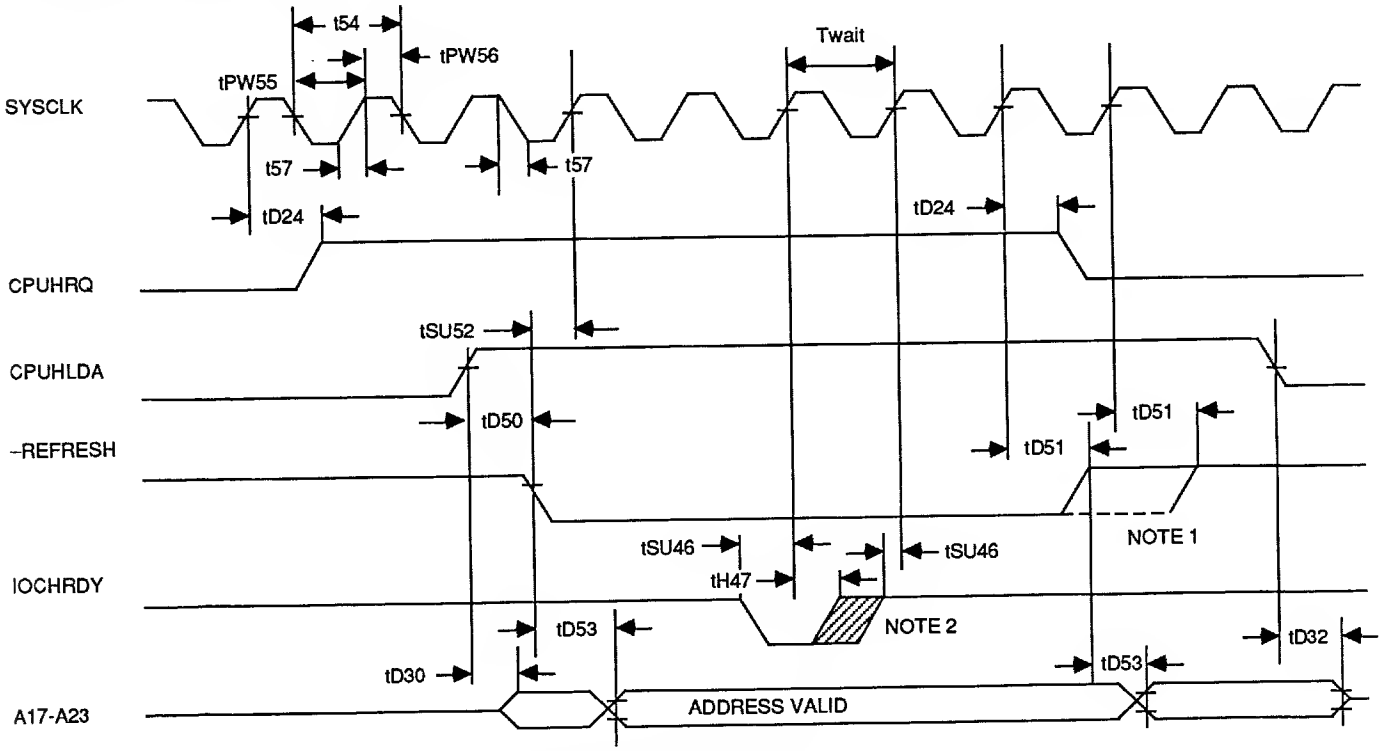
–MASTER TIMING WAVEFORM



Notes: 1. The DMA channel used for requesting control of the bus by a new bus master must be programmed in cascade mode. The new master should not pull –MASTER low until it has received the corresponding –DACK signal.

2. The timing shown is assuming one of the 16 bit DMA channels is used. There will be extra cycles between DRQ and CPUHRQ before and after the request cycle when using an 8 bit DMA channel. These extra cycles are caused by the cascade delay from the slave 8237 through the master 8237.

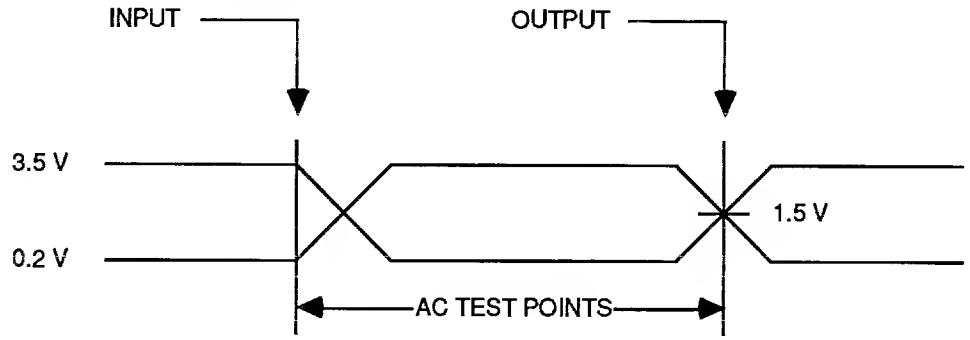
–REFRESH TIMING WAVEFORM



Notes: 1. A refresh pulse is normally three SYSCLK cycles long (with no wait states). Refresh pulses will be four SYSCLK cycles if a hold request is pending from the DMA controllers.

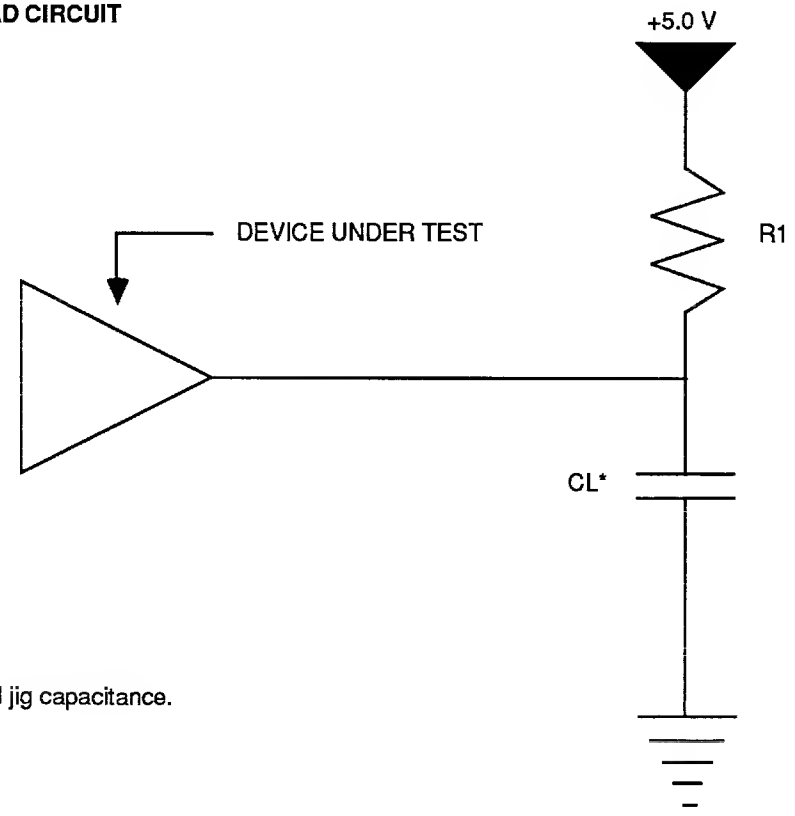
2. –REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC TESTING - INPUT, OUTPUT WAVEFORM



AC testing inputs are driven at 3.5 V for a logic 1 and 0.2 V for a logic 0. Clock inputs SYSCLK and MHZ119 are driven at 4.3 V and 0.2 V. Timing measurements are made at 1.5 V for both a logic 1 and 0.

AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)	R 1 (Ω)
–REFRESH	100	1K
All –DACKs, T/C	100	
All Other I/O and Output Pins	50	

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –400 µA
VOL1	Output Low Voltage		0.45	V	IOL = 20 mA, –REFRESH
VOL2	Output Low Voltage		0.45	V	IOL = 2 mA, All Other Pins
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL
VIL	Input Low Voltage	–0.5	0.8	V	TTL
VIHC	Input High Voltage	3.8	VDD + 0.5	V	RESET, SYSCLK, MHZ119
VILC	Input Low Voltage	–0.5	0.6	V	RESET, SYSCLK, MHZ119
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
IF	Input Leakage Current		–0.5	mA	VIN = 0.45 V, All IRQ & DRQ Inputs
ILI	Input Leakage Current	–10	10	µA	All Other Inputs
ICC	Power Supply Current		30	mA	Note

Note: VIN = VDD or GND, VDD = 5.25 V, outputs unloaded.

VL82C101B

PC/AT-COMPATIBLE SYSTEM CONTROLLER

FEATURES

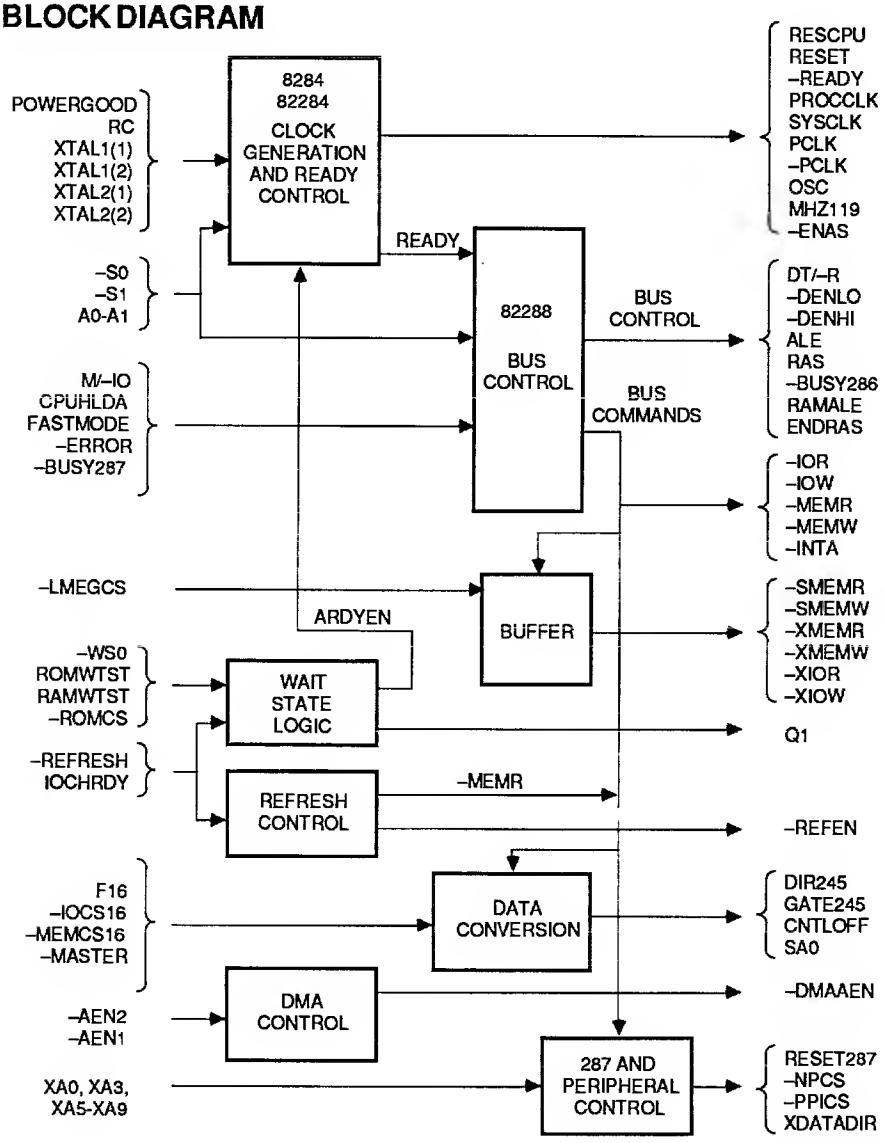
- Fully compatible with IBM PC/AT-type designs
- Replaces 36 integrated circuits on the PC/AT-type board
- Supports up to 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Sink 20 mA on slot driver outputs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C101B PC/AT-Compatible System Controller replaces an 82C284 Clock Controller and 82C288 Bus Controller (both are used in '286-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately 31 other less complex integrated circuits used as Wait State logic. When used in 12 MHz systems utilizing 80 ns DRAMs, the device provides the required one wait state for a "write" operation, and zero wait states for a "read" operation. A 12 MHz system using 120 ns DRAMs will be provided with one wait state for "write" and one wait state for "read". The device accepts both the 24 MHz crystal to control the system clock as well as the 14.318 MHz crystal to control the video clock. It also supplies reset and clock signals to the I/O slots.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C101B is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



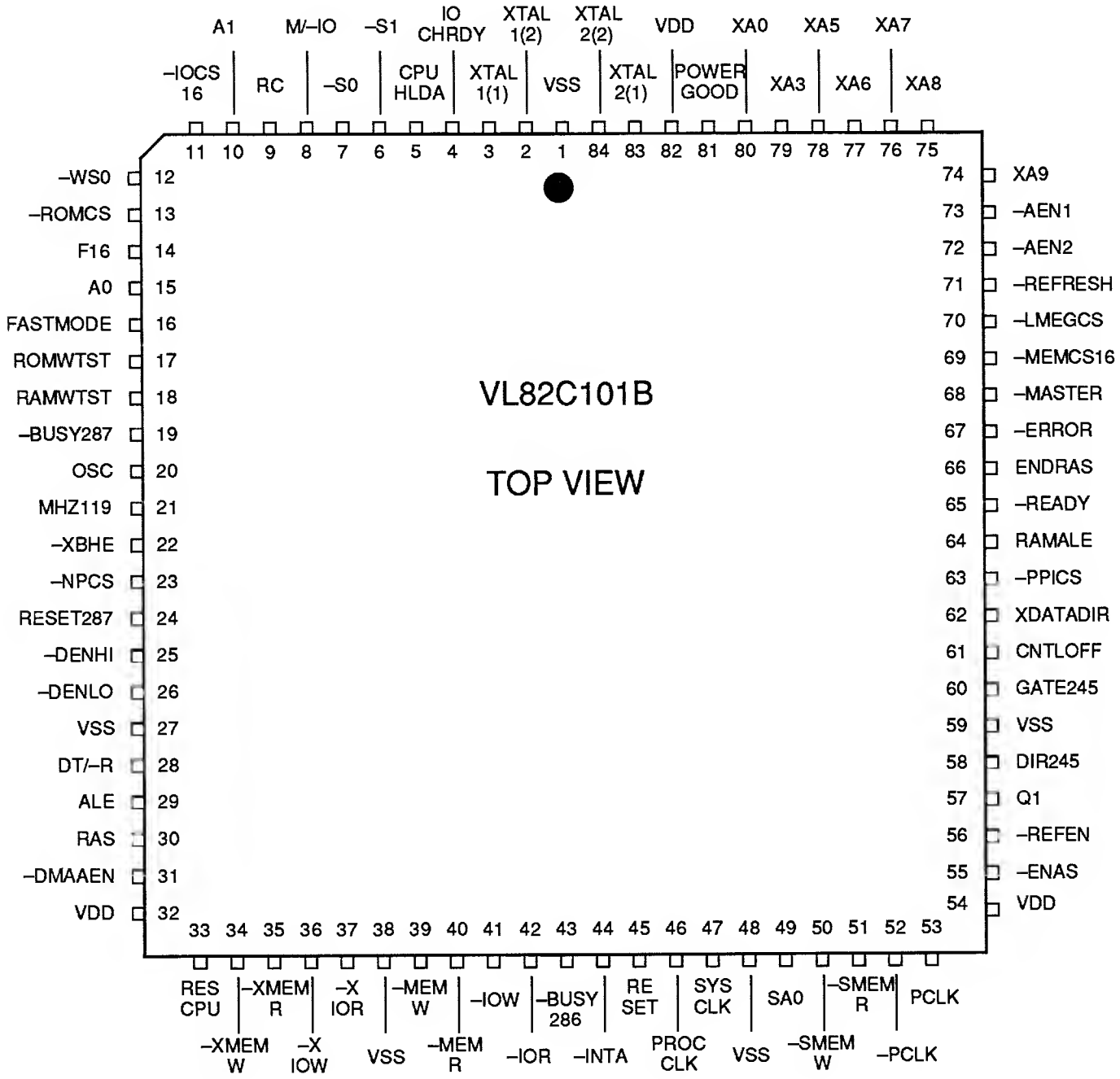
ORDER INFORMATION

Part Number	Package
VL82C101B-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

4

PIN DIAGRAM


A1
M/–IO
–S1
IO CHRDY
XTAL 1(2)
XTAL 2(2)
VDD
XA0
XA5
XA7
–IOCS 16
RC
–S0
CPU HLDA
XTAL 1(1)
VSS
XTAL 2(1)
POWER GOOD
XA3
XA6
XA8
11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75
–WS0 12
–ROMCS 13
F16 14
A0 15
FASTMODE 16
ROMWTST 17
RAMWTST 18
–BUSY287 19
OSC 20
MHZ119 21
–XBHE 22
–NPCS 23
RESET287 24
–DENHI 25
–DENLO 26
VSS 27
DT/–R 28
ALE 29
RAS 30
–DMAAEN 31
VDD 32
74 XA9
73 –AEN1
72 –AEN2
71 –REFRESH
70 –LMEGCS
69 –MEMCS16
68 –MASTER
67 –ERROR
66 ENDRAS
65 –READY
64 RAMALE
63 –PPICS
62 XDATADIR
61 CNTLOFF
60 GATE245
59 VSS
58 DIR245
57 Q1
56 –REFEN
55 –ENAS
54 VDD
33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
RES CPU
–XMEM R
–X IOR
–MEM W
–IOW
–BUSY 286
RE SET
SYS CLK
SA0
–SMEM R
PCLK
–XMEM W
–X IOW
VSS
–MEM R
–IOR
–INTA
PROC CLK
VSS
–SMEM W
–PCLK
VL82C101B
TOP VIEW

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
XTAL1(2)	2	O	Crystal 1 Output 2 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This is the crystal output.
XTAL1(1)	3	I	Crystal 1 Input 1 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This input drives the internal oscillator and determines the frequency of OSC.
IOCHRDY	4	I	I/O Channel Ready - This input is generated by an I/O device. When low, it indicates a not ready condition. This is used to extend memory or I/O accesses by inserting wait states. When high, this signal allows normal completion of a memory or I/O access by an I/O device.
CPUHLDA	5	I	CPU Hold Acknowledge - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
–S1	6	I	Status 1 - An active low input/pull-up from the CPU in combination with –S0 and M/–IO determine which type of bus cycle to initiate. –S1 going active indicates a read cycle unless –S0 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or halt/shutdown operation.
–S0	7	I	Status 0 - An active low input/pull-up from the CPU in combination with –S1 and M/–IO determine which type of bus cycle to initiate. –S0 going active indicates a write cycle unless –S1 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or a halt/shutdown operation.
M/–IO	8	I	Memory or I/O Select - This input indicates the type of bus cycle to be performed. If high, a memory cycle or halt/shutdown cycle is started. If low, then an I/O cycle or an interrupt acknowledge cycle will be initiated.
RC	9	I	This active low input signal will force a CPU reset when active. It is generated by the keyboard controller.
A1	10	I	CPU Address Bus Bit 1 - This input is used to determine when to initiate a shutdown operation. A shutdown will be started when A1 is low, M/–IO is high, and both –S0 and –S1 go low.
–IOCS16	11	I	I/O Chip Select 16 - This active low input is generated by an I/O device for a 16-bit data bus access.
–WS0	12	I	Wait State 0 - This active low input signal should have an external pull-up. A peripheral device can pull this signal low to force a zero wait state cycle.
–ROMCS	13	I	ROM Chip Select - This active low input is a signal generated from –LCS0ROM and –LCS1ROM and is used to indicate a ROM memory access.
F16	14	I	This input indicates a word memory access. It is used to inhibit command delays during a 16 bit memory access.
A0	15	I	CPU Address Bus Bit 0 - This input is used to generate enable signals for the data bus transceivers.
FASTMODE	16	I	This active high input enables the generation of an early ALE signal, called RAMALE, from the edge of –MEMR or –MEMW. If FASTMODE is desired, this pin must be held low until after the first memory read cycle. RAMALE is equal to ALE when FASTMODE is inactive.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
ROMWTST	17	I	ROM Wait State - This input is used to select the desired number of ROM access wait states. ROMWTST = 0 indicates two waits while RAMWTST = 1 indicates one wait state. If two wait state mode is required, this pin must be set high when CPUHLDA (pin 5) is high.
RAMWTST	18	I	RAM Wait State - This input is used to select the desired number of RAM access wait states. RAMWTST = 0 indicates zero waits while RAMWTST = 1 indicates one wait state.
–BUSY287	19	I	Busy 287 - A busy status input that is asserted by the 80287 to indicate that it is currently executing a command.
OSC	20	O	This is the buffered output of XTAL1 oscillator.
MHZ119	21	O	This output is the OSC output clock divided by 12. It is used by the Peripheral Controller device for the timer controller.
–XBHE	22	I/O	Transfer Byte High Enable - This active low I/O is used to allow the upper data byte of be passed through the data bus transceivers.
–NPCS	23	O	Numerical Processor Chip Select - This active low output is the chip select for the 80287 numerical processor.
RESET287	24	O	Reset 287 - This active high output is used to reset the 80287 numerical processor.
–DENHI	25	O	Data Bus Enable High - This active low output is used to enable the data bus transceiver on the high byte of the data bus.
–DENLO	26	O	Data Bus Enable Low - This active low output is used to enable the data bus latch byte accesses.
DT/–R	28	O	Data Transmit/Receive - An output that determines the data direction to and from the local data bus. A high indicates a write bus cycle and a low indicates a read bus cycle. DT/–R is high when no bus cycle is active. –DENLO and –DENHI are always inactive when DT/–R changes state.
ALE	29	O	Address Latch Enable - A positive edge output that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
RAS	30	O	This output will go active anytime a memory read or memory write command is issued.
–DMAAEN	31	O	DMA Address Enable - An active low output that is active whenever an I/O device is making a DMA access to the system memory.
RESCPU	33	O	Reset CPU - This is the active high output system reset for the CPU. It is generated from POWERGOOD, RC or when a shut down status is generated by the CPU.
–XMEMW	34	I/O	Peripheral Bus Memory Write - An active low I/O that is the memory write command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–XMEMR	35	I/O	Peripheral Bus Memory Read - An active low I/O that is the memory read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–XIOW	36	I/O	Peripheral Bus Input/Output Write - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–XIOR	37	I/O	Peripheral Bus Input/Output Read - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–MEMW	39	I/O	Memory Write - This active low I/O is the memory write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–MEMR	40	I/O	Memory Read - This active low I/O is the memory read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. –MEMR is also active during a refresh cycle.
–IOW	41	I/O	Input/Output Write - This is the active low I/O write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–IOR	42	I/O	Input/Output Read - This is the active low I/O read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–BUSY286	43	O	Processor 286 Extension Busy - This output goes to the –BUSY input of the 80286. If pulled low, this signal stops the 80286 program execution on all WAIT and some ESC instructions until it returns inactive (high).
–INTA	44	O	Interrupt Acknowledge - This active low output that is three-stated, is the interrupt acknowledge command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
RESET	45	O	Reset - This active high output signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK.
PROCCLK	46	O	Processor Clock - This output is the processor clock for the CPU and coprocessor. It is equal to the crystal frequency on crystal oscillator input XTAL2.
SYSCLK	47	O	System Clock - This output is the main system clock. It is equal to half the PROCCLK frequency and is synchronized to the processor's T-states.
SA0	49	O	System Address Bus Bit 0 - A three-stated output.
–SMEMW	50	O	Memory Write - An active low three-stated output that is the memory write command to the expansion bus. Drives when –LMEGCS is low.
–SMEMR	51	O	Memory Read - An active low three-stated output that is the memory read command to the expansion bus.
–PCLK	52	O	Peripheral Clock Complement Phase - This output is the complement phase of the peripheral clock. It is equal to half the PROCCLK frequency and is used for clocking peripheral devices.
PCLK	53	O	Peripheral Clock True Phase - This output is the true phase of the peripheral clock. It is equal to half the PROCCLK frequency and is used for clocking peripheral devices.
–ENAS	55	O	Enable Address Strobe - This active low output is used to enable the address strobe on the real time clock. It will go low the first time –S0 is asserted after a system reset.
–REFEN	56	O	Refresh Enable - An active low output. It will be asserted when a refresh cycle is needed for the DRAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
Q1	57	O	This active high output will go active during the second phase of a CPU bus cycle following the T-state. It is used by other devices to generate the address strobe for the real time clock.
DIR245	58	O	Direction 245 - This output determines the direction of the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals.
GATE245	60	O	Gate 245 - This output enables the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals.
CNTLOFF	61	O	Control Off - This output is used to enable the lower byte data bus latch during byte accesses.
XDATADIR	62	O	Transfer Data Direction - This output controls the direction of data flow through the transceiver between the X data bus and the lower byte of the S data bus. A high indicates data flow from the S bus to the X bus. A low indicates data flow from the X bus to the S bus.
–PPICS	63	O	Programmable Peripheral Interface Chip Select - This active low output is used to generate the chip select for the keyboard controller.
RAMALE	64	O	RAM Address Latch Enable - This output is used in the FASTMODE of operation. When FASTMODE is inactive RAMALE is equal to ALE.
–READY	65	O	Ready - When active, indicates that the current bus cycle is to be completed. –READY is an open drain output requiring an external pull-up resistor.
ENDRAS	66	O	An output that is used to complete a memory read/write cycle.
–ERROR	67	I	Error - An error status input from the 80287. This reflects the ES bit of the 80287 status word and indicates that an unmashed error condition exists.
–MASTER	68	I	Master - This active low input is asserted low by devices on the expansion bus. A low indicates that another device is active.
–MEMCS16	69	I	Memory Chip Select 16 - A low on this pin indicates that the off-board memory is 16-bits wide.
–LMEGCS	70	I	Lower Megabyte Chip Select - This input indicates that the lower memory address space (0-1 megabyte) is selected. When low, it enables the three-state drivers on –SMEMR and –SMEMW.
–REFRESH	71	I	Refresh - This active low input is used to initiate a refresh cycle for the dynamic RAMs.
–AEN2	72	I	Address Enable 2 - This active low input is from the DMA controllers and is used to enable the address latches for 16 bit data transfers.
–AEN1	73	I	Address Enable 1- This active low input is from the DMA controllers and is used to enable the address latches for 8 bit data transfers.
XA5-XA9	78-74	I	Peripheral Address Bus Bits 5-9 - These inputs are used to decode chip select and reset signals for the coprocessor.
XA3	79	I	Peripheral Address Bus Bit 3 - This input is used in control of the coprocessor reset and chip select signals.
XA0	80	I	Peripheral Address bus bit 0 - This input is used in control of the coprocessor and 8/16-bit data conversions.
POWERGOOD	81	I	System Power-on Reset - This input signal indicates that power to the board is stable. A Schmitt-trigger input is used so the input can be connected directly to an RC network.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
XTAL2(1)	83	I	Crystal 2 Input 1- A parallel resonant fundamental mode crystal should be attached across XTAL2(1) and XTAL2(2). This input drives the internal oscillator and determines the frequency for PROCCLK.
XTAL2(2)	84	O	Crystal 2 Output 2 - A parallel resonant fundamental mode crystal should be attached across XTAL2(1) and XTAL2(2). This is the crystal output.
VDD	32, 54, 82		System Power: 5 V
VSS	1, 27, 38, 48, 59		System Ground

FUNCTIONAL DESCRIPTION

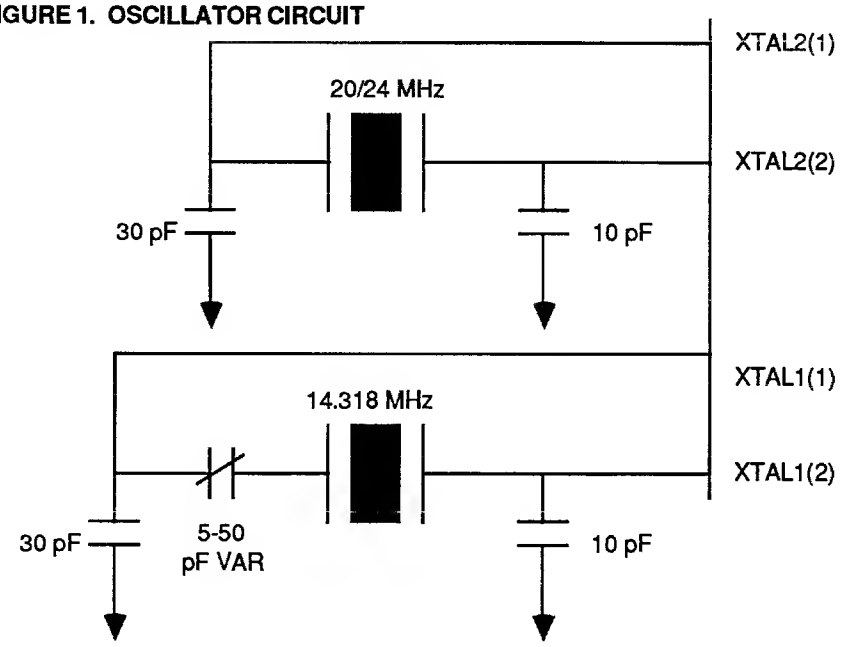
The VL82C101B chip generates all the major clocks for an AT-compatible system design along with the command and control signals for both the system and peripheral buses. It interfaces with the CPU to determine the type of bus cycle to execute and generates the –READY signal to indicate that the current bus cycle can be terminated. It also contains logic to make conversions between 16 bit and 8 bit data accesses. Finally, it generates some of the control signals necessary for the 80287 Numerical Processor.

CLOCK GENERATION

The VL82C101B contains two oscillators to generate the clocks for an AT-compatible design. Both oscillators are designed to use an external, parallel resonant fundamental mode crystal. The first oscillator is used to generate the video clock output (OSC) and MHZ119 which is the clock for the 8254 timer in the Peripheral Controller device. A 14.318 MHz crystal should be used on this oscillator to maintain compatibility. The OSC output is generated directly from this oscillator for the system bus and the MHZ119 output is derived from the OSC output divided by 12. To guarantee sufficient drive and a clean signal on the slots it is recommended that the OSC output be buffered before driving the expansion connectors.

The second oscillator is used to generate the system clocks. The crystal frequency for this oscillator should be twice the operating frequency of the CPU. For a 12 MHz system, a 24 MHz oscillator should be used. This oscillator is used to generate four clock outputs. PROCCLK is generated directly from the oscillator and will have the same frequency as the crystal input. This output is connected directly to the CPU and Numerical Processors clock inputs. PCLK and –PCLK are used to clock the keyboard controller. These outputs are free running clock signals with a frequency of half the PROCCLK frequency. The last clock output is SYSCLK. This clock is also at half the PROCCLK frequency, but it will be held low during RESET and will not begin running until the first bus cycle is initiated by the CPU. It will then make its first low to high transition on the falling edge of PROCCLK during the start of the first TC cycle (see timing waveforms). This synchronization is done to ensure that the system clock is synchronized with the 80286 internal system clock. The SYSCLK output is used to drive the Peripheral Controller device directly and should be buffered externally before driving the expansion connectors to guarantee sufficient drive and a clean signal on the slots.

FIGURE 1. OSCILLATOR CIRCUIT



RESET AND READY CONTROL

The 82284 megacell along with some support logic is used to control the system reset signals and –READY signal for the CPU. Two basic reset signals are generated for the system. RESET is the system reset out of the 82284 megacell and is synchronized to

PROCCLK. It is generated from the POWERGOOD input signal. RESCPU, the other reset output, is connected to the input on the 80286 processor. RESCPU will be active anytime RESET is active. It can also be generated from two other possible sources. The first is the RC input from the keyboard controller. RESCPU will go active within 4 to 18 PROCCLK cycles after RC is asserted and will go inactive 16 PROCCLK cycles later or 16 PROCCLK cycles after RC is negated. RESCPU will also be generated if a shutdown command cycle is decoded from the CPU. As with the RC input, RESPCU will go active within 4 to 18 PROCCLK cycles of detecting the shutdown command and will be negated 16 PROCCLK cycles later. The POWERGOOD pin has a Schmitt-trigger input so that an RC network can be used to generate the reset signals.

The –READY output is synchronized and controlled by the 82284 megacell. –READY is an open drain output connected directly to the CPU and requires an external pull-up resistor. A resistor value of 700 Ω is recommended for 10 or 12 MHz operation. Bus cycle length is controlled by the –READY output. Bus cycles are lengthened and shortened internally by the VL82C101B depending on the type of bus cycle being executed. The length of a bus cycle can be shortened externally by pulling the –WS0 input low or lengthened by pulling the IOCHRDY input low. If IOCHRDY is pulled low the bus cycle will not be terminated until IOCHRDY is returned high.

COMMAND AND BUS CONTROL

The VL82C101B contains an 82288 bus controller megacell to generate all the bus command and control signals. The 82288 megacell generates the –MEMR, –MEMW, –IOR and –IOW command signals and the DT/–R control signal. The DEN output from the megacell is split into –DENLO and –DENHI for enables on the upper and lower bytes of the data bus. Internal circuitry is used to insert one PROCCLK cycle of command delay for all I/O cycles and off-board 8 bit memory cycles. Refer to the 82288 data sheet for complete operation of the 82288 megacell.

OPERATING MODES

The VL82C101B operates in four basic modes. First, and most common, is the CPU mode. This mode is active any time the input CPUHLDA is low. While in CPU mode the VL82C101B will drive both the CMD (–MEMR, –MEMW, –IOR, –IOW) bus and XCMD (–XMEMR, –XMEMW, –XIOR, –XIOW) bus.

The other modes can only be active when CPUHLDA is high. Then the VL82C101B can be in DMA mode, –MASTER mode, or –REFRESH mode. If the inputs –AEN1 or –AEN2 are active, the VL82C101B is in DMA mode and the CMD bus is driven from the inputs on the XCMD bus. If the –MASTER input is active, the VL82C101B is in –MASTER mode and the XCMD bus is driven from the inputs on the CMD bus. When the –REFRESH mode is active the –MEMR output will be driven to generate the refresh for the DRAMs but –MEMW, –IOR and –IOW will be in a high impedance state. The XCMD pins will be configured as outputs driving whatever value is on the CMD pins.

SYSTEM BOARD MEMORY CONTROL

Memory control on the system board is accomplished with three signals, RAMALE, RAS, and ENDRAS.

The system board memory controls can operate in two different modes. While in CPU mode with the FASTMODE input set low or in non-CPU mode, RAMALE will look the same as ALE and RAS will be generated from –MEMR and –MEMW. In this mode the memory timing will look the same as an AT-compatible design. If the FASTMODE input is set high, the RAMALE and RAS signals are changed during CPU mode accesses to allow for more DRAM access time.

RAMALE is used by both the Memory Controller and Address Buffer devices to latch in current address values to generate both address and enable signals for the DRAMs. In FASTMODE the RAMALE signal is changed so that it will only go low when a memory read or write command is active. This guarantees that the memory address and chip select signals will remain valid during the entire memory cycle and allows RAMALE to return high as soon as possible to transmit through the new address for the next cycle.

The RAS output is changed in FASTMODE so that it will go active one PROCCLK cycle sooner during a memory read cycle to allow more read access time. The RAS output will look the same as non-FASTMODE timing for write cycles. This was done to allow for zero wait state cycles on memory reads. RAS could not be moved up on memory writes because the data from the CPU would not be valid in time to be written into the DRAMs.

ENDRAS is used to terminate the RAS signals to the DRAMs without terminating the memory access. This allows for the required RAS precharge time before the next memory access. It will normally be high and make a high to low transition to terminate the RAS signals to the DRAMs on the third PROCCLK after RAS goes active. ENDRAS will then remain low until RAS returns low, which will cause ENDRAS to return high. The exception to this timing is for a zero wait state RAM read. In this case, ENDRAS will make the high to low transition two PROCCLK cycles after RAS instead of three.

WAIT STATE LOGIC

Wait states can be controlled from a number of different sources within the VL82C101B. It is internally programmed to generate the wait states shown in Table 1 based on the appropriate input signals.

Any of these programmed values can be overridden by the inputs IOCHRDY and –WS0. IOCHRDY can be used to extend any bus cycle. When IOCHRDY is pulled low the current bus cycle will be maintained until it is returned high. A low on –WS0 will terminate the current bus cycle as soon as it is recognized by the VL82C101B. These inputs need only be pulled low to modify the values shown in Table 1. IOCHRDY and –WS0 are mutually exclusive and only one of them should

be pulled low within a given bus cycle. Refer to the timing diagrams for setup and hold requirements.

REFRESH CONTROL

The VL82C101B contains circuitry to control a refresh cycle in an AT-compatible design. When the input –REFRESH is pulled low the VL82C101B will issue –REFEN to clock the refresh counter and enable the refresh addresses onto the memory address bus. It will also issue a –MEMR command. For correct operation –REFRESH should not be pulled low unless CPUHLDA is active.

DATA CONVERSION

A state machine for controlling the conversion between 16 bit data accesses from the CPU and 8 bit peripherals is contained in the VL82C101B. This state machine will generate the control signals DIR245, GATE245, and CNTLOFF to the Data Buffer chip to route the data correctly for both read and write conversions. The conversion logic will signal the wait state logic to hold the CPU and start the read/write of the low data byte. It will then latch the low byte for a read operation, negate the bus control signals, switch SA0 to a high, and then perform the read/write operation for the high data byte. The VL82C101B also uses the DIR245 and GATE245 during 8-bit DMA cycles to route the lower byte on the system data bus to or from the high or low byte of on-board memory.

NUMERICAL PROCESSOR AND PERIPHERAL CONTROL

The VL82C101B generates a RESET signal and chip select signal for the 80287 Numerical Processor. The signal RESET287 is used to reset the 80287 and can be activated by a system reset or an I/O write to address 0F1 hex. –NPCS is used as a chip select for the 80287 and is decoded at addresses 0F8-0FF hex.

The VL82C101B also controls the –BUSY286 signal sent to the 80286 from the Numerical Processor. The 80287 will assert –BUSY287 whenever it is performing a task. This signal is passed to the 80286 by asserting the –BUSY286 output. Normally –BUSY286 will follow –BUSY287. However, if the –ERROR signal is asserted while the –BUSY287 signal is active, the –BUSY286 output will be latched low and will remain active until cleared by an I/O write cycle to address 0F0 hex or 0F1 hex.

4

TABLE 1. WAIT STATES

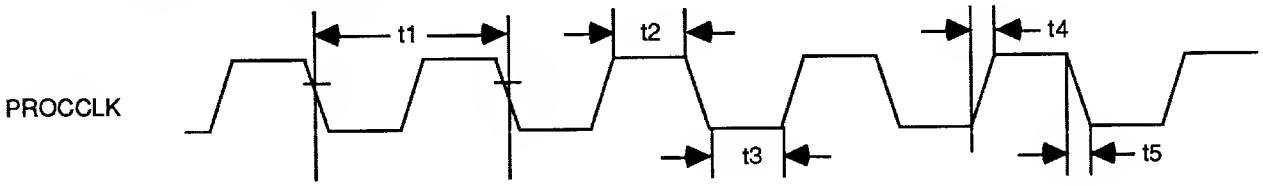
Access Type	RAMWTST	ROMWTST	F16	–MEMCS16	–IOCS16	Number of Waits
INTA Cycles	X	X	X	X	X	4
8 Bit I/O	X	X	X	X	1	4
16 Bit I/O	X	X	X	X	0	1
Off-board 8-Bit Memory	X	X	0	1	X	4
Off-board 16-Bit Memory	X	X	0	0	X	1
On-board ROM Read	X	1	1	X	X	1
On-board ROM Read	X	0	1	X	X	2
On-board RAM Write	X	X	1	X	X	1
On-board RAM Read	1	X	1	X	X	1
On-board RAM Read	0	X	1	X	X	0

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

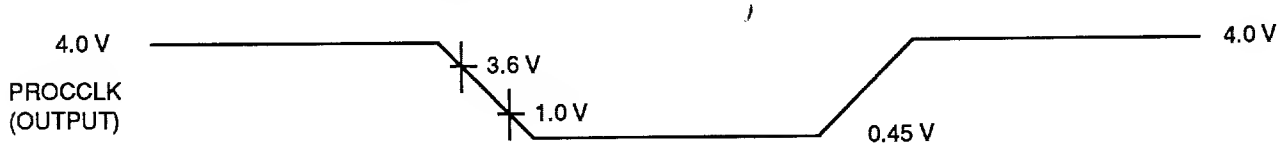
PROCCLK MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t1	PROCCLK Period	42	250	ns	24 MHz Crystal Oscillator
t2	PROCCLK High Time	14	239	ns	
t3	PROCCLK Low Time	12	237	ns	
t4	PROCCLK Rise Time		8	ns	1.0 V to 3.6 V, CL = 150 pF
t5	PROCCLK Fall Time		8	ns	3.6 V to 1.0 V, CL = 150 pF

PROCCLK TIMING WAVEFORMS



AC measurement characteristics from PROCCLK going low:



The PROCCLK (from '284 Megacell) is the main reference point for most of the AC signals. PROCCLK has a guaranteed VOH of 4.0 V and a VOL of 0.45 V. However, all AC measurements referenced to PROCCLK going low are from the 1.0 V point. At 24 MHz the transition time from 3.6 V to 1.0 V (and 1.0 V to 3.6 V) is guaranteed to be 8 ns or less.

CPU MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tSU6	POWERGOOD to PROCCLK Setup Time	20		ns	Note 1
tH7	POWERGOOD from PROCCLK Hold Time	10		ns	Note 1
tD8	RESET from PROCCLK Delay		25	ns	
tD9	SYSCLK, PCLK, –PCLK from PROCCLK Delay		25	ns	
tD10	RESCPU from PROCCLK Delay		24	ns	
tSU11	M/–IO, A1 to –S0, –S1 Setup Time	22		ns	
t12	OSC Rise/Fall Time		8	ns	CL = 100 pF
t13	MHZ119 Rise/Fall Time		8	ns	CL = 100 pF
tD14	MHZ119 from OSC Delay		20	ns	
tSU15	–S0, –S1 to PROCCLK Setup Time	24		ns	
tH16	–S0, –S1 from PROCCLK Hold Time	3		ns	
tD17	ALE Valid from PROCCLK Delay		19	ns	
tD18	DT/–R Low from PROCCLK Delay		28	ns	
tD19	DT/–R High from PROCCLK Delay		45	ns	
tD20	DT/–R High from –DENHI, –DENLO High Delay	3		ns	
tD21	–DENLO, –DENHI Active from PROCCLK Delay		35	ns	
tD22	–DENLO, –DENHI Inactive from PROCCLK Delay		35	ns	
tD23	–READY Active from PROCCLK Delay		20	ns	
tD24	–READY Inactive from PROCCLK Delay	3		ns	Note 2
tD25	–IOR, –XIOR Valid from PROCCLK Delay		40	ns	
tD26	–IOW, –XIOW Valid from PROCCLK Delay		40	ns	
tD27	XDATADIR Valid from PROCCLK Delay		40	ns	
tSU28	–IOCS16 PROCCLK Setup Time	30		ns	
tH29	–IOCS16 PROCCLK Hold Time	10		ns	
tSU30	IOCHRDY to PROCCLK Setup Time	25		ns	
tD31	–ENAS Valid from PROCCLK Delay		30	ns	
tD32	RAMALE Valid from PROCCLK Delay		24	ns	

Notes: 1. POWERGOOD is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific PROCCLK edge.

2. –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLK cycles. We recommend 700 Ω for the pull-up resistor for 10 MHz and 12 MHz systems.

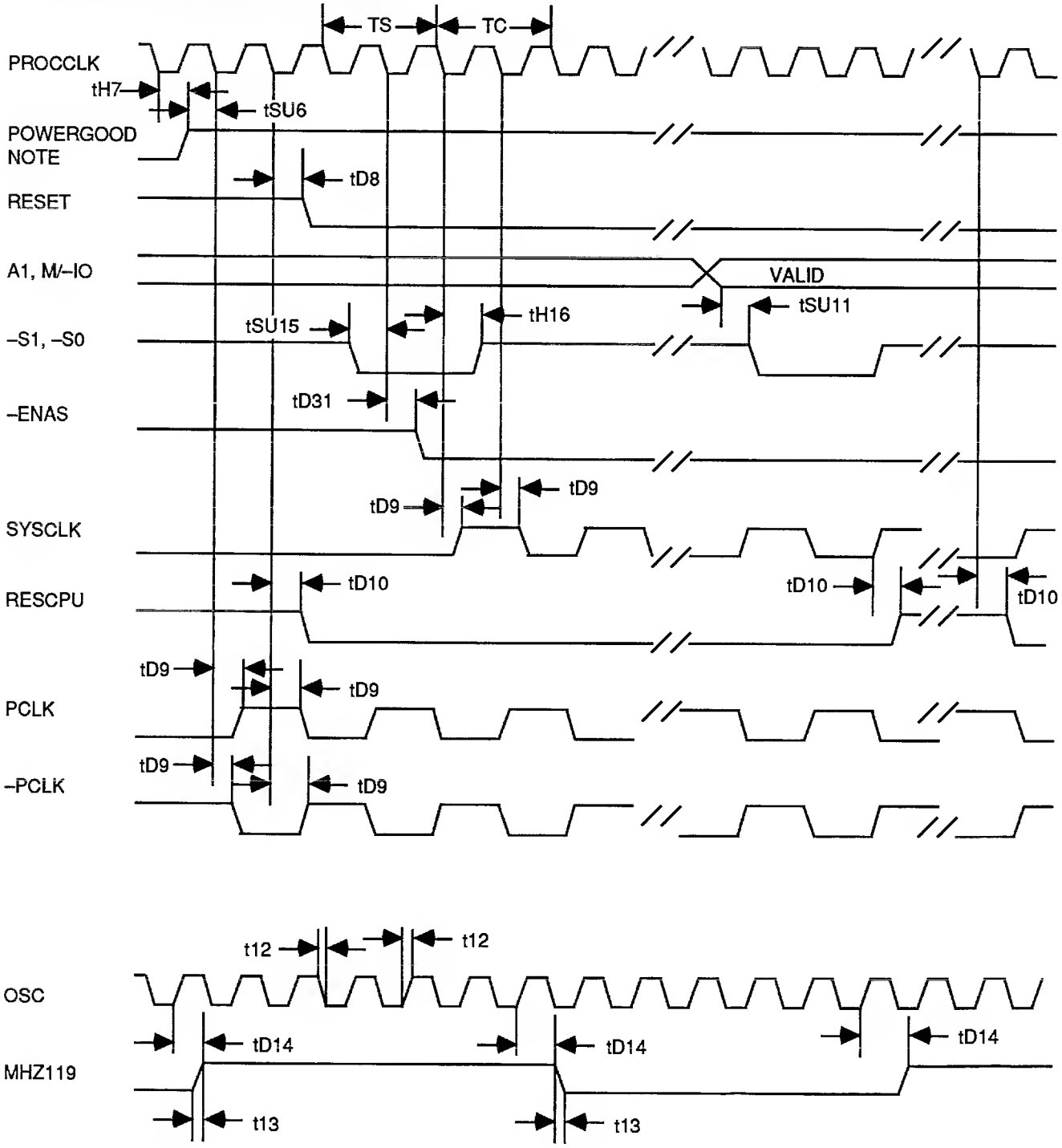
CPU MODE TIMING (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
tD33	RAS High from PROCCLK Delay		18	ns	Note 3
tD34	RAS High from PROCCLK Delay		15	ns	FASTMODE = 1, MEM Read Only
tD35	RAS Low from PROCCLK Delay		28	ns	
tD36	ENDRAS Low from PROCCLK Delay		25	ns	
tD37	ENDRAS High from PROCCLK Low Delay		55	ns	
tD38	ENDRAS High from RAS Low Delay	3		ns	
tD39	–MEMR, –XMEMR, –SMEMR Valid from PROCCLK Delay		40	ns	
tD40	–MEMW, –XMEMW, –SMEMW Valid from PROCCLK Delay		40	ns	
tSU41	–WS0 to PROCCLK Setup Time	22		ns	
tH42	–WS0 from PROCCLK Hold Time	1		ns	
tSU43	F16 to PROCCLK Setup Time	30		ns	
tH44	F16 from PROCCLK Hold Time	10		ns	
tSU45	–MEMCS16 to PROCCLK Setup Time	32		ns	
tH46	–MEMCS16 from PROCCLK Hold Time	5		ns	
tSU47	A0 to PROCCLK Setup Time	30		ns	
tD48	SA0 from PROCCLK Delay Time		35	ns	
tSU49	–XBHE to PROCCLK Setup Time	30		ns	
tD50	Q1 from PROCCLK Delay Time		35	ns	
tD51	CNTLOFF from PROCCLK Delay Time		25	ns	Note 4
tD52	DIR245 from PROCCLK Delay Time		45	ns	
tD53	GATE245 from PROCCLK Delay Time		55	ns	
tD54	–INTA Valid from PROCCLK Delay Time		42	ns	

Notes: 3. FASTMODE = 1, MEM write only. FASTMODE = 0, MEM read only.

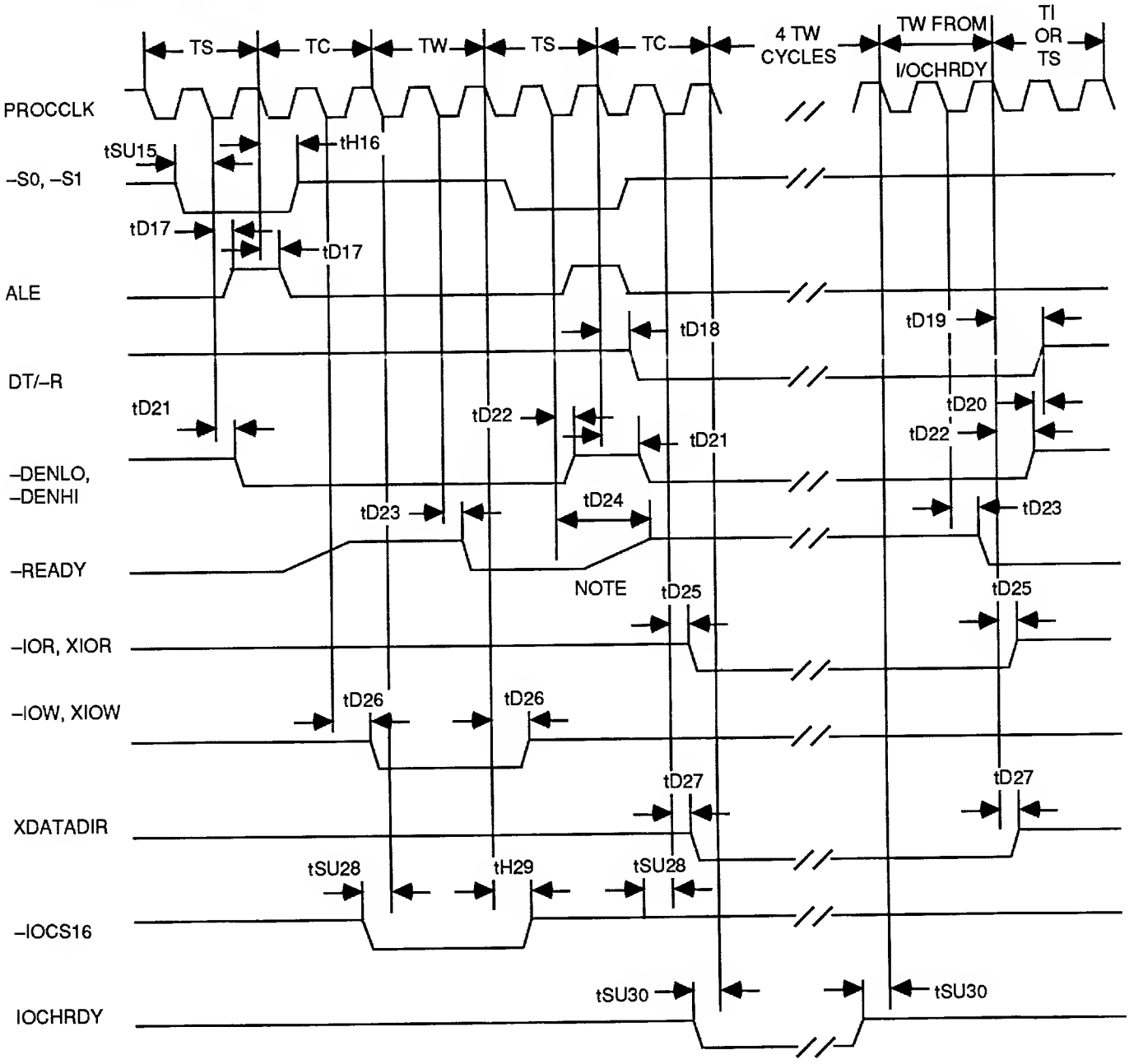
4. DIR245 goes low for a write cycle. It will remain high for read cycles.

RESET AND CLOCK TIMING WAVEFORMS



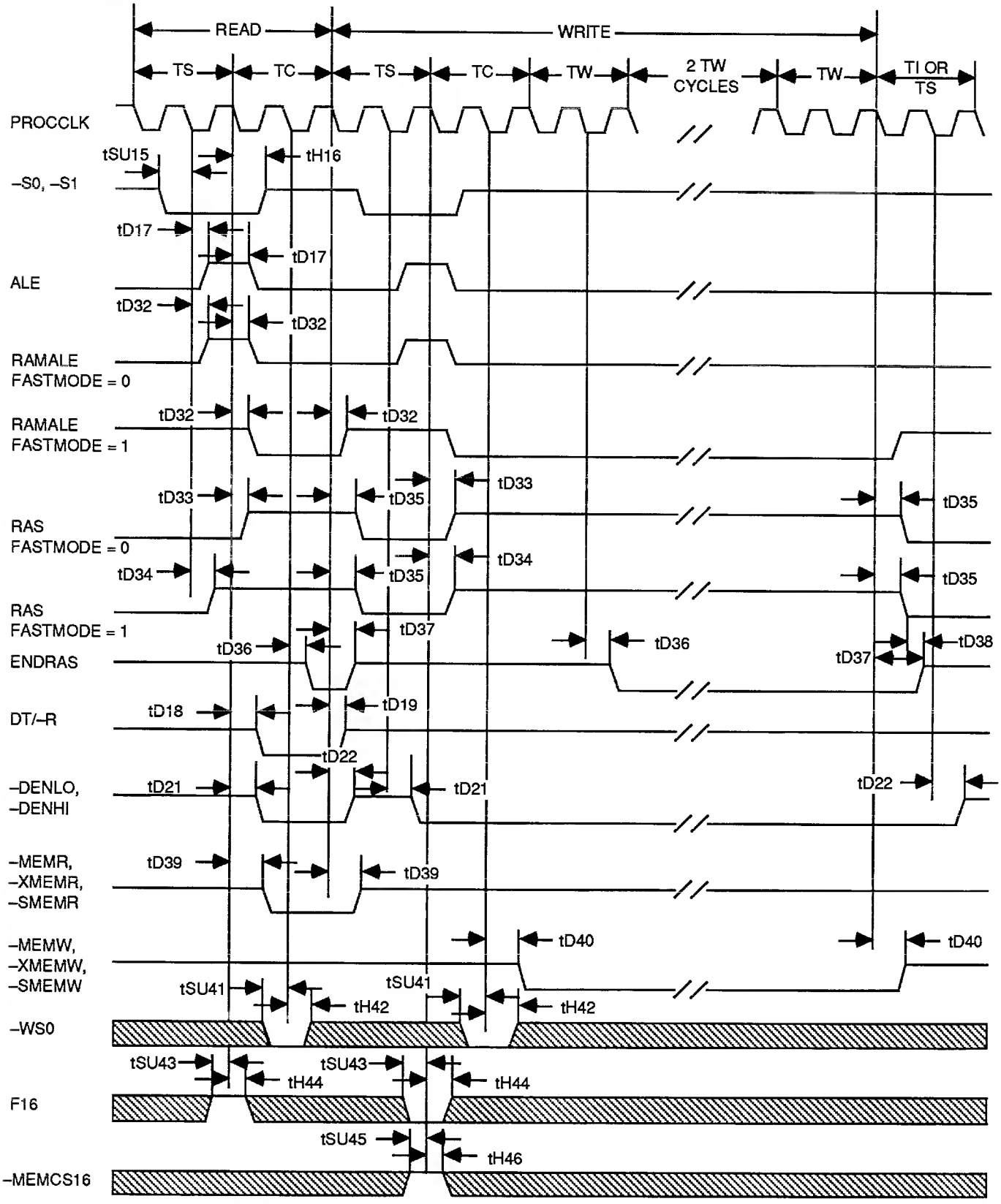
Note: POWERGOOD is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific PROCCLK edge.

I/O TIMING WAVEFORM



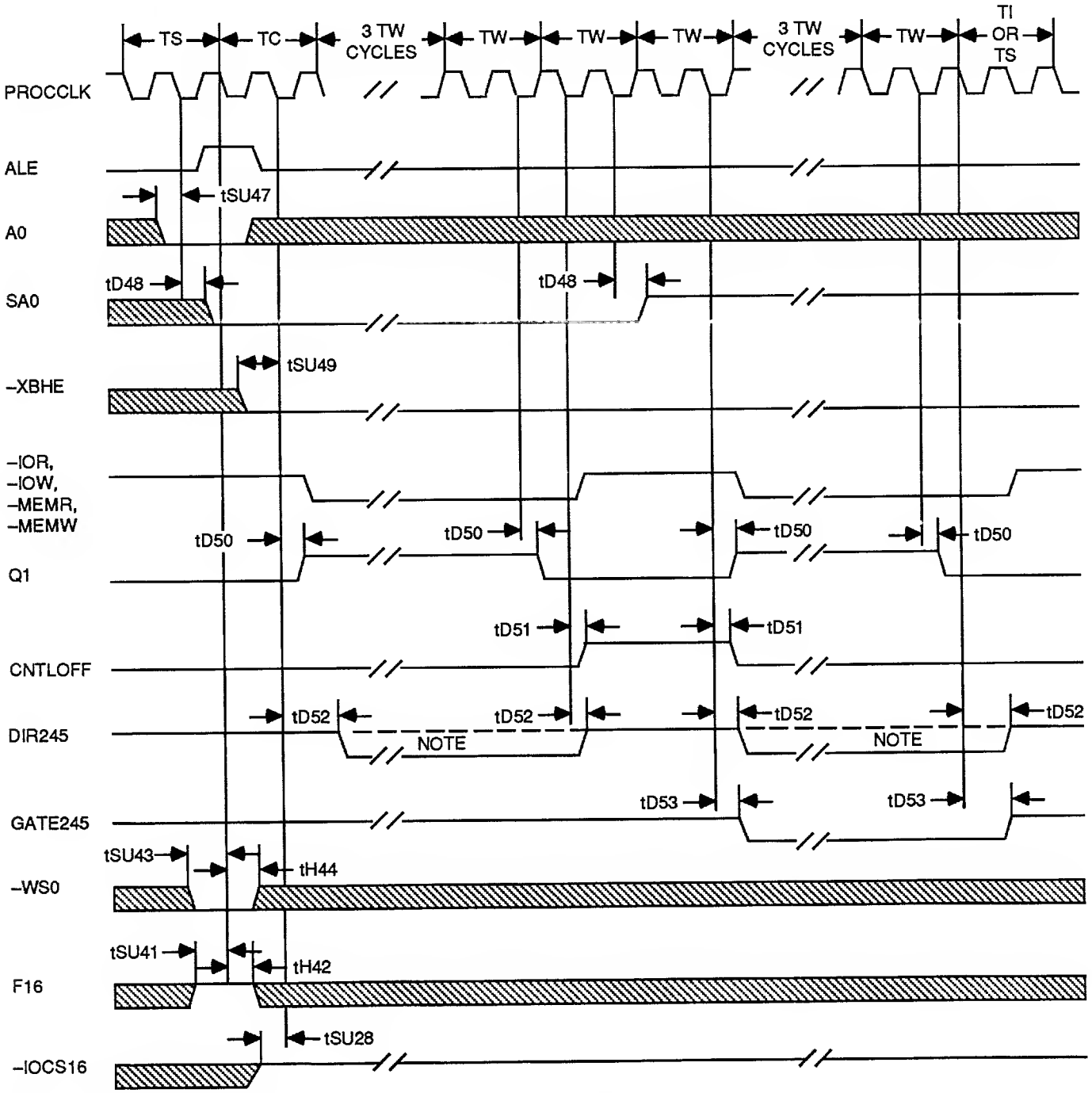
Note: –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLK cycles. We recommend 700 Ω for the pull-up resistor for 10 MHz and 12 MHz systems.

MEMORY TIMING WAVEFORM



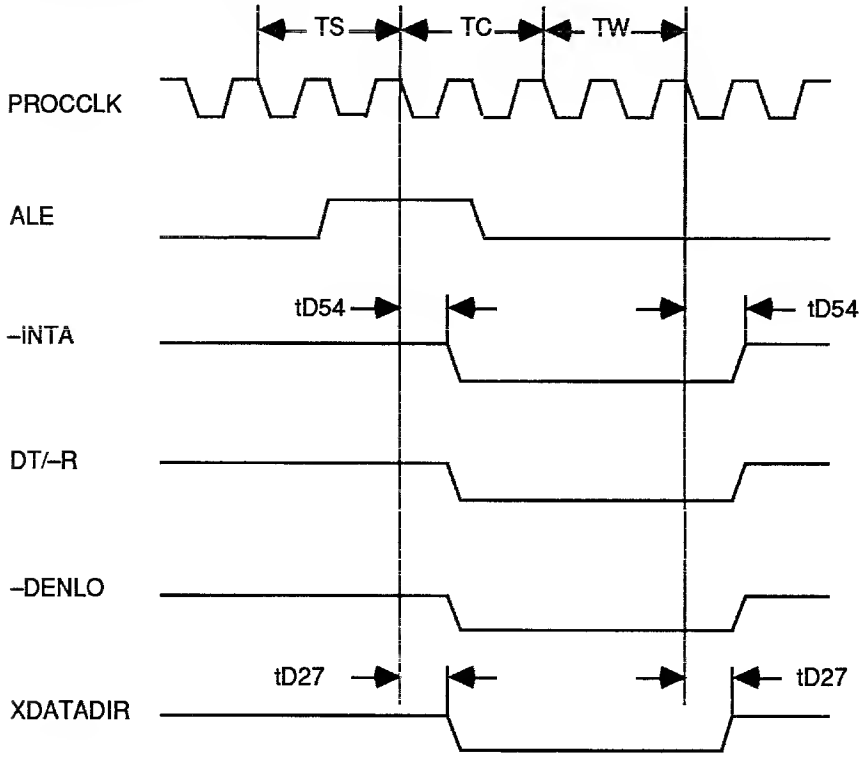
4

CONVERSION TIMING WAVEFORM



Note: DIR245 goes low for a write cycle. It will remain high for read cycles.

INTA TIMING WAVEFORM

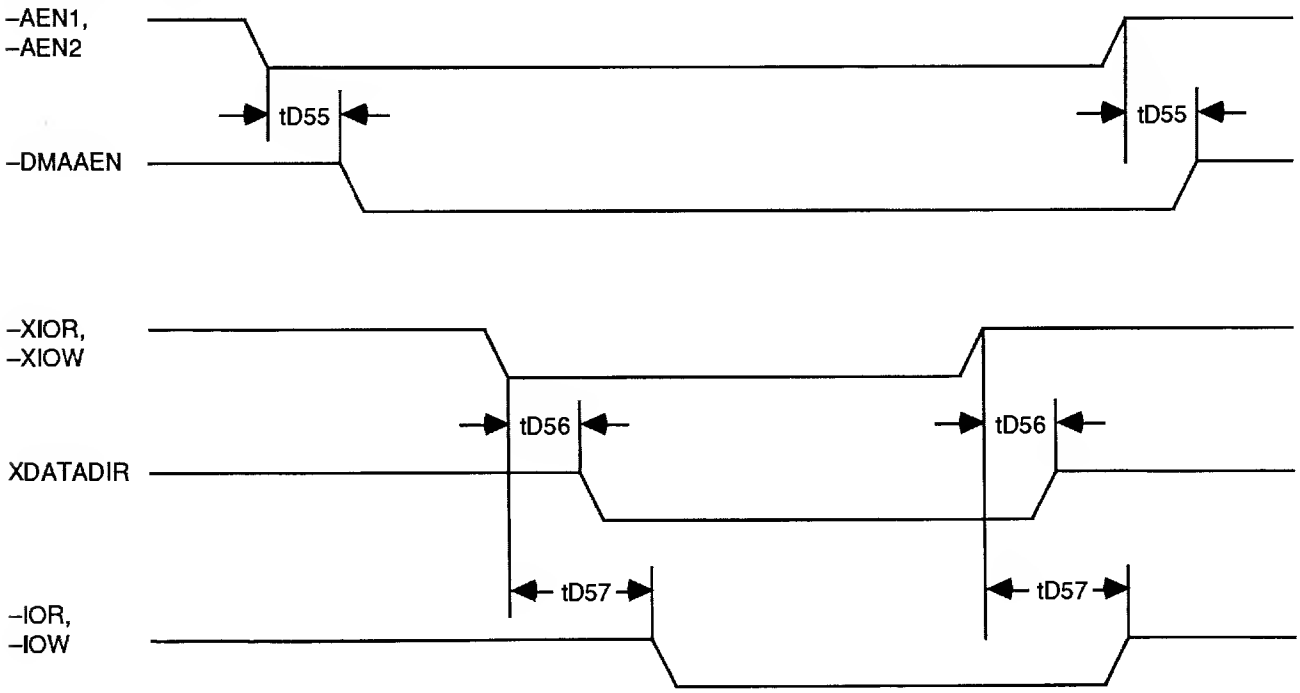


DMA MODE TIMING

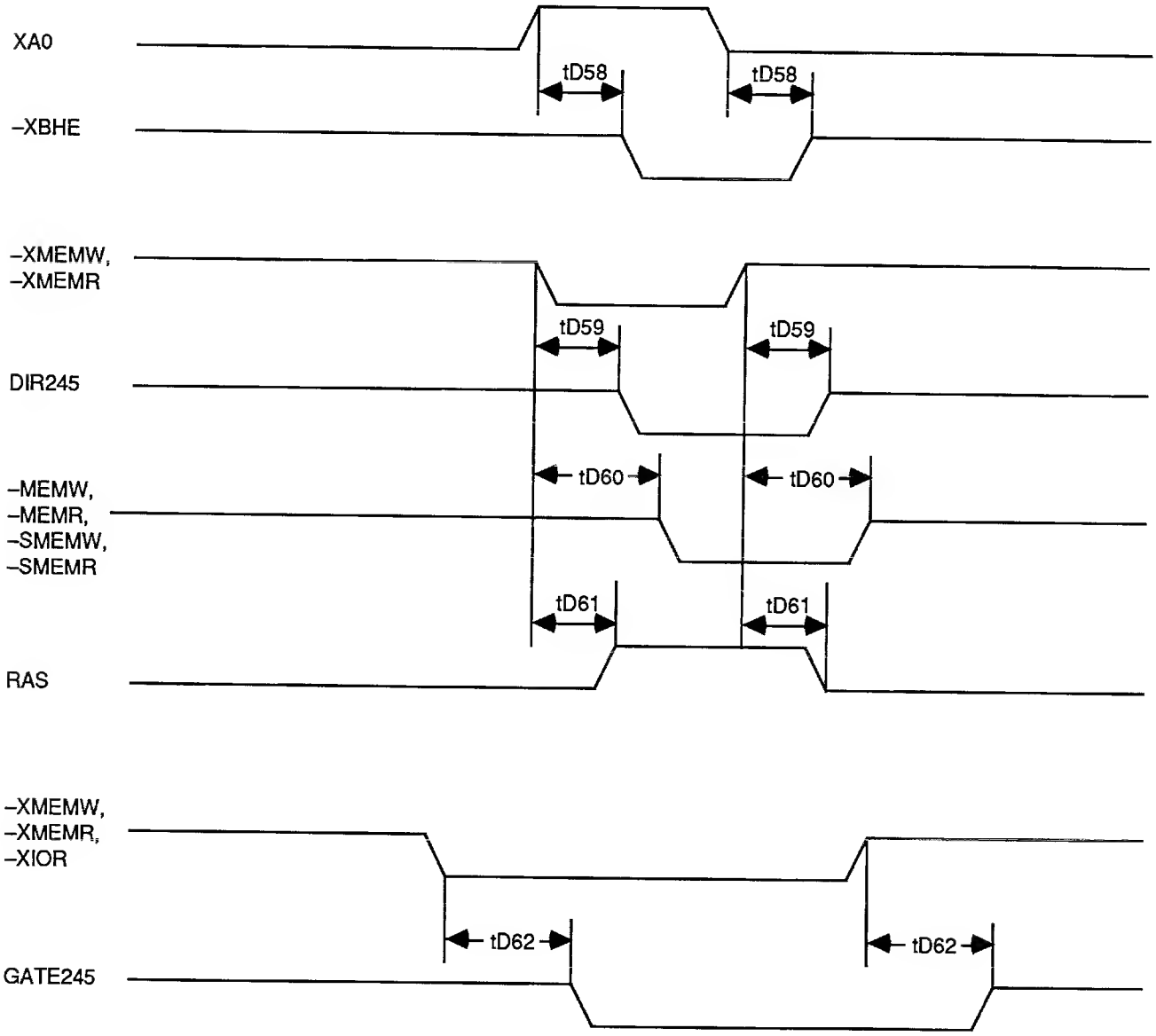
Symbol	Parameter	Min	Max	Unit	Condition
tD55	–DMAAEN Delay		20	ns	Note 1
tD56	XDATADIR Delay		27	ns	From –XIOR
tD57	–IOR, –IOW Delay		40	ns	
tD58	–XBHE Delay		35	ns	Note 2
tD59	DIR245 Delay		35	ns	
tD60	–MEMW, –MEMR, –SMEMW, –SMEMR Delay		40	ns	
tD61	RAS Delay		35	ns	
tD62	GATE245 Delay		40	ns	–AEN1 Only

Notes: 1. Either –AEN1 or –AEN2 forces –DMAAEN low.
2. During –AEN2, –XBHE is low; during –AEN1, –XHBE follows XA0 inverted.

DMA MODE TIMING WAVEFORMS



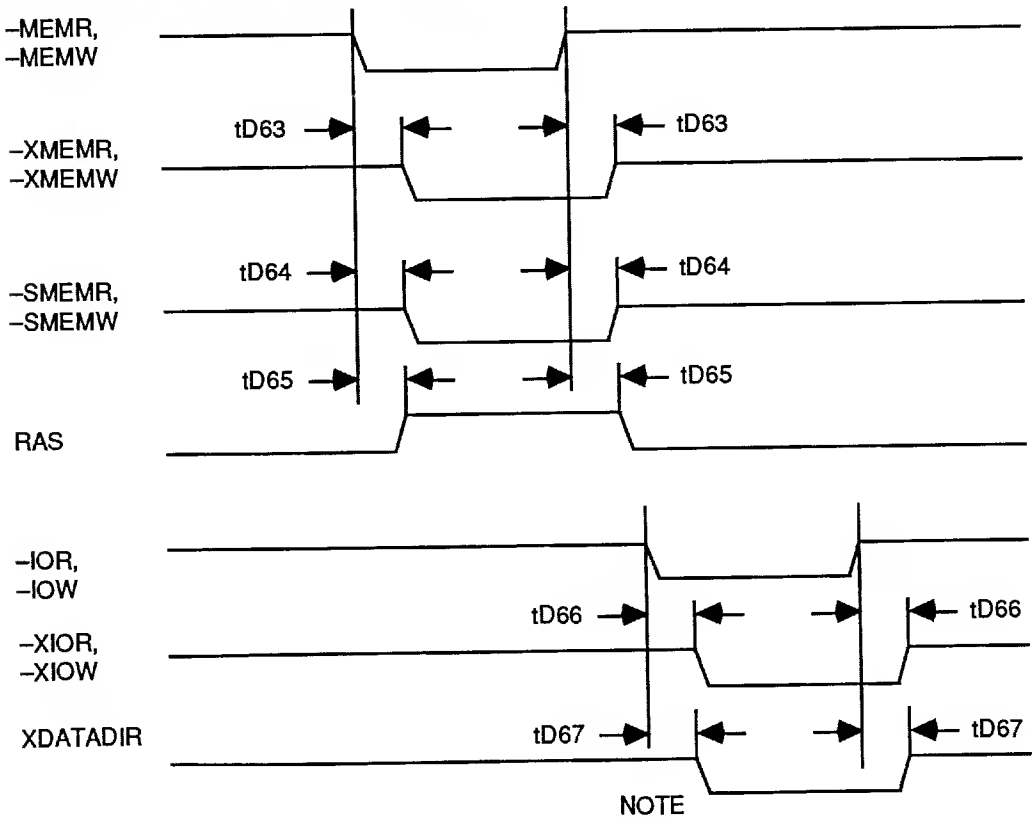
DMA MODE TIMING WAVEFORMS (Cont.)



BUS MASTER MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD63	–XMEMR, –XMEMW from –MEMR, –MEMW Delay		250	ns	
tD64	–SMEMR, –SMEMW from –MEMR, –MEMW Delay		239	ns	
tD65	RAS from –MEMR, –MEMW Delay		237	ns	
tD66	–XIOR, –XIOW from –IOR, –IOW Delay		8	ns	
tD67	XDATADIR from –IOR, –IOW Delay		8	ns	

BUS MASTER MODE TIMING WAVEFORM

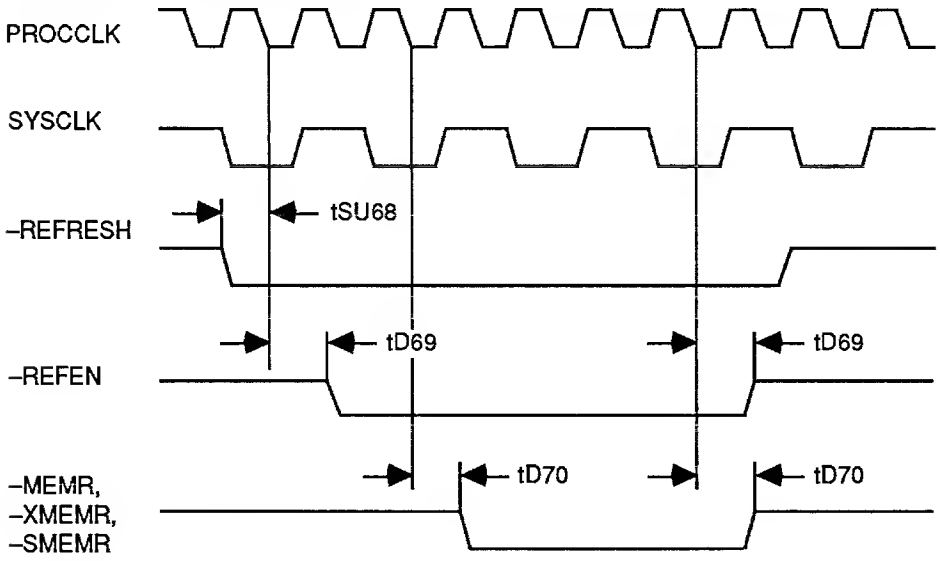


Note: XDATADIR goes low only for –IOR when XA9, XA8 are low and –NPCS is not active.

REFRESH TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tSU68	–REFRESH to PROCCLK Setup Time	20		ns	
tD69	–REFEN from PROCCLK Delay Time		35	ns	
tD70	–MEMR, –XMEMR, –SMEMR from PROCCLK Delay Time		60	ns	

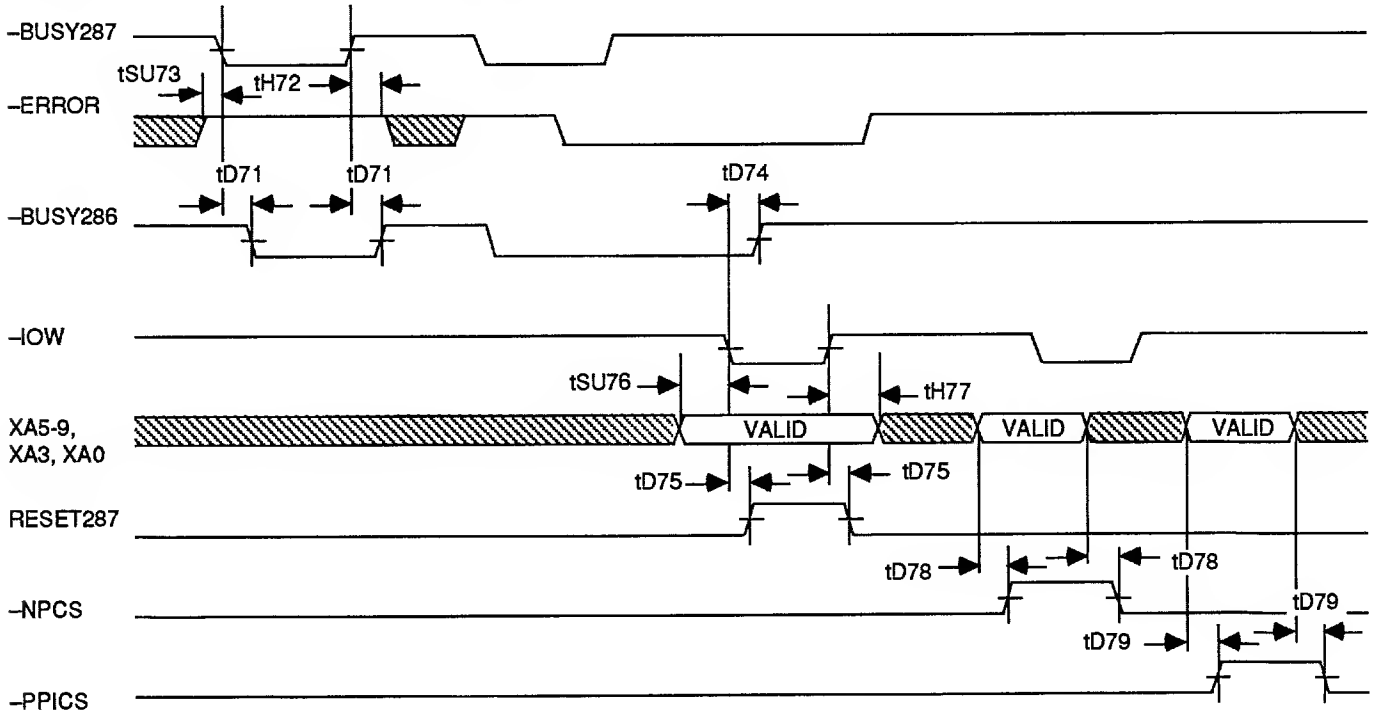
REFRESH TIMING WAVEFORM



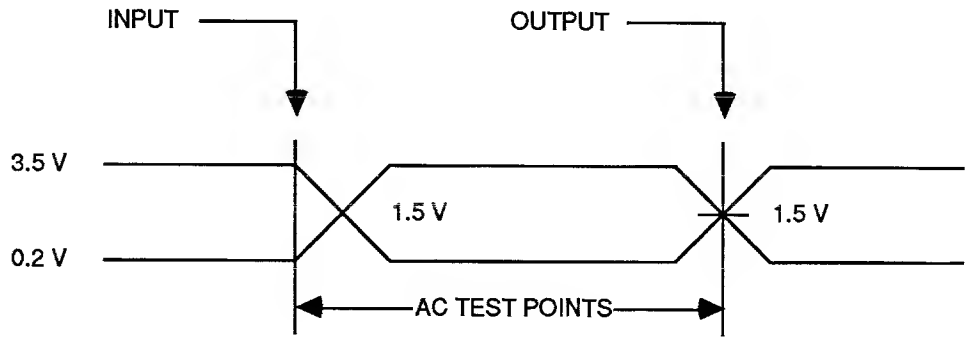
NUMERICAL PROCESSOR INTERFACE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD71	–BUSY286 from –BUSY287 Delay		35	ns	
tH72	–ERROR from –BUSY287 Hold Time	15		ns	
tSU73	–ERROR to –BUSY287 Setup Time	20		ns	
tD74	–BUSY286 from –IOW Delay		35	ns	
tD75	RESET287 from –IOW Delay		35	ns	
tSU76	XA Inputs to –IOW Setup Time	25		ns	
tH77	XA Inputs from –IOW Hold Time	20		ns	
tD78	XA Inputs to –NPCS Delay		35	ns	
tD79	XA Inputs to –PPICS Delay		35	ns	

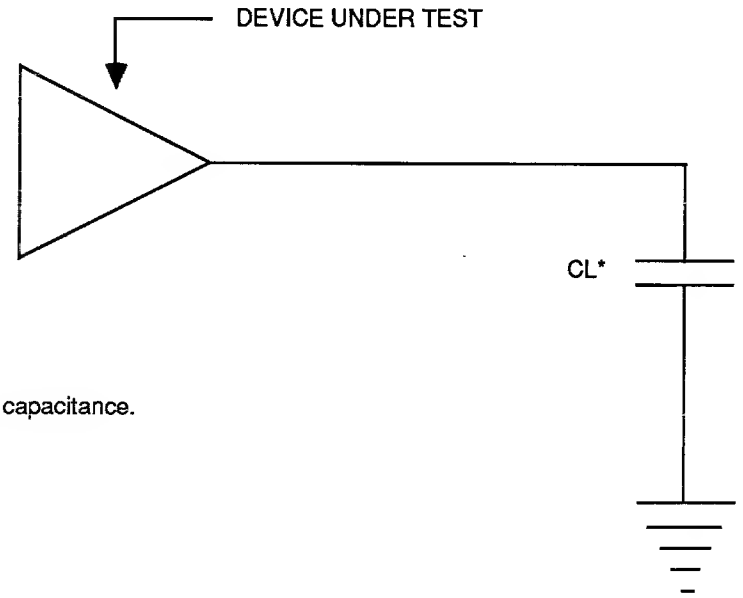
NUMERICAL PROCESSOR INTERFACE TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
49	200
39-42, 46, 50, 51, 65	150
20-22, 31, 34-37, 45, 47,	100
29	60
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to + 7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 20 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VOL3	Output Low Voltage		0.45		IOL = 2 mA, All Other Pins
VIH	Input High Voltage	2.0	VDD + 0.5	V	Except POWERGOOD
VIL	Input Low Voltage	–0.5	0.8	V	
VIHS	Input High Voltage	4.0	VDD + 0.5	V	POWERGOOD, Schmitt-trigger
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	Except –S0, –S1, XTAL1(2), XTAL2(2)
ILIS	Input Leakage Current	–0.5	0.01	µA	–S0, –S1, Note 3
ILIX	Input Leakage Current	50	50	µA	XTAL1(2), XTAL2(2)
ICC	Power Supply Current		20	mA	Note 4

Notes: 1. Pins 39-42 and 49-51.
2. Pins 20-22, 31, 34-37, 45-47 and 65.
3. –S1 and –S0 have small pull-up resistors to VDD and source up to 0.5 mA when pulled low.
4. Inputs = VSS or VDD, outputs not loaded.

PC/AT-COMPATIBLE MEMORY CONTROLLER

FEATURES

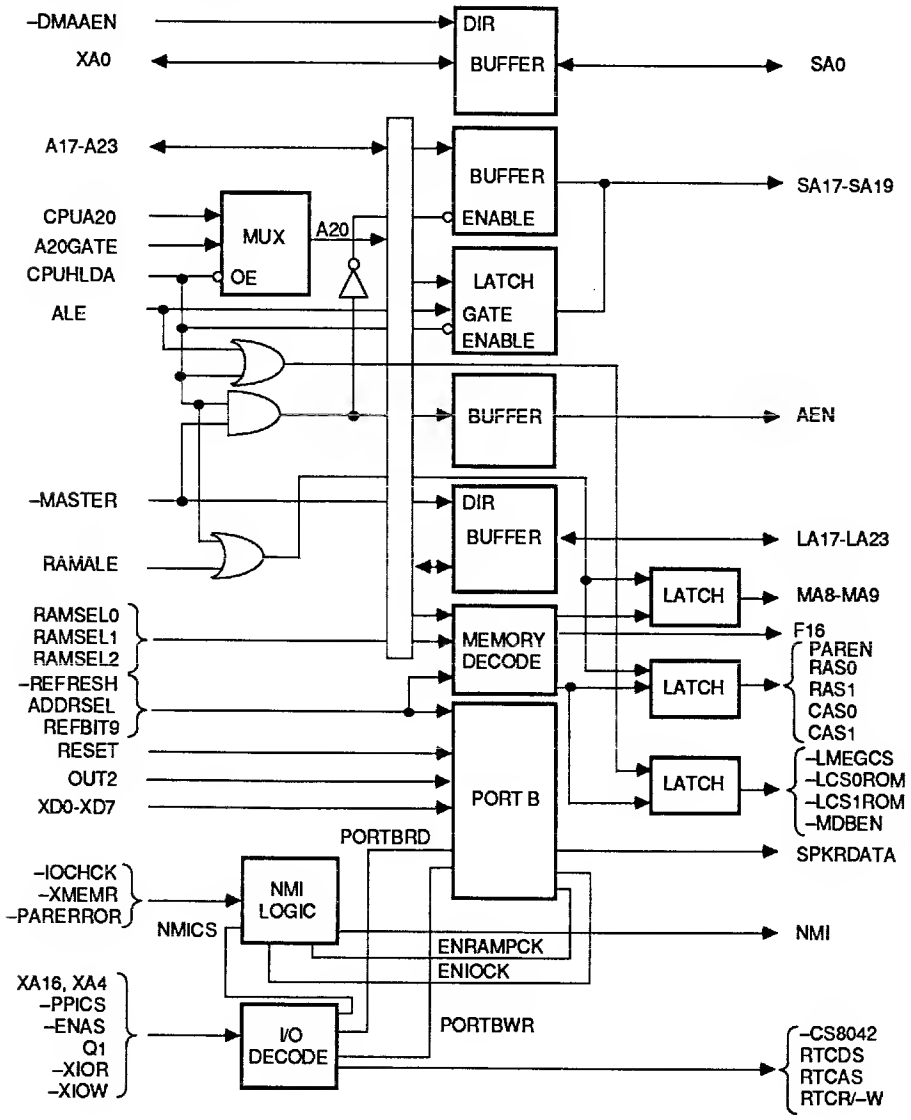
- Fully compatible with IBM PC/AT-type designs
- Completely performs memory control function in IBM PC/AT-compatible systems
- Replaces 20 integrated circuits on PC/AT-type motherboard
- Support 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C102A PC/AT-Compatible Memory Controller generates the row and column decodes necessary to support the dynamic RAMs used in PC/AT-type systems. In addition, the device allows five motherboard memory options for the user, up to a full 4M-byte system. Four of the five options allow a full 640k-bytes user area to support the disk operating system (DOS). In addition, the VL82C102A provides the upper addresses to the I/O slots, the chip select for the ROM and RAM memory, and drives the system's speaker.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C102A is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



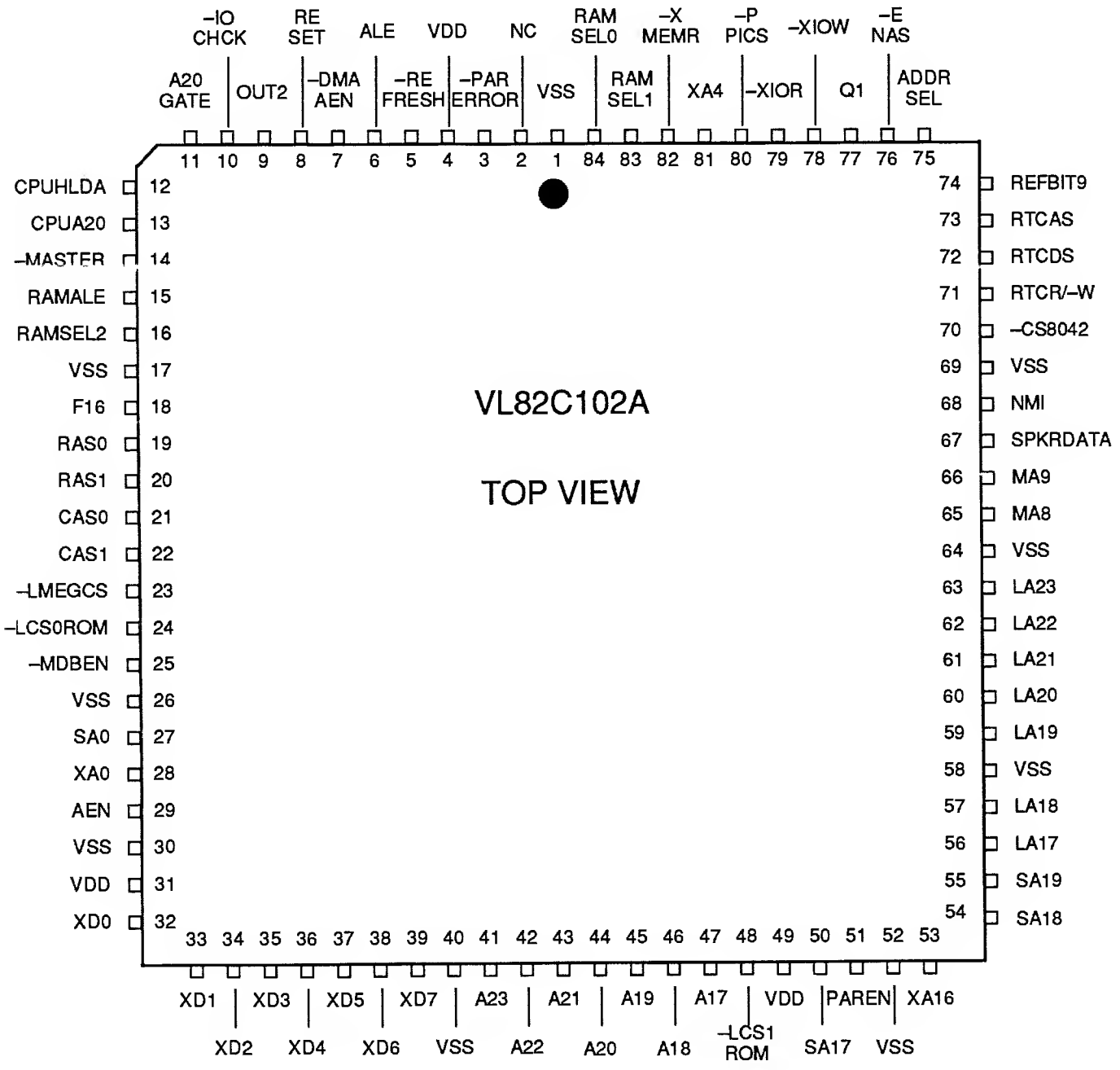
ORDER INFORMATION

Part Number	Package
VL82C102A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

4

PIN DIAGRAM


VL82C102A
TOP VIEW
11 –IO CHCK
10 A20 GATE
9 OUT2
8 RE SET
7 –DMA AEN
6 ALE
5 –RE FRESH
4 VDD
3 –PAR ERROR
2 NC
1 VSS
84 RAM SEL0
83 RAM SEL1
82 –X MEMR
81 XA4
80 –P PICS
79 –XIOR
78 –XIOW
77 Q1
76 –E NAS
75 ADDR SEL
12 CPUHLDA
13 CPUA20
14 –MASTER
15 RAMALE
16 RAMSEL2
17 VSS
18 F16
19 RAS0
20 RAS1
21 CAS0
22 CAS1
23 –LMEGCS
24 –LCS0ROM
25 –MDBEN
26 VSS
27 SA0
28 XA0
29 AEN
30 VSS
31 VDD
32 XD0
74 REFBIT9
73 RTCAS
72 RTCDS
71 RTCR/–W
70 –CS8042
69 VSS
68 NMI
67 SPKRDATA
66 MA9
65 MA8
64 VSS
63 LA23
62 LA22
61 LA21
60 LA20
59 LA19
58 VSS
57 LA18
56 LA17
55 SA19
54 SA18
33 XD1
34 XD2
35 XD3
36 XD4
37 XD5
38 XD6
39 XD7
40 VSS
41 A23
42 A22
43 A21
44 A20
45 A19
46 A18
47 A17
48 –LCS1 ROM
49 VDD
50 SA17
51 PAREN
52 VSS
53 XA16

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
NC	2		No Connect
–PARERROR	3	I	Parity Error - A low true input used to indicate that a memory parity error has occurred.
–REFRESH	5	I	Refresh - An active low input used to initiate a refresh cycle for the dynamic RAMs.
ALE	6	I	Address Latch Enable - This is a positive edge input that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
–DMAAEN	7	I	DMA Address Enable - This is an active low input. It is active whenever an I/O device is making a DMA access to the system memory.
RESET	8	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK.
OUT2	9	I	Out 2 - The output of the timer controller. it can be read by the CPU on Port B.
–IOCHCK	10	I	I/O Channel Check - This active low input is asserted by devices on the expansion bus. It will generate a non-maskable interrupt if NMI is enabled. –IOCHCK can be read by the CPU on Port B.
A20GATE	11	I	A20GATE - Used to select the proper value for address bit 20. CPUA20 is transmitted out as A20 if A20GATE is high, otherwise A20 is forced low.
CPUHLDA	12	I	CPU Bus Hold Acknowledge - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
CPUA20	13	I	CPU Address Bus Bit 20 - It is transmitted out as A20 if A20GATE is high.
–MASTER	14	I	Master - An active low input. It is asserted low by devices on the expansion bus. A low indicates that another device is active.
RAMALE	15	I	RAM Address Latch Enable - Used in the FASTMODE of operation. When FASTMODE is inactive RAMALE is equal to ALE
RAMSEL2	16	I	RAM Select 2 - Used with RAMSEL0 and RAMSEL1 to select the system RAM configuration.
F16	18	O	An output that indicates a word memory access. It is used to inhibit command delays during a 16 bit memory access.
RAS0	19	O	RAM Address Select 0 - An active high output that is the select signal for the lower address bank of RAM.
RAS1	20	O	RAM Address Select 1 - An active high output that is the select signal for the upper address bank of RAM.
CAS0	21	O	An active high output that is the select signal for the lower bank of RAM.
CAS1	22	O	An active high output that is the select signal for the upper bank of RAM.
–LMEGCS	23	O	Lower Megabyte Chip Select - An active low output that indicates that the lower memory address space (0-1 megabyte) is selected.
–LCS0ROM	24	O	Latched Chip Select 0 for ROM - An active low output that is the latched chip select for the ROM address space.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–MDBEN	25	O	Memory Bus Enable - An active low output that controls the direction of data flow between the system and memory data buses. When –MDBEN is high data flows from memory to system. When low, data flows from system to memory.
SA0	27	I/O	System Address Bus Bit 0 - This signal will be an output with the value of XA0 when –DMAAEN is low. It will be an input and drive XA0 when –DMAAEN = 1.
XA0	28	I/O	Peripheral Address Bus Bit 0 - This signal is an output driven by SA0 when –DMAAEN = 1, and an input driving SA0 when –DMAAEN = 0.
AEN	29	O	Address Enable - This is an output signal for the expansion bus. It will go low when master is active or HLDA is inactive.
XD0-XD3	32-35	I/O	Peripheral Data Bus Bits 0-3 - These are data bits for the peripheral bus. They are outputs when Port B is being read; otherwise they are inputs.
XD4-XD6	36-38	O	Peripheral Data Bus Bits 4-6 - These are data bits for the peripheral bus. They are driven as outputs when Port B is being read, otherwise three-stated.
XD7	39	I/O	Peripheral Data Bus Bit 7 - An output when Port B is read, and an input which enables NMI during an NMICS.
A17-A23	47-41	I/O	CPU Bus Bits 17-23 - These are the upper bits of the CPU address bus. Outputs when –MASTER is low, inputs when –MASTER is high.
–LCS1ROM	48	O	Latched Chip Select 1 for ROM - The active low latched chip select output for the high ROM address space.
PAREN	51	O	Parity check Enabled - Logical OR of CAS0 and CAS1, indicates a memory access so parity check is enabled.
SA17-SA19	50, 54, 55	O	System Address Bus Bits 17-19 - A17-A19 are latched by ALE and transmitted out on these outputs when CPUHLDA is inactive. They are driven directly by A17-A19 when CPUHLDA is active and –MASTER is inactive. They are three-stated when –MASTER is active.
XA16	53	I	Peripheral Address Bus Bit 16 - This switches between –LCS0ROM and –LCS1ROM.
LA17, LA18, LA19-LA23	56, 57 59-63	I/O	System Address Bus Bits 17-23 - These are the upper bits of the system address bus to the expansion slots. These pins are configured as outputs when –MASTER is high, and as inputs when –MASTER is low.
MA8, MA9	65, 66	O	DRAM Memory Address Bus Bits 8-9 - These outputs are the 8th and 9th bit of the DRAM memory address. They are located on the VL82C102A to allow system address mapping. REFBIT9 is multiplexed into MA8 during a refresh cycle.
SPKRDATA	67	O	Speaker Data - Output to be buffered by the 75477 and sent to the speaker.
NMI	71	O	Non-maskable Interrupt - This output is the non-maskable interrupt signal for the CPU.
–CS8042	70	O	Chip Select signal for the Keyboard Controller - This active low output is the chip select signal for the keyboard controller programmable interface device.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–RTCR/W	71	O	Real Time Clock Signal for Read/Write - This is the read/write select output signal for the real time clock. A high indicates a read operation and a low write operation.
RTCDS	72	O	Real Time Clock Data Strobe - This is the data strobe for the real time clock.
RTCAS	73	O	Real Time Clock Address Strobe - This is the address strobe for the real time clock.
REFBIT9	74	I	Refresh Bit 9 - The carry out of the refresh counter. It is used to generate a refresh for 1M DRAMs. It is multiplexed out as MA8 when –REFRESH is active.
ADDRSEL	75	I	Address Select - This input is a multiplex row/column select for the Memory Address Bus drivers.
–ENAS	76	I	Enable Address Strobe - This active low input is used to enable the address strobe on the real time clock. It will go low the first time –S0 is asserted after a system reset.
Q1	77	I	Goes active during the second phase of a CPU bus cycle following the TS state. It is used by the VL82C102A chip to generate the address strobe for the real time clock.
–XIOW	78	I	Input/Output Write - The active low input command to and from the peripheral bus. Used to generate selects for the keyboard controller, real time clock, and Port B.
–XIOR	79	I	Input/Output Read - The active low input command to and from the peripheral bus. Used to generate selects for the keyboard controller, real time clock, and Port B.
–PPICS	80	I	Programmable Peripheral Interface Chip Select - An active low input used to generate the chip select for the keyboard controller.
XA4	81	I	Peripheral Address Bus Bit 4 - An input used to generate selects for the keyboard controller, real time clock, and Port B.
–XMEMR	82	I	Memory Read - An active low input command to and from the peripheral bus. This pin is used to determine the direction of data on the memory data bus and to clock in parity check results.
RAMSEL1	83	I	RAM Select 1 - This input is used with RAMSEL0 to designate the system RAM configuration.
RAMSEL0	84	I	RAM Select 0 - This input is used with RAMSEL1 to designate the system RAM configuration.
VDD	4, 31, 49		System Power: 5 V
VSS	1, 17, 26, 30, 40, 52, 58, 64, 69		System Ground

4

FUNCTIONAL DESCRIPTION

The VL82C102A Memory Controller provides address buffering for the upper address bits on the system and CPU address buses. It generates chip selects for the two possible RAM banks and the two possible ROM banks. The VL82C102A also contains the Port B register logic to control the Non-Maskable Interrupt signal and the speaker. It also generates chip select decodes for the keyboard controller and real time clock.

MEMORY DECODES

The upper address bits A17-A23 and XA16 are used to decode chip selects for all on-board memory. The three option inputs RAMSEL2, RAMSEL1, and RAMSEL0 are used to select one of five possible memory mapping options. Refer to Figure 1.

RAM SELECTS

The memory mapping options shown in Figure 1 are used to generate the enable signals for the RAS and CAS pulses to the DRAMs. RAS0 and CAS0 are the enables for Bank 0. RAS1 and CAS1 are the enables for Bank 1. These signals will be active anytime the decode on address bits A17-A23 fall in the ranges shown in the memory maps. The signals are latched by the input signal RAMALE. The latches will be transparent while RAMALE is high and hold the value in the latch while RAMALE is low. The latch clocks will also be forced high when CPUHLDA is active making the latches transparent during all hold acknowledge operations.

When –REFRESH is active, address bits A17-A23 are ignored and both RAS0 and RAS1 are forced active (high) while CAS0 and CAS1 are forced inactive (low).

MA8 AND MA9

A17-A23 are also used to generate four address bits for the upper address bits of the DRAM memory space. These address bits are also latched by the combination of RAMALE and CPUHLDA as described for the RAM selects. The four latched address bits are then multiplexed out on MA8 and MA9. MA9 is needed only if a memory mapping option using 1M-bit DRAMs is selected. REFBIT9 is multiplexed out onto MA8 during refresh cycles.

ROM SELECTS

The ROM address space is decoded from A17-A23 and latched by ALE. These latches are also forced transparent when CPUHLDA is active in the same manner as the latches for the RAM chip selects. This latched value is then split into the two signals –LCS0ROM and –LCS1ROM using the XA16 input. If two banks of 32K by 16-bit words of ROM are used, the XA16 input must by tied to the XA16 signal on the system board to select the proper bank based on the value on XA16. If XA16 is low, –LCS0ROM will go active any time the ROM address space is decoded. If XA16 is high, –LCS1ROM is decoded. In this configuration –LCS0ROM selects the address space from 0E 0000 to 0E FFFF while –LCS1ROM selects the address space 0F 0000 to 0F FFFF. When only using one bank of 16K, 32K, or 64K by 16-bit words of ROM, the XA16 input can be tied high and –LCS1ROM used to select the bank. In this configuration –LCS0ROM will always remain inactive while –LCS1ROM selects the address space 0E 0000 to 0F FFFF.

The ROM address space is duplicated at FE 0000 to FF FFFF and the chip selects will go active in the same manner as described above in this address space.

UPPER ADDRESS BUFFERS

The VL82C102A provides buffer drive capability to drive the card slots on the I/O signals LA17-LA23 and SA17-SA19. The values on A17-A23 are passed directly through to the LA17-LA23 outputs if –MASTER is high. If –MASTER is low LA17-LA23 become inputs and pass the value on those pins to the A17-A23 bus.

A17-A19 are latched by ALE and driven onto the SA17-SA19 bus whenever CPUHLDA is low. When CPUHLDA is high and –MASTER is high, the latch is bypassed and A17-A19 is driven directly to SA17-SA19. SA17-SA19 will be left floating when CPUHLDA is high and –MASTER is low.

ADDRESS BIT 20

Address bit 20 is handled differently than the other address bits. The A20 signal will be generated directly from CPUA20 (which should be connected to A20 on the 80286 CPU) if the input A20GATE is high. If A20GATE is low, the A20 signal is forced low.

ADDRESS BIT 0

A buffer transceiver between XA0 and SA0 is also provided on the VL82C102A. If the input –DMAAEN is high, signal flow is from SA0 to XA0. If –DMAAEN is low, signal flow is from XA0 to SA0.

PORT B

The Port B register in an AT-compatible design is located on the VL82C102A. It can be read or written to with an I/O command to address 61 hex. Port B is used to control the speaker and mask out NMI sources. It can be read to find status of –REFRESH, speaker data, and possible sources of NMI.

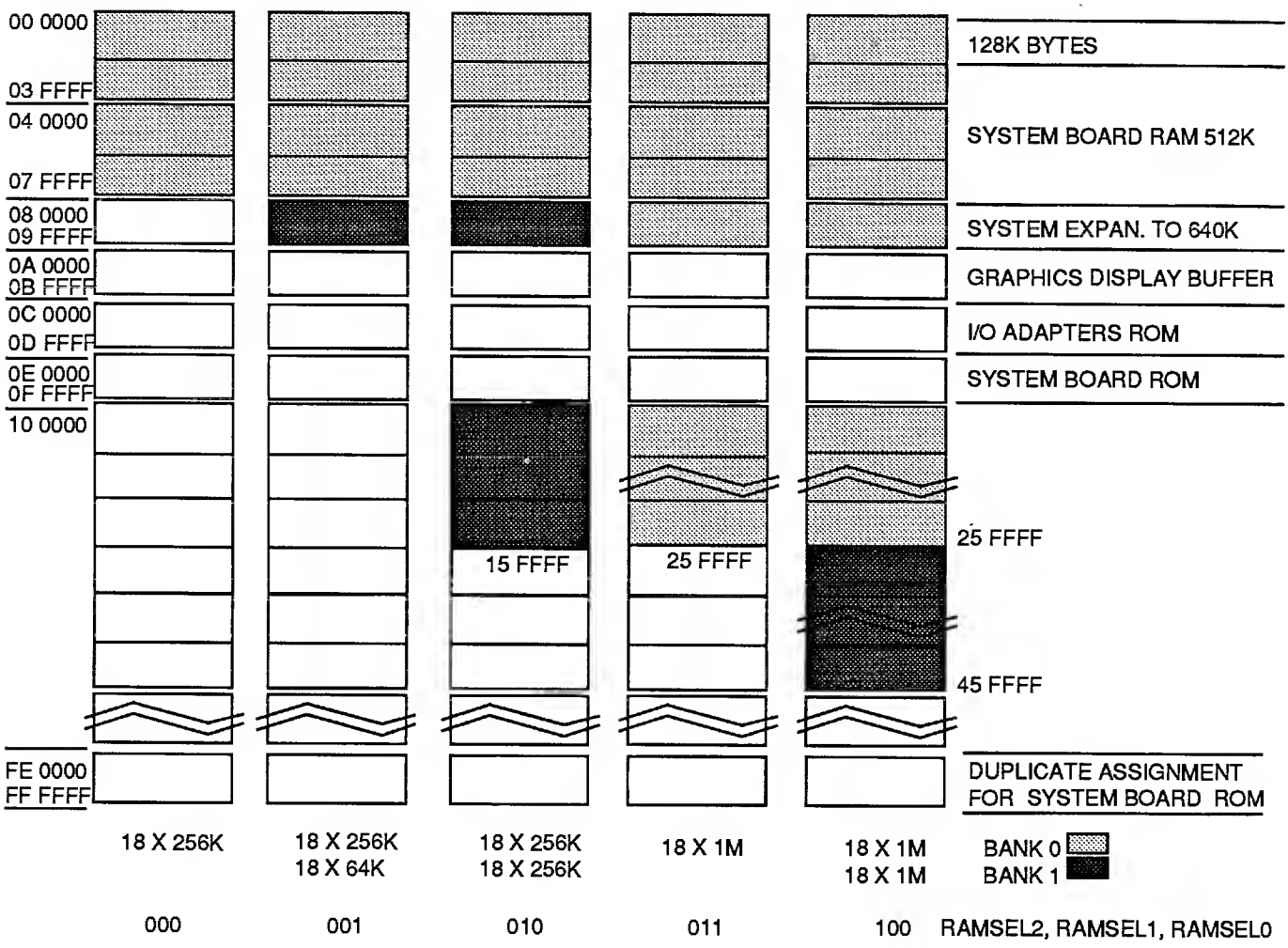
I/O DECODES

The VL82C102A provides the chip select signals for the on-board I/O peripherals (keyboard controller and real time clock).

NMI LOGIC

The logic necessary to control the Non-Maskable Interrupt (NMI) signal to the processor is contained in the VL82C102A. An NMI can be caused by a parity error from the system board DRAM or if an I/O adapter pulls the input IOCHCK low. These two possible sources can be individually enabled to cause an NMI by setting the appropriate bits in the Port B register. At power-up time, the NMI signal is masked off. NMI can be masked on by writing to I/O address 070 hex with bit 7 low, or masked off by writing to I/O address 070 hex with bit 7 high.

FIGURE 1. MEMORY MAP OPTIONS



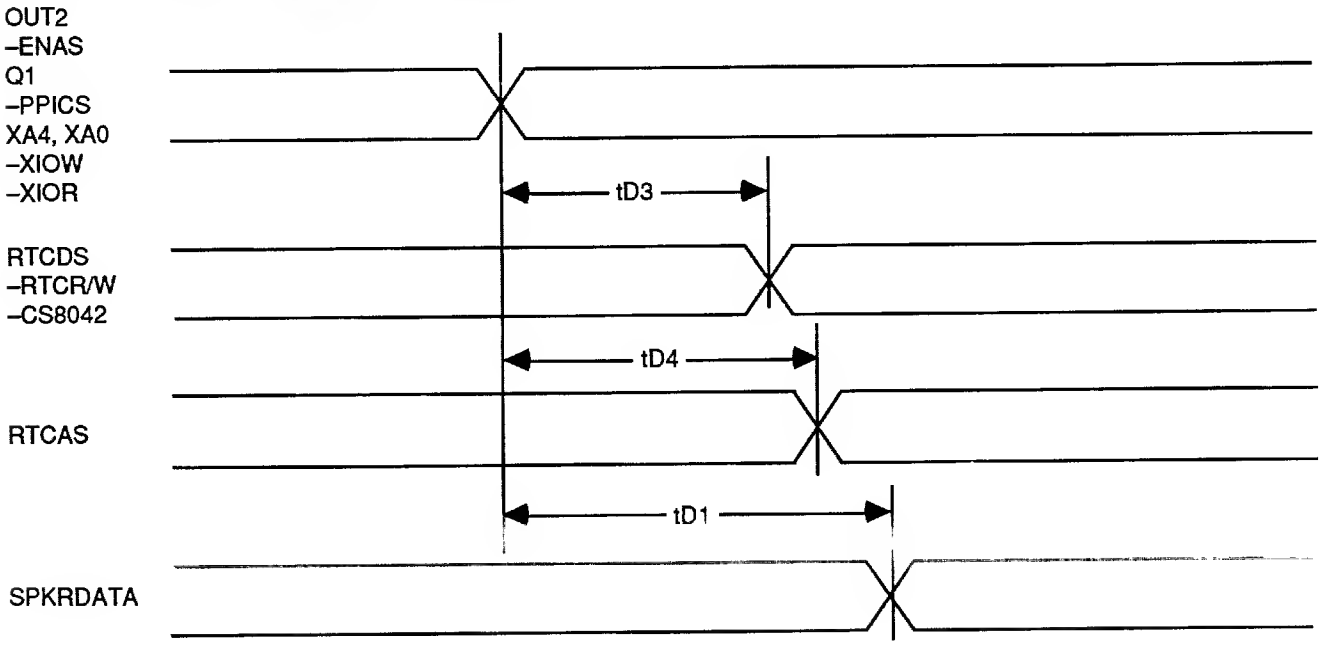
4

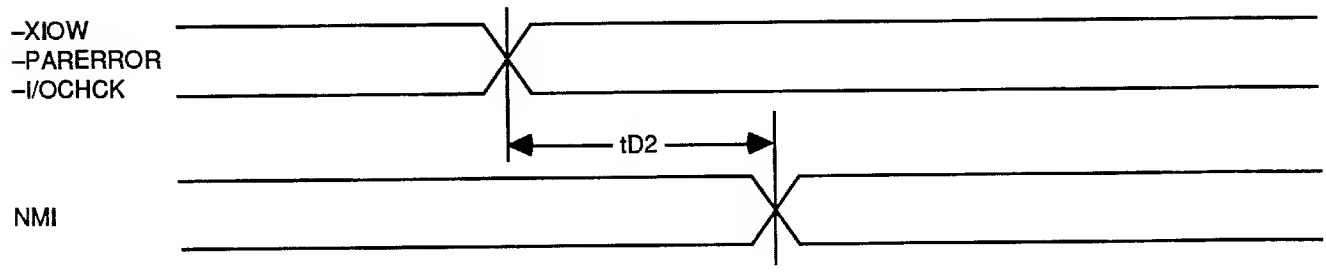
AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V

PERIPHERAL CONTROL TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD1	SPKRDATA Output Delay		40	ns	CL = 50 pF
tD2	NMI Output Delay		40	ns	CL = 100 pF
tD3	RTCDS, –RTCR/W, –CS8042 Output Delays		35	ns	CL = 50 pF
tD4	RTCAS Output Delay		40	ns	CL = 50 pF

PERIPHERAL CONTROL TIMING WAVEFORMS



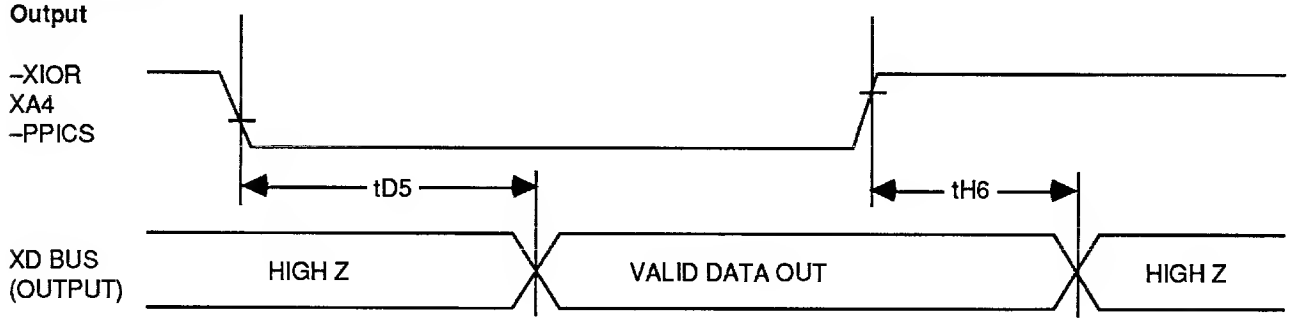


XD BUS TIMING

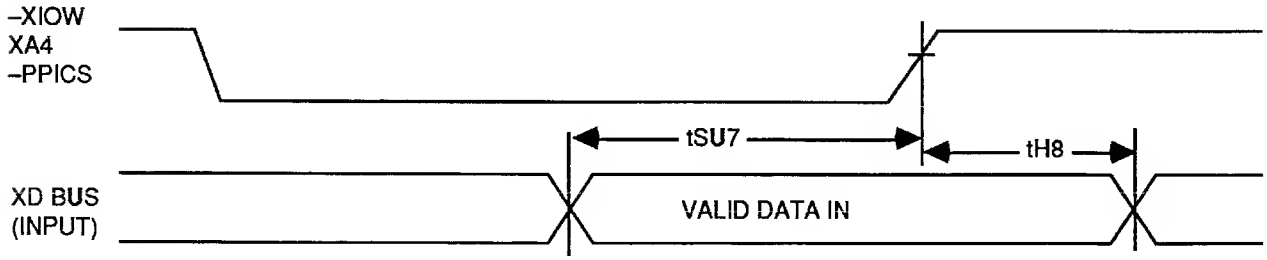
Symbol	Parameter	Min	Max	Unit	Condition
tD5	XD Bus Delay		40	ns	XD = Output
tH6	XD Bus Hold Time	6		ns	XD = Output
tSU7	XD Bus Setup Time	20		ns	XD = Input
tH8	XD Bus Hold Time	12		ns	XD = Input

XD BUS TIMING WAVEFORMS

Output



Input



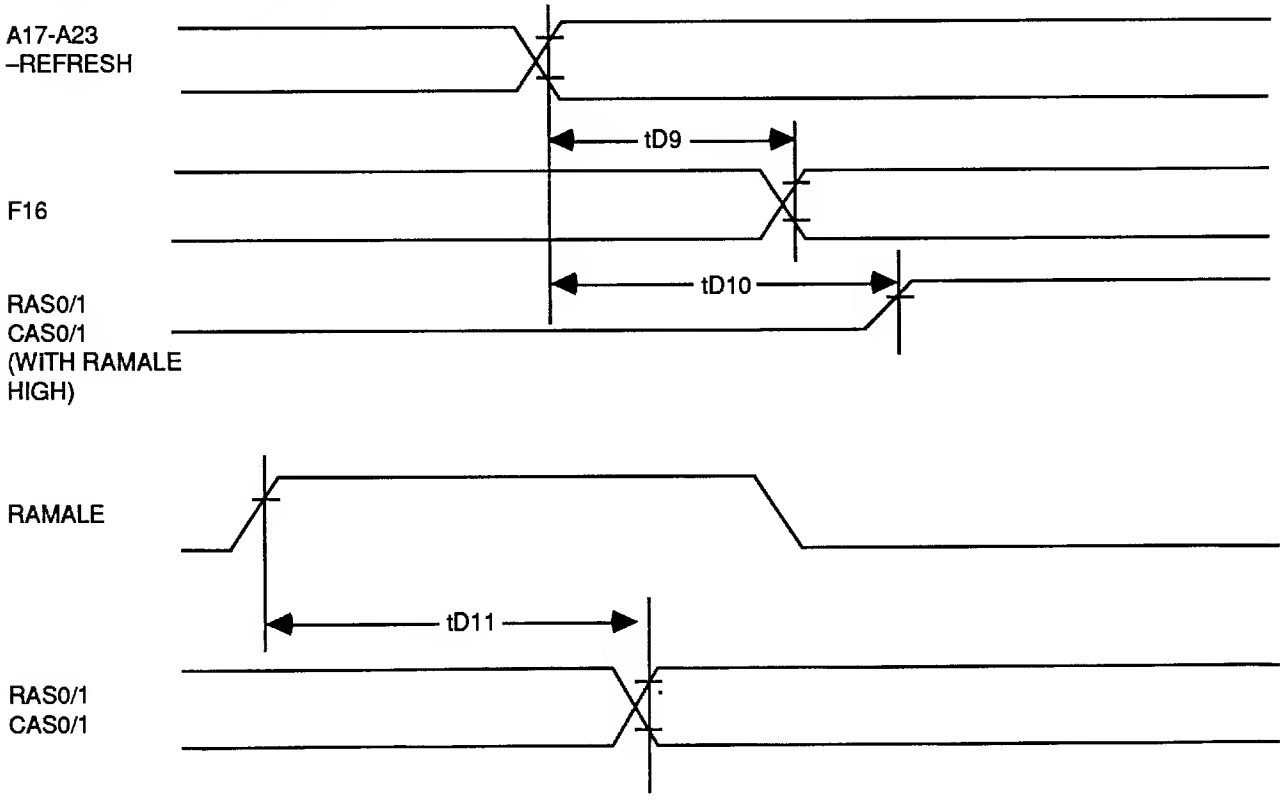
4

ADDRESS CONTROL TIMING

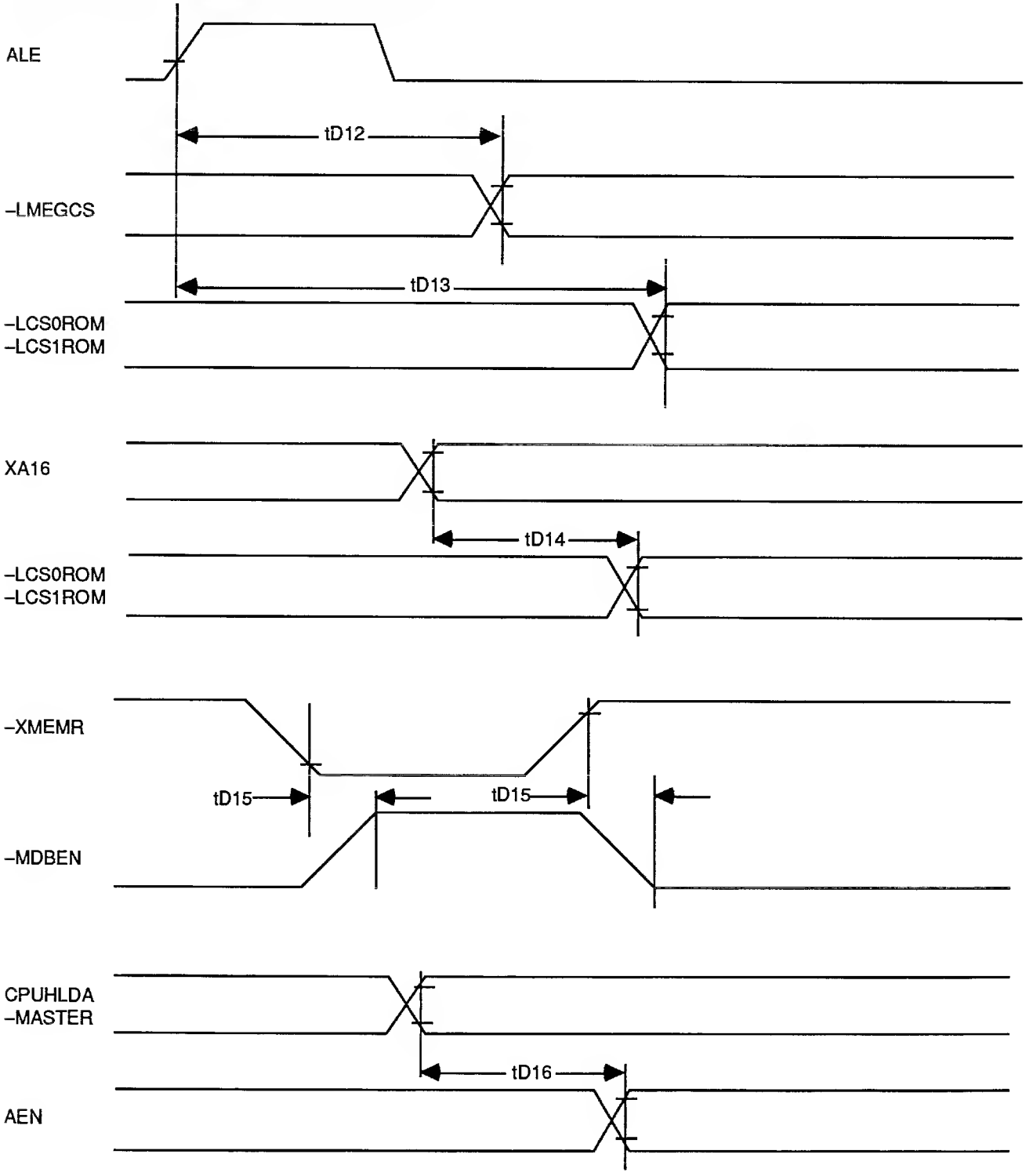
Symbol	Parameter	Min	Max	Unit	Condition
tD9	F16 Output Delay		40	ns	CL = 50 pF
tD10	RAS0/1, CAS0/1 Delay from A17-A23		45	ns	CL = 50 pF, RAMALE High
tD11	RAS0/1, CAS0/1 Delay from RAMALE		24	ns	
tD12	–LMEGCS Delay from ALE		30	ns	CL = 50 pF
tD13	–LCS1ROM, –LCS0ROM Delay from ALE		35	ns	CL = 50 pF
tD14	–LCS1ROM, –LCS0ROM Delay from A16		20	ns	CL = 50 pF
tD15	MDBEN Output Delay		30	ns	CL = 50 pF
tD16	AEN Output Delay		35	ns	CL = 150 pF

Note: RAMSEL0, RAMSEL1, and RAMSEL2 are assumed setup one processor clock before the user generates any memory control signals. These inputs are normally strapped to VDD or VSS in a system.

ADDRESS CONTROL TIMING WAVEFORMS



ADDRESS CONTROL TIMING WAVEFORMS (Cont.)

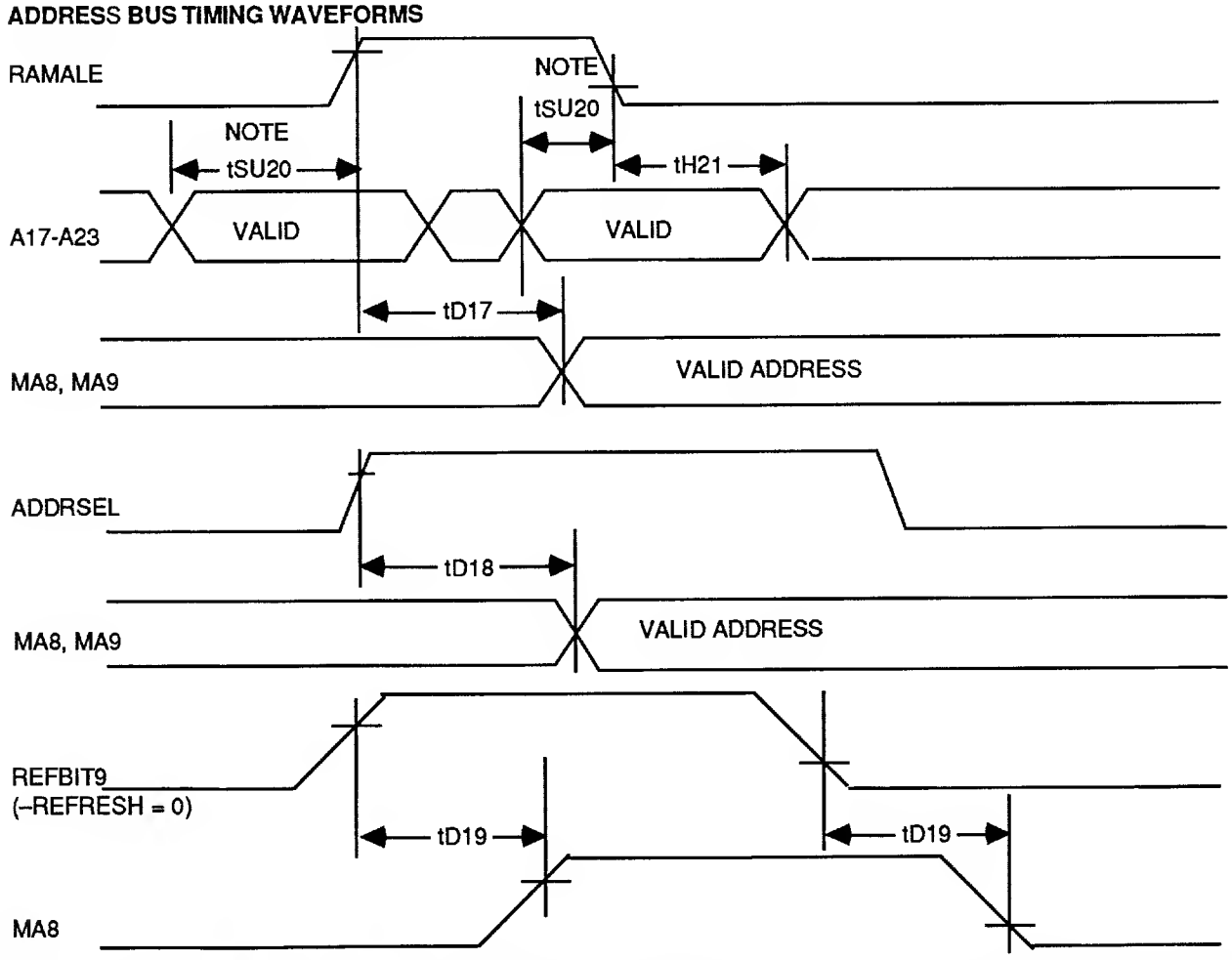


ADDRESS BUS TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tD17	MA8, MA9 Delay from RAMALE		24	ns	CL = 150 pF
tD18	MA8, MA9, Delay from ADDRSEL	6	17	ns	Note, CL = 150 pF
tD19	MA8 Delay from REFBIT9		27	ns	–REFRESH = 0
tSU20	A17-A23 Setup to ALE, RAMALE	45		ns	
tH21	A17-A23 Hold	10		ns	
tD22	XA0/SA0 Delay		35	ns	CL = 50 pF SA0, CL - 100 pF XA0
tD23	SA17-SA19 Delay		40	ns	CL = 200 pF, CPUHLDA = 1, –MASTER = 1
tD24	SA17-SA19 Delay from ALE		35	ns	CL = 200 pF, CPUHLDA = 0
tD25	LA17-LA23 Delay		40		CL = 200 pF, –MASTER = 1
tD26	A17-A23 Delay		40		CL = 50 pF, –MASTER = 0

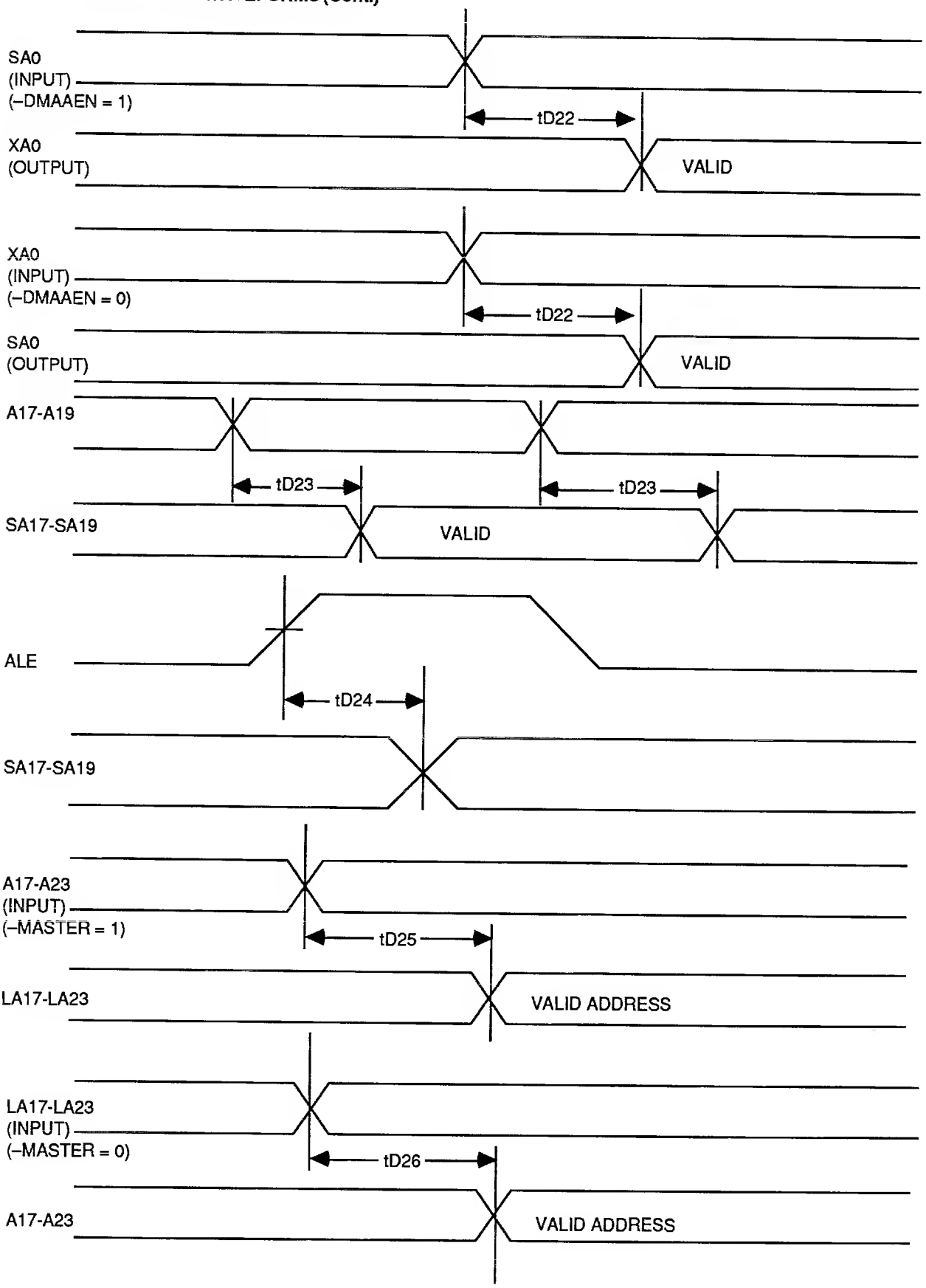
Note: tD18 delay may be derated by a factor of .04 ns/pF for heavier loads.

ADDRESS BUS TIMING WAVEFORMS

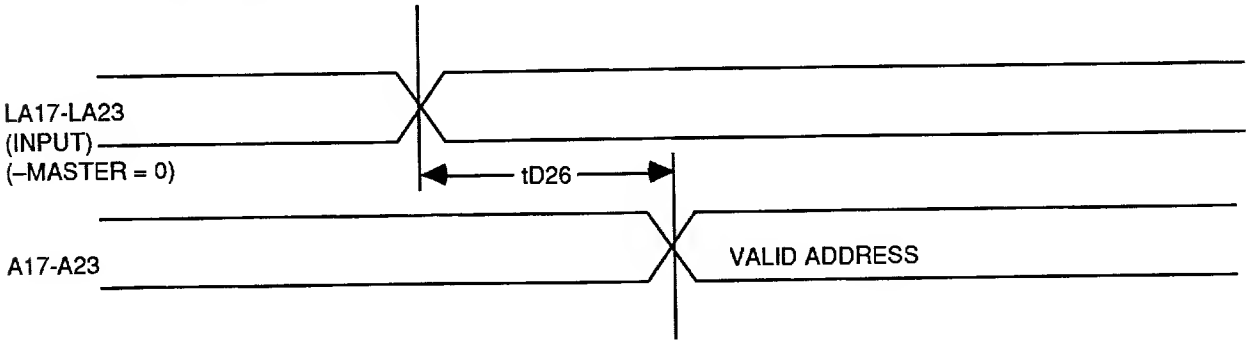


Note: tSU20 is specified with respect to the falling edge of RAMALE to guarantee the correct address decodes will be latched in. tSU20 is shown with respect to the rising edge of RAMALE to show time required for address decodes such that propagation delays tD17 and tD11 will be valid. The time does not have to be met with respect to the rising edge for correct functionality.

ADDRESS BUS TIMING WAVEFORMS (Cont.)



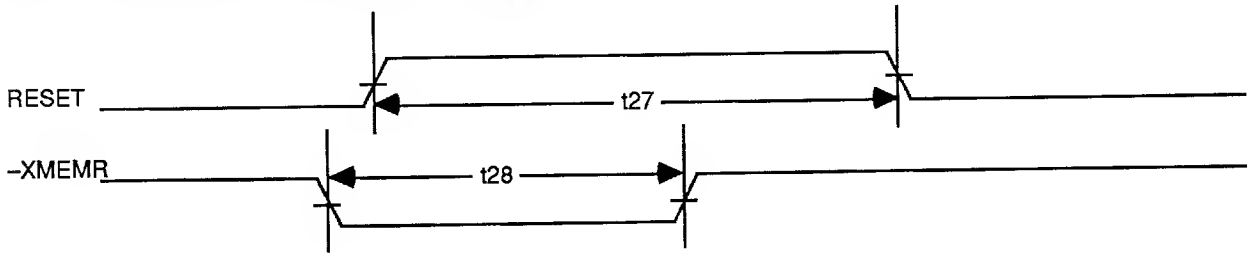
ADDRESS BUS TIMING WAVEFORMS (Cont.)



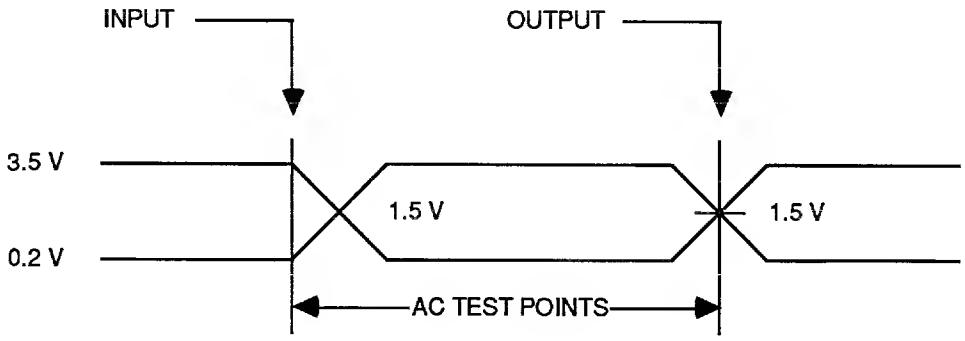
MISCELLANEOUS INPUT TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t27	Min High (Active) Time on RESET	100		ns	
t28	Min Low time for –XMEMR	40		ns	

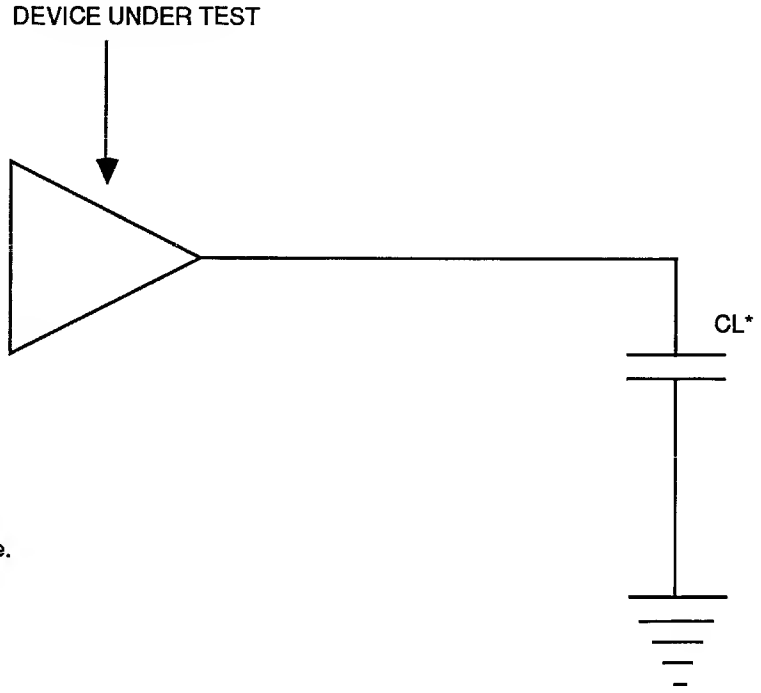
MISCELLANEOUS INPUT TIMING WAVEFORMS



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
27, 29, 50, 54-57, 59-63	200
65, 66	150
28, 32-39	100
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to 7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	SA0, SA17-SA19, AEN, LA17-LA23, IOL = 20 mA
VOL2	Output Low Voltage		0.45	V	MA8, MA9, F16, XA0, XD0-XD7, IOL = 8 mA
VOL3	Output Low Voltage		0.45	V	All Other Pins, IOL = 2 mA
VIH	Input High Voltage	2.0	VDD + 0.5	V	Except –REFRESH
VIL	Input Low Voltage	–0.5	0.8	V	Except –REFRESH
VIHS	Input High Voltage	3.5	VDD + 0.5	V	–REFRESH, Schmitt-trigger
VILS	Input Low Voltage	–0.5	0.6	V	–REFRESH, Schmitt-trigger
CO	Output Capacitance		16	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		25	mA	Note

Note: Inputs = VSS or VDD, outputs are not loaded.

VL82C103A

PC/AT-COMPATIBLE ADDRESS BUFFER

FEATURES

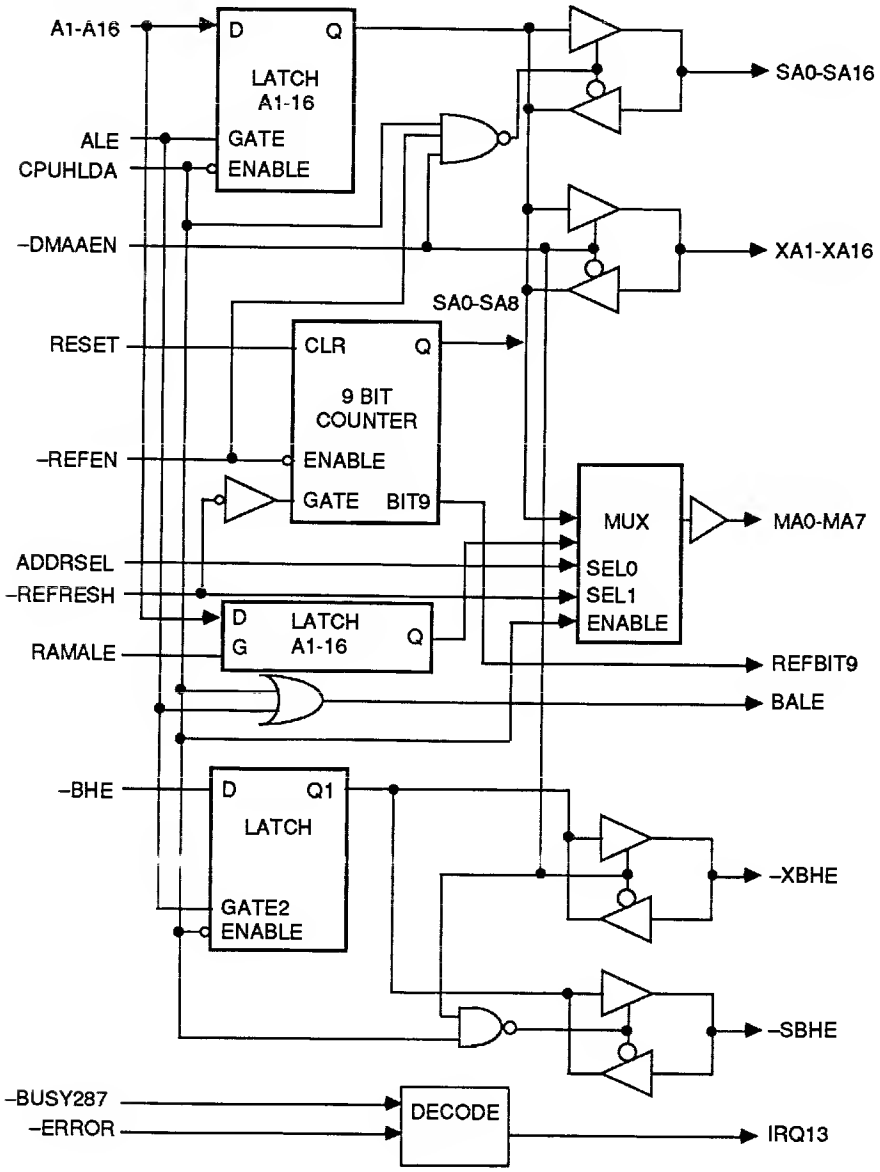
- Fully compatible with IBM PC/AT-type designs
- Completely performs address buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C103A PC/AT-Compatible Address Buffer provides the system with a 16-bit address bus input from the CPU to 41 buffered drivers. The buffered drivers consist of 17 bidirectional system bus drivers, each capable of sinking 20 mA (50 'LS loads) of current and driving 200 pF of capacitance on the backplane; 16 bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and eight memory bus drivers, also capable of sinking 8 mA of current. On-chip refresh circuitry supports both 256K-bit and 1M-bit DRAMs. The VL82C103A provides addressing for the I/O slots as well as the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C103A is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



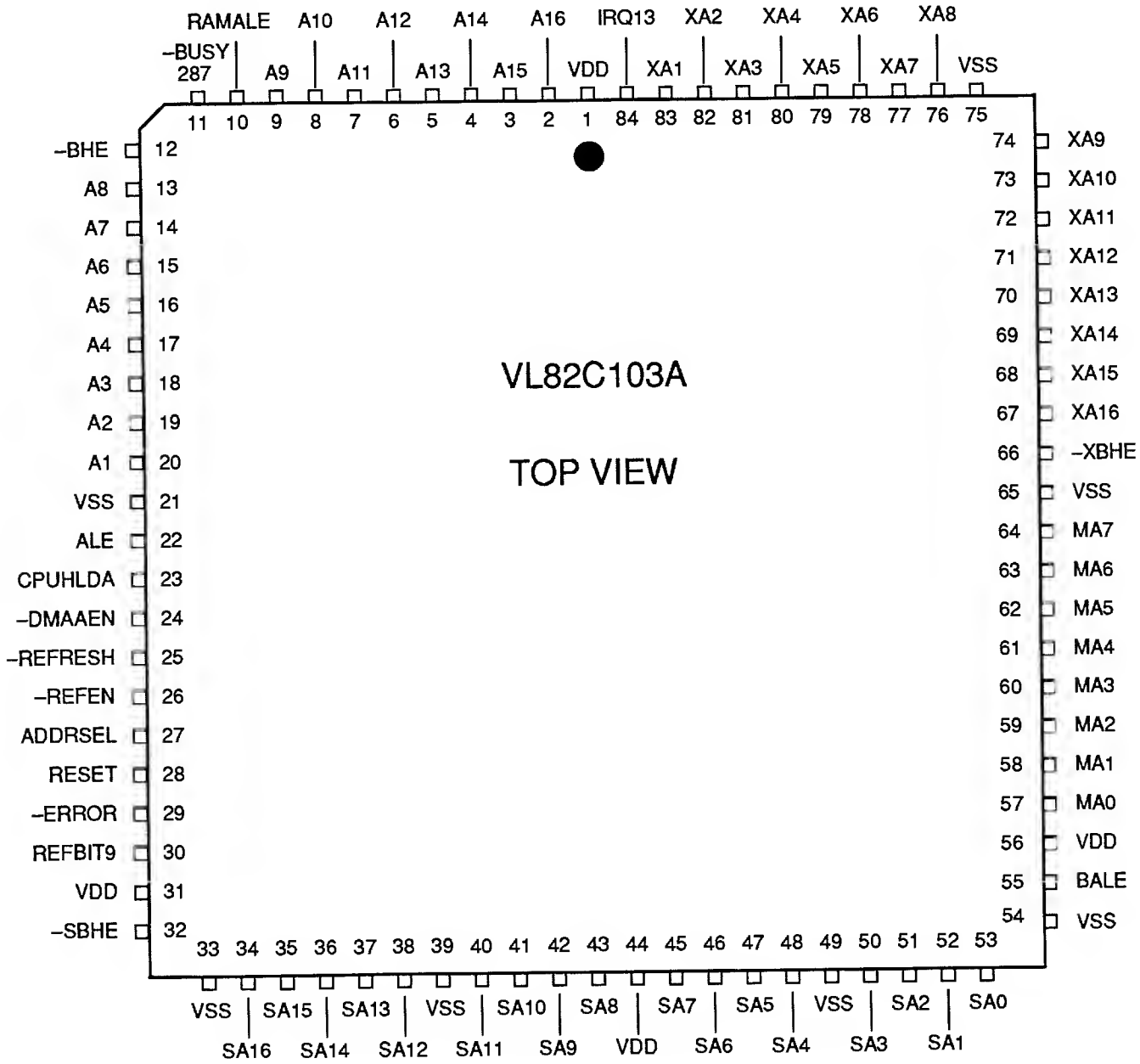
ORDER INFORMATION

Part Number	Package
VL82C103A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

4

PIN DIAGRAM


RAMALE
A10
A12
A14
A16
IRQ13
XA2
XA4
XA6
XA8
-BUSY
287
A9
A11
A13
A15
VDD
XA1
XA3
XA5
XA7
VSS
11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75
-BHE 12
A8 13
A7 14
A6 15
A5 16
A4 17
A3 18
A2 19
A1 20
VSS 21
ALE 22
CPUHLDA 23
-DMAAEN 24
-REFRESH 25
-REFEN 26
ADDRSEL 27
RESET 28
-ERROR 29
REFBIT9 30
VDD 31
-SBHE 32
74 XA9
73 XA10
72 XA11
71 XA12
70 XA13
69 XA14
68 XA15
67 XA16
66 -XBHE
65 VSS
64 MA7
63 MA6
62 MA5
61 MA4
60 MA3
59 MA2
58 MA1
57 MA0
56 VDD
55 BALE
54 VSS
33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
VSS
SA16
SA15
SA14
SA13
SA12
VSS
SA11
SA10
SA9
SA8
VDD
SA7
SA6
SA5
SA4
VSS
SA3
SA2
SA1
SA0
VL82C103A
TOP VIEW

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
A1-A8, A9-A16	20-13 9-2	I	CPU Address Bus Bits 1-16 - The lower 16 bits of the CPU address bits. These are multiplexed to the System Address Bus for the slots SA1-SA16, the Memory Address Bus MA0-MA7 and the Peripheral Address Bus XA1-XA16.
RAMALE	10	I	RAM Address Latch Enable - This positive edge input controls the address latch for the Memory Address bus outputs (MA0-MA7). When used with the System Controller Chip, in FASTMODE, RAMALE will open the memory address latches at the same time a –MEMR or a –MEMW is generated. If FASTMODE is not used, RAMALE is the same as ALE. The memory address latches are open when RAMALE is in the high state.
–BUSY287	11	I	Busy 287 - A busy status input that is asserted by the 80287 to indicate that it is currently executing a command.
–BHE	12	I	Bus High Enable - This is the active low input signal from the 80286 microprocessor which is used to indicate a transfer of data on the upper byte on the data bus, D8-D15.
ALE	22	I	Address Latch Enable - This positive edge input controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle. All latches are open when ALE is in the high state.
CPUHLDA	23	I	CPU Hold Acknowledge - This active high input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
–DMAAEN	24	I	DMA Address Enable - This is an active low input which is active whenever an I/O device is making a DMA access to the system memory.
–REFRESH	25	I	Refresh - An active low input which is used to initiate a refresh cycle for the dynamic RAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle.
–REFEN	26	I	Refresh Enable - An active low input that will be asserted when a refresh cycle is needed for the DRAMs.
ADDRSEL	27	I	Address Select - This is a multiplex select for the Memory Address Bus drivers. When ADDRSEL is low, the lower order address bits are selected. When high, the high order address bits are selected.
RESET	28	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK and used to reset the refresh counter.
–ERROR	29	I	Error - This is an active low input which indicates an error has occurred within the 80287 coprocessor.
REFBIT9	30	O	Refresh Bit 9 - This is the MSB of the refresh counter. When used with the Memory Controller chip a refresh address will be generated for 1M byte DRAMs.
–SBHE	32	I/O	System Bus High Enable - This is the system I/O signal used to indicate transfer of local data on the upper byte on the local data bus, D3-D15. –SBHE is active low and will be in input mode during bus hold acknowledge.
SA0-SA16	53-50, 48-45 43-40, 38-34	O	System Address Bus Bits 0-16 - SA0 will be active only during a refresh cycle otherwise it will be three-stated (input mode).

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BALE	55	O	Buffered Address Latch Enable - An active high output that is used to latch valid addresses and memory decodes from the 80286. System addresses SA0-SA16 are latched on the falling edge of BALE. During a DMA cycle bale is forced active high.
MA0-MA7	57-64	O	DRAM Memory Address Bus Bits 0-7 - This 8-bit output is multiplexed using ADDRSEL to give a full 16-bit address.
XA1-XA16	83-76, 74-67	I/O	Peripheral Address Bus Bits 1-16 - These I/Os are used to control the coprocessor, keyboard, ROM memory and the DMA controllers.
–XBHE	66	I/O	Transfer Byte High Enable - This is an active low I/O used to allow the upper data byte to be transferred through the bus transceivers.
IRQ13	84	O	This is an active high output which indicates an error has occurred within the 80287 coprocessor.
VDD	1, 31, 44, 56		System Supply: 5 V
VSS	21, 33, 39, 49, 54, 65, 75		System Ground

FUNCTIONAL DESCRIPTION

The VL82C103A is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Address Buffer replaces several bus transceivers and address data latches located within the PC/AT-type system. The DRAM refresh circuitry is also located on this device.

The primary function of the Address Buffer is to multiplex the 80286 microprocessor address lines (A1-A16) to the system address bus (SA1-SA16), the peripheral address bus (XA1-XA16), and the memory address bus (MA0-MA7). This is accomplished through two sets of 16-bit wide, positive edge triggered latches and a group of data multiplexors. The two groups of latches can be seen in the block diagram of the device. One set of latches have their output enabled with CPUHLDA and are gated with ALE. This set of latches drive the SA and XA bus outputs. Another parallel set of latches are multiplexed into the MA lines and are gated with RAMALE. RAMALE is an early ALE signal which is generated inside the System Controller chip. When FASTMODE is enabled, RAMALE becomes active as soon as a –MEMR or –MEMW signal is generated (typically one PROCCLK earlier than ALE). This allows more setup time for the address to be multiplexed to the DRAMs. If FASTMODE is not enabled, RAMALE and ALE are identical signals. If the VL82C103A is not used in conjunction with the other PC/AT-devices, RAMALE and ALE should be wired together to provide maximum PC/AT-compatibility.

The device also provides for address flow between the SA, XA, and MA buses and the –XBHE and –SBHE signals. This control flow is arbitrated with the CPUHLDA, –DMAAEN, and –REFEN inputs and is shown in Table1.

Memory addresses are multiplexed from the SA and A bus sources and are controlled via the CPUHLDA, –REFRESH, and ADDRSEL inputs. The mapping and control is shown in Table 2.

A 9-bit refresh counter is provided on this device. This allows support for DRAMs of up to 1M-bit in size. The refresh counter is clocked on the rising edge of the –REFRESH input. A latched register inside the counter latches in the current state of the counter on the falling edge of –REFEN and transfers this value to the internal bus which routes to the SA and MA bus outputs. The SA0 output is provided only for refresh purposes and is driven only during this time. During a refresh the SA and MA bus outputs are driven from the output of the refresh counter latch Q0-Q8. Refer to Table 3 for the mapping of the refresh counter to the bus lines.

Note that all SA bus lines are driven during a refresh cycle. ADDRSEL is not normally toggled during a refresh cycle but is shown in Table 3 for completeness of the logic implementation. The REFBIT9 signal is the Q8 output of the refresh counter. This is output to the Memory Controller chip which controls the upper MA address lines. This is required only for the refresh of 1M-bit DRAMs.

TABLE 1. INTERNAL BUS CONTROL DECODE

CPUHLDA	–DMAAEN	–REFEN	A	SA	XA	MA	–XBHE	–SBHE
0	1	1	I	O	O	O	O	O
1	0	1	I	O	I	O	I	O
1	1	0	I	O	O	O	O	I
1	1	1	I	I	O	O	O	I

I = Input Mode
O = Output Mode

TABLE 2. MEMORY ADDRESS MAPPING

Mux Control Input			MA Bus	
CPUHLDA	–REFRESH	ADDRSEL	MA7	MA0-MA6
1	0	0	SA8	SA1-SA7
1	0	1	SA16	SA9-SA15
0	X	0	A8	A1-A7
0	X	1	A16	A9-A15

X = Don't Care

TABLE 3. REFRESH ADDRESS MAPPING

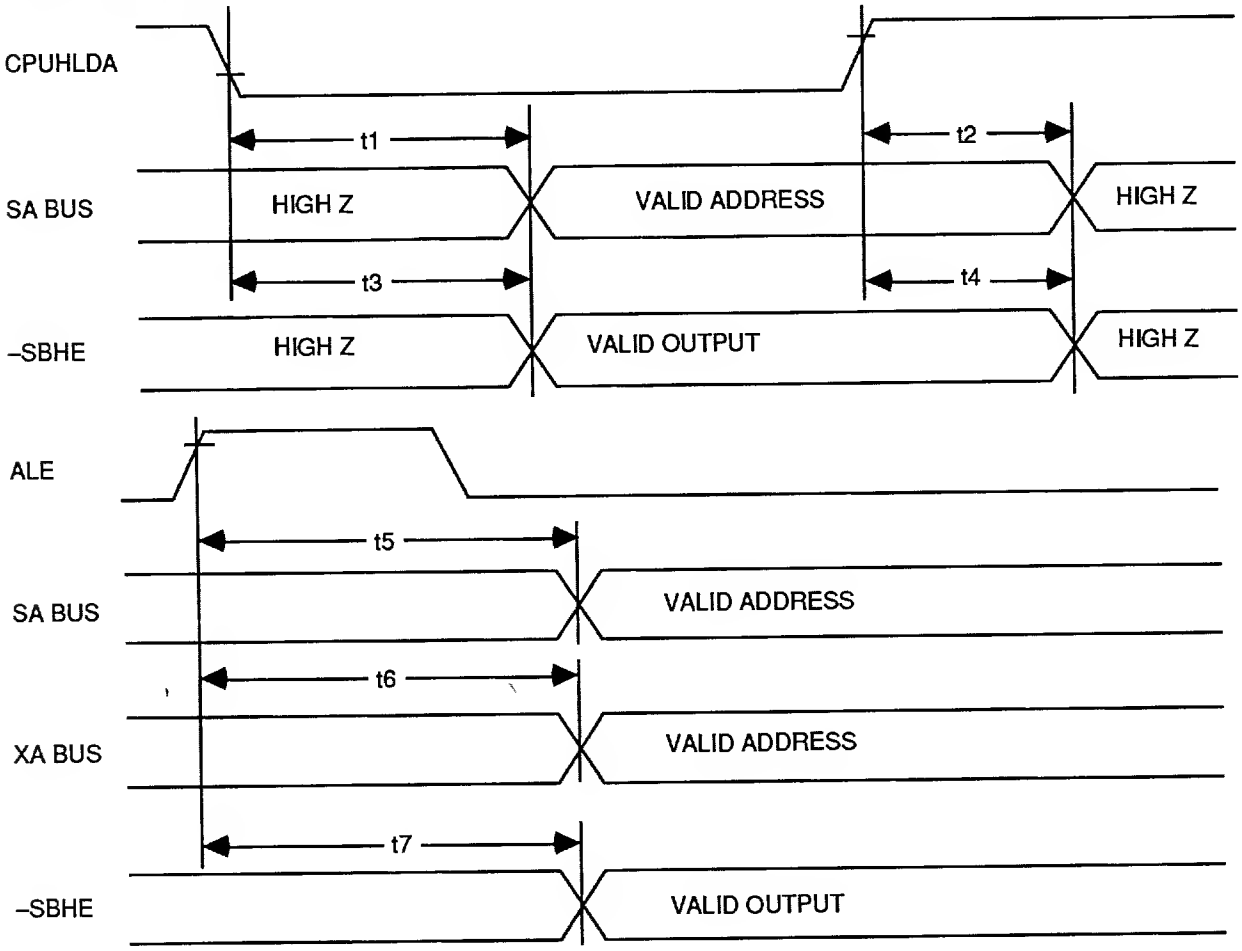
Mux Control Input			MA Bus		SA Bus	
CPU HLDA	–REF EN	ADDR SEL	MA7	MA0-MA6	SA9-SA15	SA0-SA8
1	0	0	Q0	Q1-Q7	0	Q0-Q8
1	0	1	0	0	0	Q0-Q8

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V

CPU MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t1	CPUHLDA to SA Bus from High Z to Valid Add Out		35	ns	
t2	CPUHLDA to SA Bus High Z State		35	ns	
t3	CPUHLDA to –SBHE from High Z to Valid Output		35	ns	
t4	CPUHLDA to –SBHE High Z State		35	ns	
t5	ALE to SA Bus Valid Address		40	ns	CL = 200 pF
t6	ALE to XA Bus Valid Address		40	ns	CL = 100 pF
t7	ALE to –SBHE Bus Valid Address		40	ns	CL = 150 pF

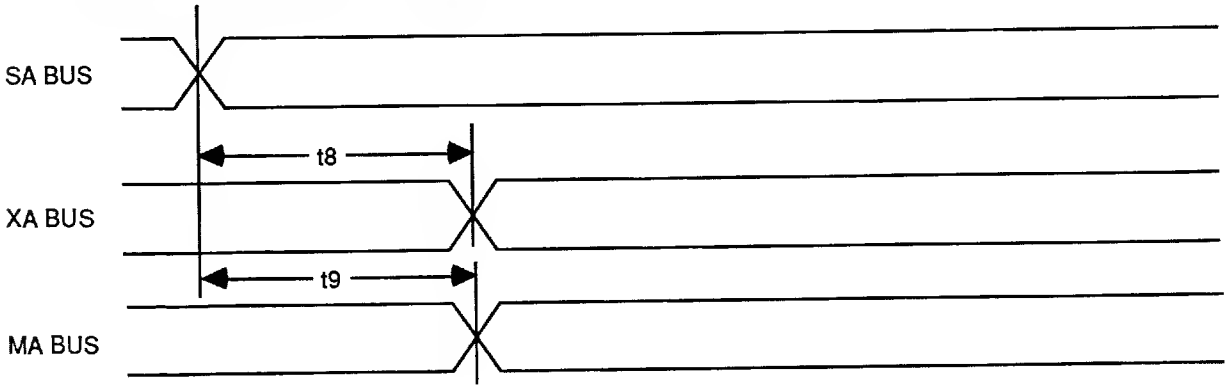
CPU MODE TIMING WAVEFORMS



SYSTEM BUS MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t8	SA Bus In to XA Bus Out		40	ns	CL = 100 pF
t9	SA Bus In to MA Bus Out		40	ns	CL = 150 pF

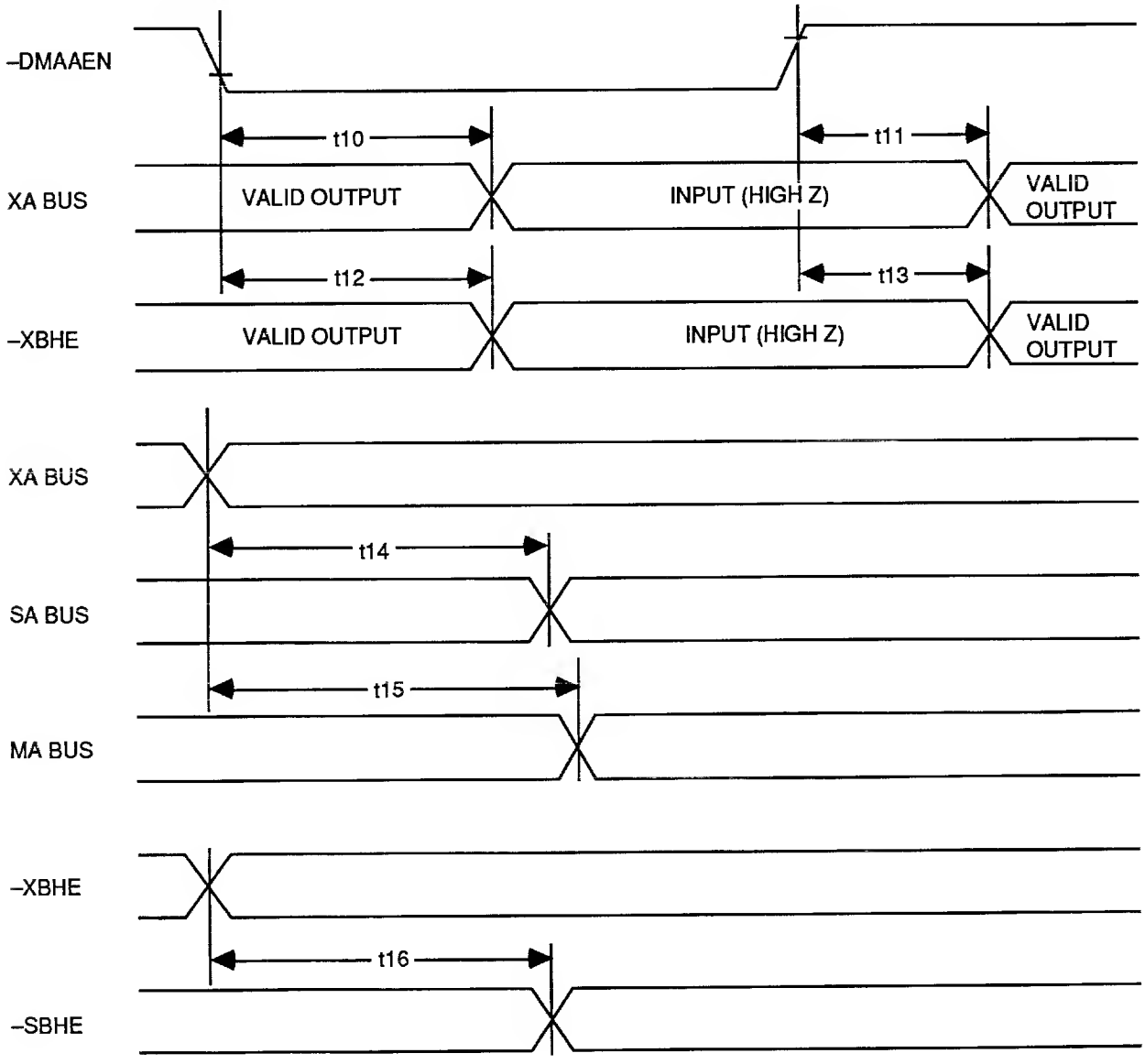
SYSTEM BUS MODE TIMING WAVEFORM



DMA MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t10	–DMAAEN to XA Bus High Z State		35	ns	
t11	–DMAAEN to XA Bus from High Z to Valid Add Out		35	ns	
t12	–DMAAEN to –XBHE High Z State		35	ns	
t13	–DMAAEN to –XBHE from High Z to Valid Output		35	ns	
t14	XA Bus to SA Bus Out		40	ns	CL = 200 pF
t15	XA Bus In to MA Bus Out		40	ns	CL = 150 pF
t16	–XBHE In to –SBHE Out		40	ns	CL = 150 pF

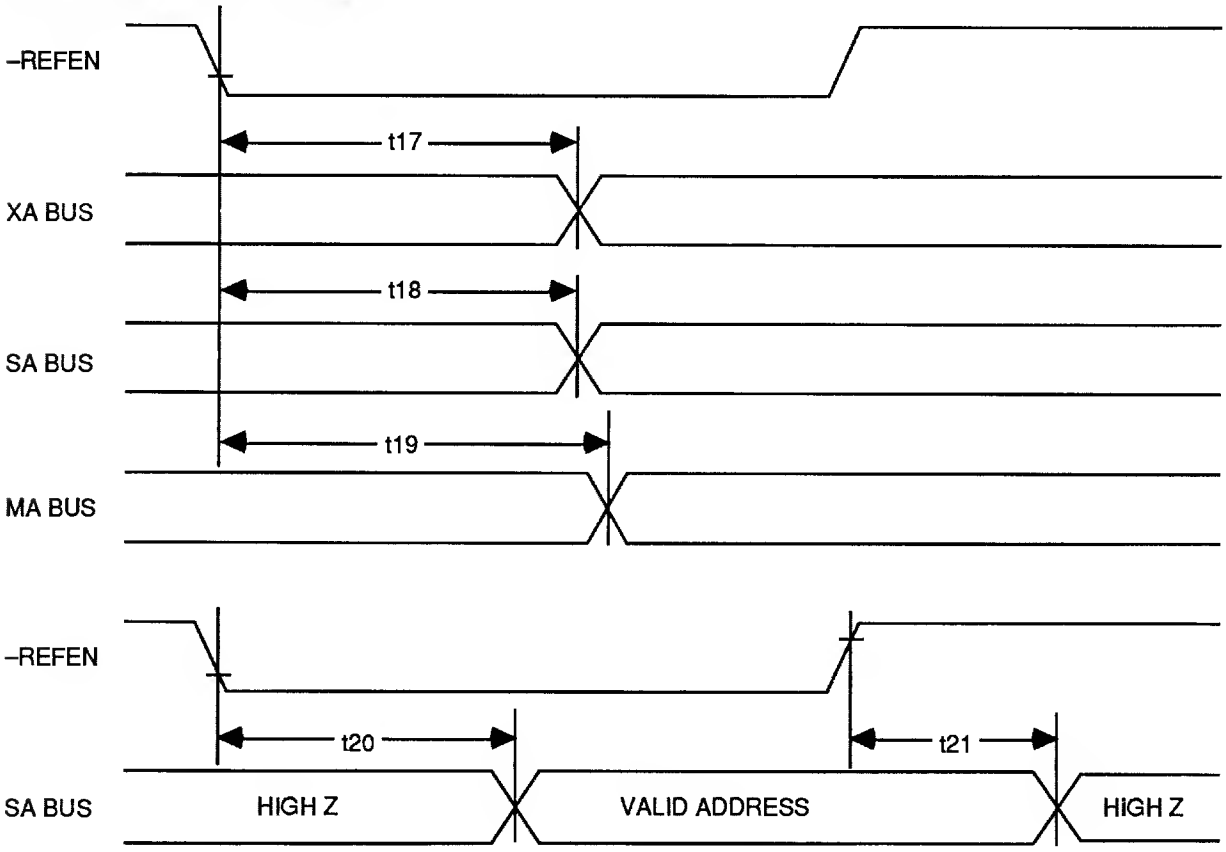
DMA MODE TIMING WAVEFORMS



REFRESH TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t17	–REFEN to XA Bus Valid Add Out		35	ns	CL = 100 pF
t18	–REFEN to SA Bus Valid Add Out		35	ns	CL = 200 pF
t19	–REFEN to MA Bus Valid Add Out		35	ns	CL = 150 pF
t20	–REFEN to SA Bus from High Z to Valid Add Out		35	ns	
t21	–REFEN to SA Bus High Z Out		35	ns	

REFRESH TIMING WAVEFORMS

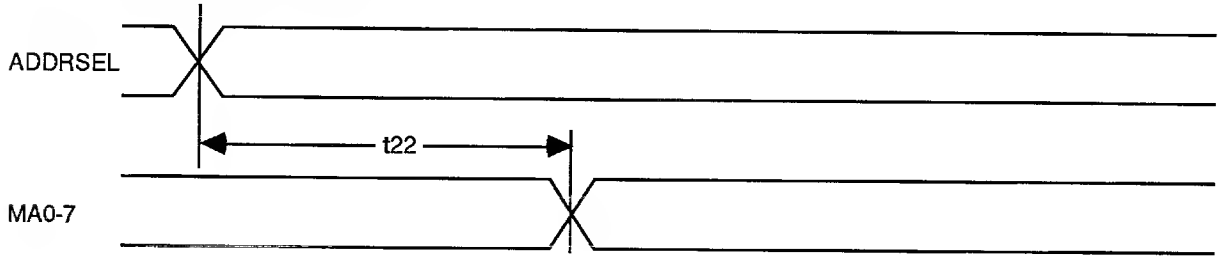


ADDRESS TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t22	ADDRSEL to MA Bus Out	6	17	ns	CL = 150 pF

Note: t22 delay may be derated by a factor of .04 ns/pF for heavier loads.

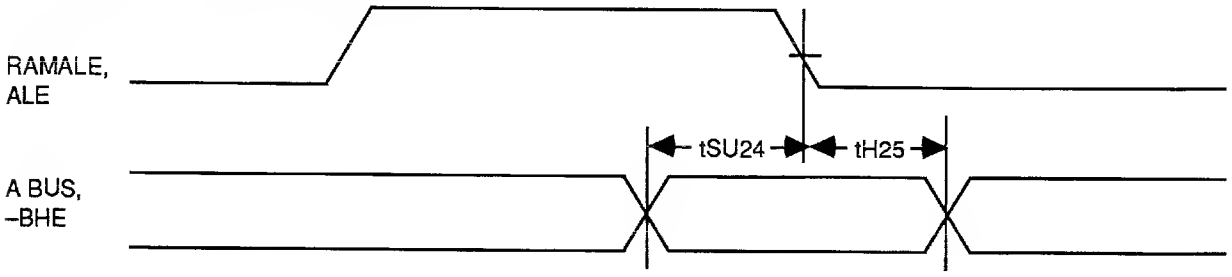
ADDRESS TIMING WAVEFORM



SETUP & HOLD TIMING

Symbol	Parameter	Min	Max	Unit	Condition
tSU23	A Bus to RAMALE and –BHE to ALE Setup Timing	10		ns	
tH24	A Bus to RAMALE and –BHE to ALE Hold Timing	10		ns	

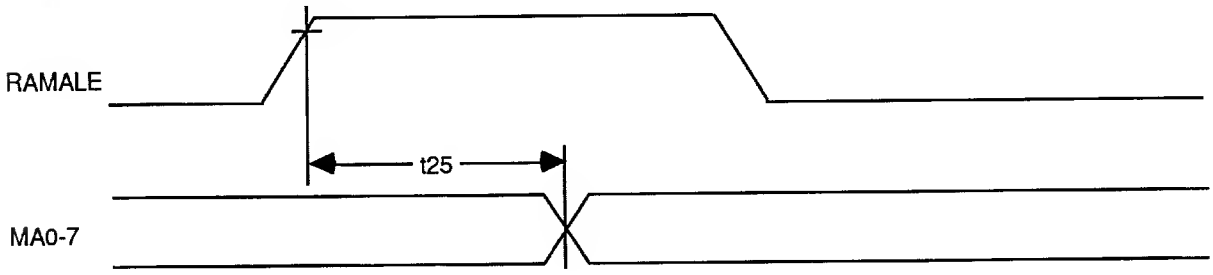
SETUP & HOLD TIMING WAVEFORM



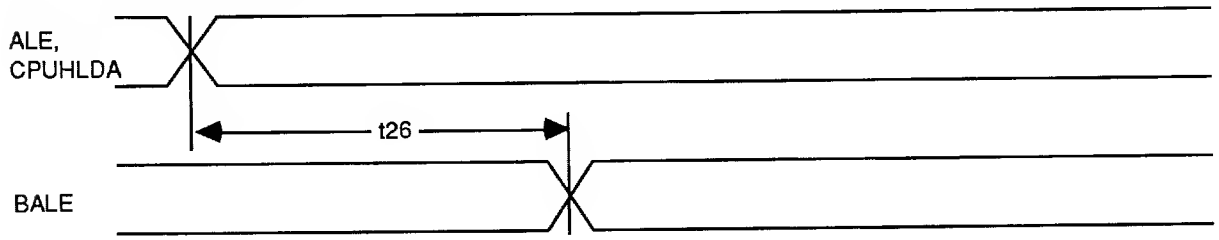
RAMALE, BALE & IRQ13 TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t25	RAMALE to MA Bus Out		24	ns	CL = 150 pF
t26	ALE, CPUHLDA to BALE Out		25	ns	CL = 200 pF
t27	–ERROR, –BUSY287 to IRQ13 Out		25	ns	CL = 50 pF
t28	–XBHE Valid from ALE		22	ns	CL = 100 pF

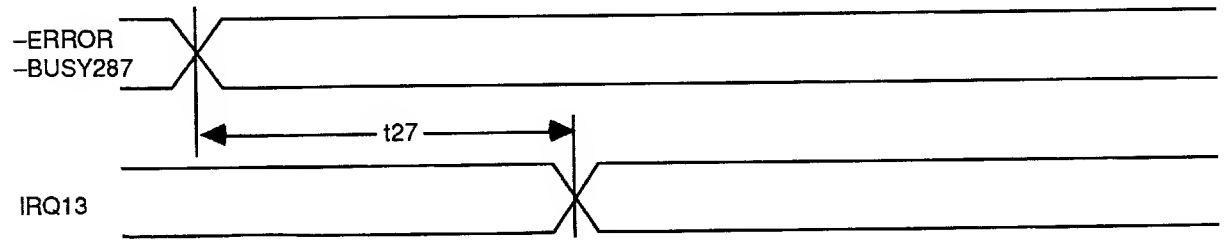
RAMALE TIMING WAVEFORM



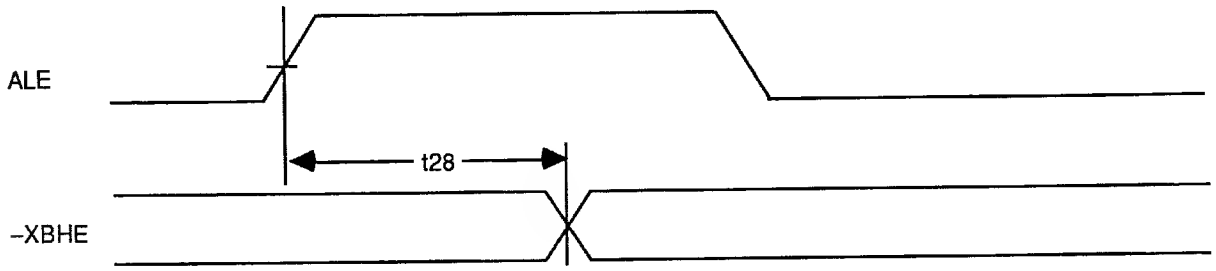
BALE TIMING WAVEFORM



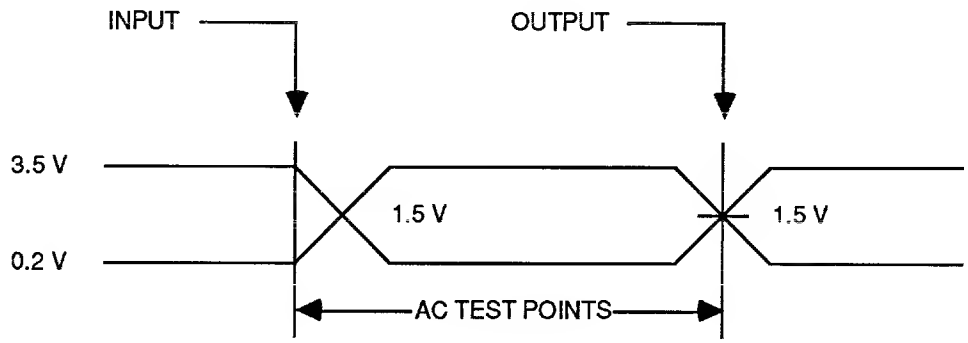
IRQ13 TIMING WAVEFORM



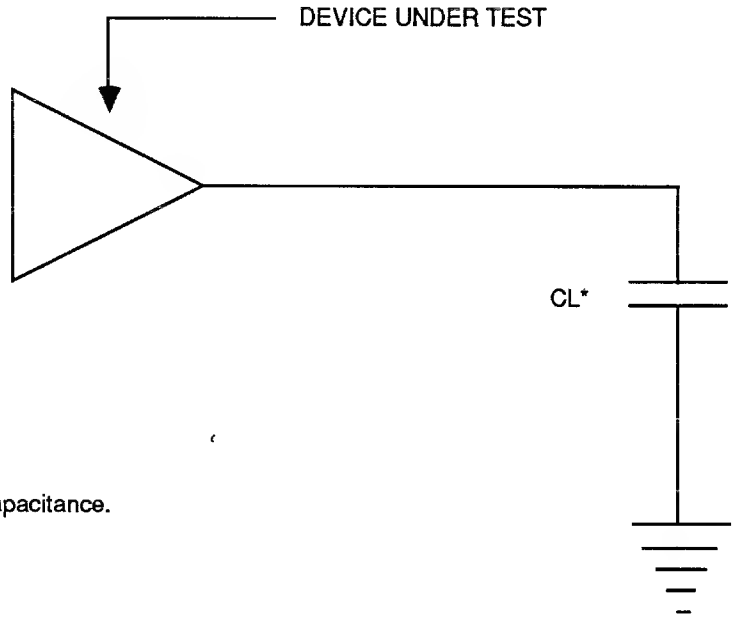
–XBHE TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
32, 34-38, 40-43, 45-48, 50-53, 55	200
57-64, 66	150
67-74, 76-83	100
	75
84, 30	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to 7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

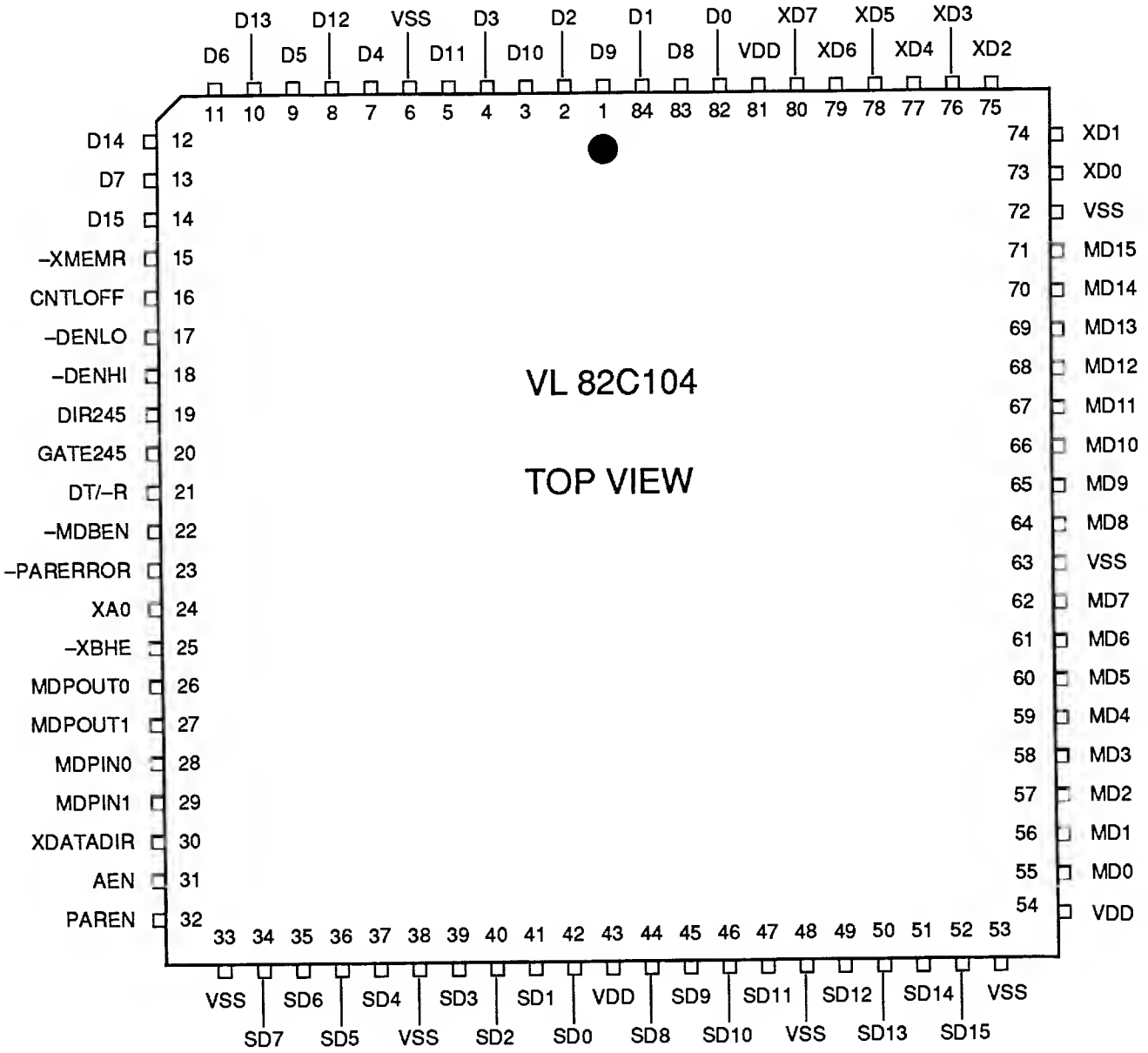
Stresses above those listed may cause permanent damage to the device. These are stress ratings only. functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 20 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	ALE, RAMALE
VILC	Input Low Voltage	–0.5	0.6	V	ALE, RAMALE
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		20	mA	

Notes: 1. Pins 57-64, 66-74, and 76-83.
2. Pins 32, 34-38, 40-43, 45-48, and 50-53, 55.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

PIN DIAGRAM


D13 D12 VSS D3 D2 D1 D0 XD7 XD5 XD3
D6 D5 D4 D11 D10 D9 D8 VDD XD6 XD4 XD2
11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75
D14 12
D7 13
D15 14
–XMEMR 15
CNTLOFF 16
–DENLO 17
–DENHI 18
DIR245 19
GATE245 20
DT/–R 21
–MDBEN 22
–PARERROR 23
XA0 24
–XBHE 25
MDPOUT0 26
MDPOUT1 27
MDPIN0 28
MDPIN1 29
XDATADIR 30
AEN 31
PAREN 32
74 XD1
73 XD0
72 VSS
71 MD15
70 MD14
69 MD13
68 MD12
67 MD11
66 MD10
65 MD9
64 MD8
63 VSS
62 MD7
61 MD6
60 MD5
59 MD4
58 MD3
57 MD2
56 MD1
55 MD0
54 VDD
VL 82C104
TOP VIEW
33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
VSS SD6 SD4 SD3 SD1 VDD SD9 SD11 SD12 SD14 VSS
SD7 SD5 VSS SD2 SD0 SD8 SD10 VSS SD13 SD15

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CNTLOFF	16	I	CNTLOFF - This input is used as a clock to latch the current data on the low byte of the system data bus. Data is latched on the rising edge of CNTLOFF and is independent of the status of DT/–R, XA0, or –DENLO.
DT/–R	21	I	Data Transmit (high)/Receive (low) - This input is a signal from the 82C288. It establishes the direction of data flow to or from the system data bus.
–DENLO	17	I	Data Enable Low - An active low input that enables a low byte data transfer on the CPU data bus low byte transceiver.
XA0	24	I	Peripheral Address Bus Bit 0 - This is the LSB of the peripheral address bus. The signal is used throughout the system to indicate low or high byte data transfers. It is used to enable the low byte memory data transceiver and to select latched or immediate data out of the CPU low byte bus transceiver. It is also used to enable low byte parity checking.
–MDBEN	22	I	Memory Data Bus Enable - An active low input that is used to set the direction of the memory data bus transceiver. –MDBEN = 0 indicates a memory write cycle while –MDBEN = 1 is a memory read cycle.
XDATADIR	30	I	Transceiver Data Direction - This input is used to select the direction of the peripheral data bus transceiver. XDATADIR = 0 indicates a DMA write to the system data bus while XDATADIR = 1 is used for a DMA read from the system data bus.
AEN	31	I	Address Enable - An active high input that is used to disable the DMA data bus transceiver while the DMA controller is using the peripheral data bus for address information.
DIR245	19	I	Direction 245 - An input control signal used to set the direction of the high/low system data bus transceiver. This is used for high to low, or low to high data byte moves.
GATE245	20	I	Gate 245 - An active low input that enables the high/low system data transceiver.
–DENHI	18	I	Data Enable High - An active low input that enables a high byte data transfer on the CPU data bus high byte transceiver.
–XBHE	25	I	Transfer Bus High Enable - An active low that indicates a transfer of data on the upper byte of the memory data bus. It is used to enable the high byte memory data tranceiver and to enable high byte parity checking.
–XMEMR	15	I	Memory Read Enable - An active low input signal that indicates when a memory read cycle is occurring. It is used to disable the MDPOUTx signals during a memory write and to latch in the detected parity error signal during a memory read.
MDPOUT0	26	I	Memory Data Parity Out 0 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the low byte of data read from memory.
MDPOUT1	27	I	Memory Data Parity Out 1 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the high byte of data read from memory.
MDPIN0	28	O	Memory Data Parity In 0 - An active high output that is the parity input to the system board memory. It is generated from the current low byte data on the memory data bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MDPIN1	29	O	Memory Data Parity In 1 - An active high output that is the parity input to the system board memory. It is generated from the current high byte data on the memory data bus.
PAREN	32	I	Parity Enable - This active high input is used to enable the parity data latch. It is used to prevent false parity errors when ROM memory access occur.
–PARERROR	23	O	Parity Error - An active low output that is used to indicate that a memory parity error has occurred. This signal is latched by –XMEMR and is valid until the next memory access.
MD0-MD15	55-62, 64-71	I/O	DRAM Memory Data bus bits 0-15 - These are I/O signals.
XD0-XD7	73-80	I/O	Peripheral Data Bus Bits 0-7 - I/O's used to control the coprocessor, keyboard, ROM memory and the DMA controllers.
D0-D15	82, 84, 2, 4, 7, 9,11,13 83,1, 3, 5, 8 10,12,14	I/O	CPU Data Bus Bits 0-15 - This is a bidirectional bus controlled by the DT/–R input.
SD0-SD15	42-39, 37-34 44-47, 49-52	I/O	System Data Bus Bits 0-15 - These are I/O signals.
VDD	43, 54, 81		System Power: 5 V
VSS	6, 33, 38, 48 53, 63, 72		System Ground

FUNCTIONAL DESCRIPTION

The VL82C104 is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Data Buffer replaces several bus transceivers and a CPU lower byte data latch located within the PC/AT-type system.

The primary function of the Data Buffer is to multiplex the 80286 microprocessor data lines D0-D15 to the system data bus SD0-SD15, the peripheral data bus XD-XD17 and the memory data bus MD0-MD15. This is accomplished through six sets of 8-bit wide data multiplexors. The lower data byte of the CPU data bus transceiver has a byte wide register which is clocked by the rising edge of CNTLOFF. The data is latched in the direction from the System Data Bus to the CPU Data bus only. XA0 is used to control data flow to the CPU Data Bus. When XA0 = 0, real time data is passed to the CPU data bus. When XA0 = 1, latched data is passed to the CPU Data Bus. The six groups of transceivers can be seen in the block diagram of the device. The data parity encoder/decoder logic is also located within this device. All data present upon the memory data bus passes through the parity logic. The outputs of the parity encoder/decoders, MDPIN0 and MDPIN1, are enabled via PAREN to prevent decoding a ROM access and are gated with –XMEMR. The –PARERROR signal is fed back to the Memory Controller chip where it is gated with other logic to produce the NMI signal for the 80286.

The logic controlling the bus transceivers has been optimized for speed and as such there are no provisions to prevent internal bus collisions. In a standard PC/AT type application using the full VL82CPCAT chip set this is not a problem as the control signals which enable the transceivers are decoded in such a fashion as to prevent this from happening. In the case where only the VL82C104 is used care must be taken as to ensure that the control signals will not cause an internal bus collision. From the block diagram it can be seen that every bus transceiver has an A and B I/O port. The DIR input to the transceiver controls the direction of data flow through the transceiver. A high (1) input into the DIR pin causes data to flow from A to B. A low (0) causes data to flow from B to A. All transceiver enables are low true causing the output of the particular transceiver to be active.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

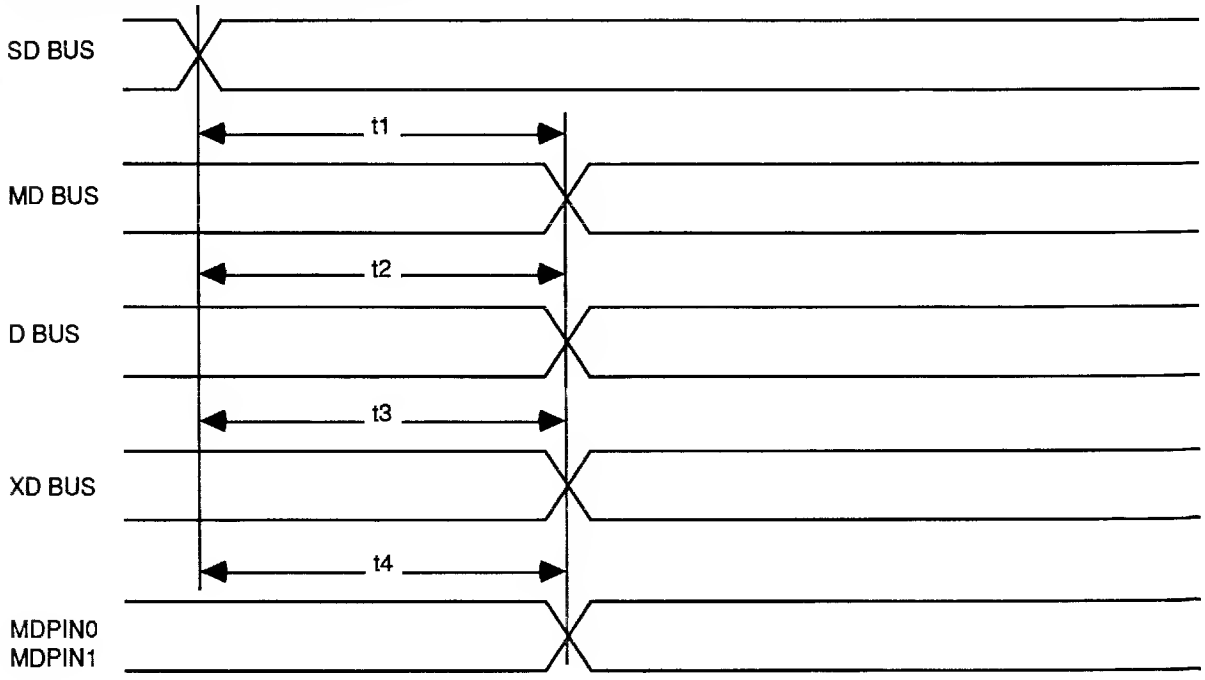
DATA BUS I/O MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t1	SD Bus In to MD Bus Out		40	ns	CL = 100 pF
t2	SD Bus In to D Bus Out		40	ns	CL = 50 pF
t3	SD Bus In to XD Bus Out		40	ns	CL = 100 pF
t4	SD Bus In to MDPIN0 and MDPIN1 Out		55	ns	CL = 50 pF
t5	D Bus In to MD Bus Out		30	ns	CL = 100 pF
t6	D Bus In to SD Bus Out		35	ns	CL = 200 pF
t7	D Bus In to XD Bus Out		30	ns	CL = 100 pF
t8	D Bus In to MDPIN0 and MDPIN1 Out		55	ns	CL = 50 pF
t9	MD Bus In to D Bus Out		19	ns	CL = 50 pF
t10	MD Bus In to SD Bus Out		35	ns	CL = 200 pF
t11	MD Bus In to XD Bus Out		30	ns	CL = 100 pF
t12	XD Bus In to D Bus Out		50	ns	CL = 50 pF
t13	XD Bus In to SD Bus Out		50	ns	CL = 200 pF
t14	XD Bus In to MD Bus Out		50	ns	CL = 100 pF
t15	XD Bus In to MDPIN0, MDPIN1 Out		45	ns	CL = 50 pF, Note

Note: This function is not available in a standard PC/AT system. It is specified here because the system can be configured to accommodate this function, although it is not tested for.

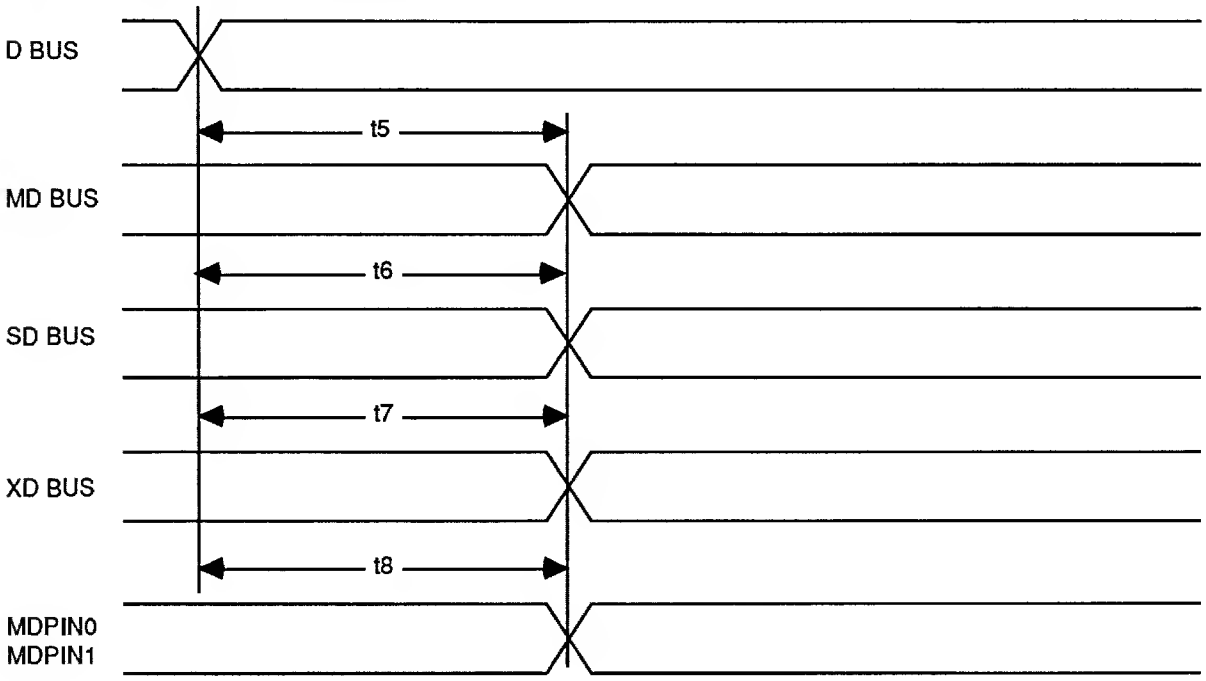
DATA BUS I/O MODE TIMING WAVEFORMS

System Data Bus Timing Waveform

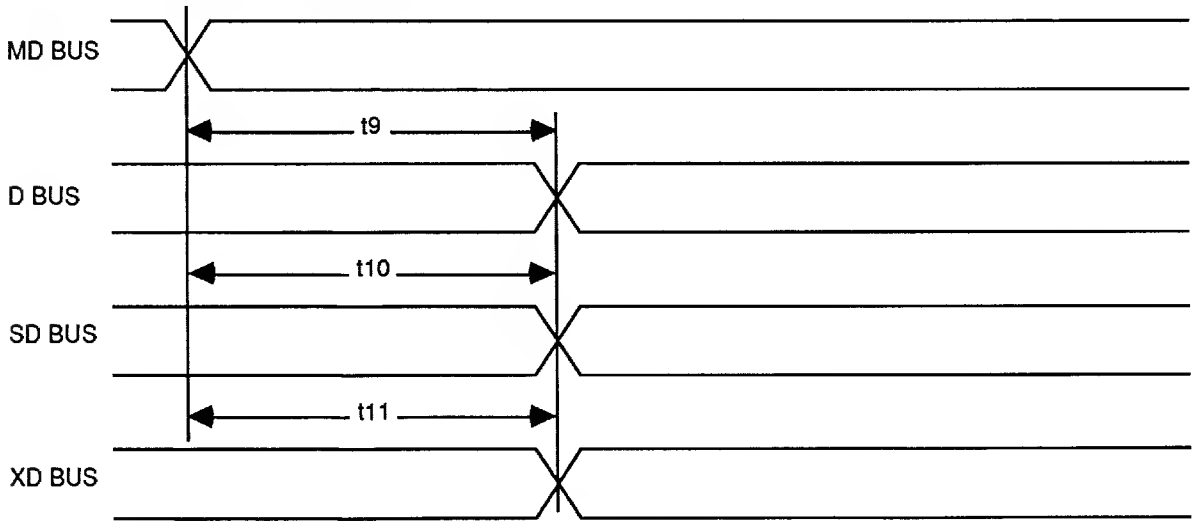


DATA BUS I/O MODE TIMING WAVEFORMS (Cont.)

CPU Data Bus Input Timing Waveform

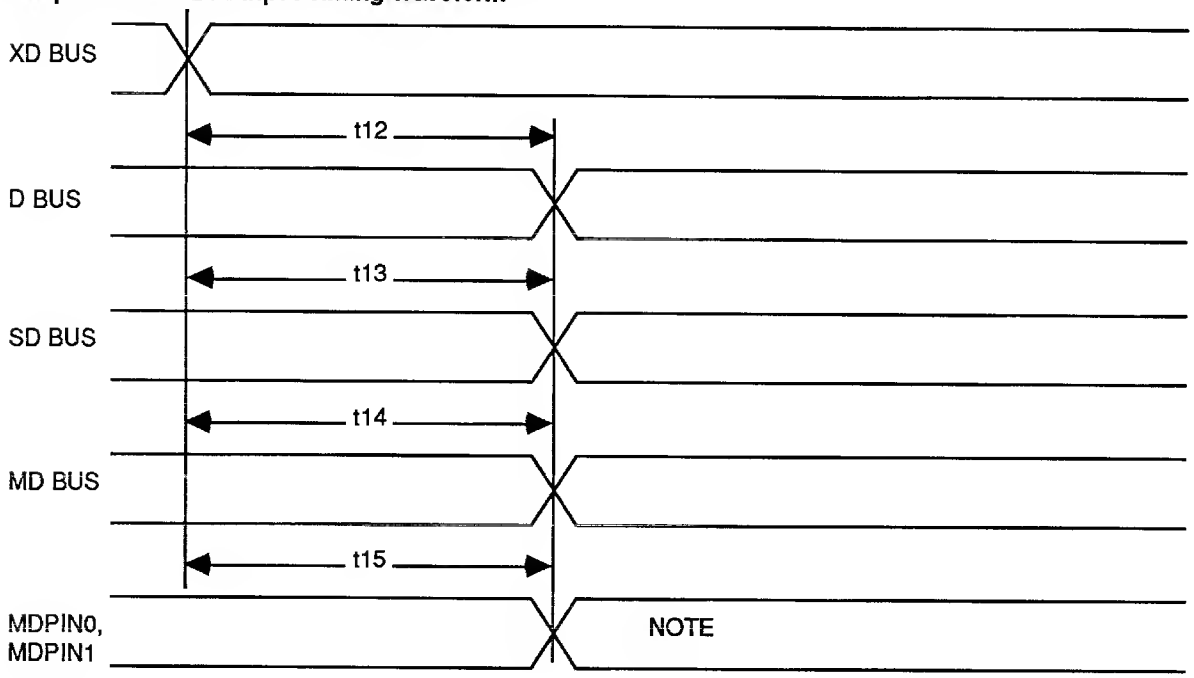


Memory Data Bus Input Timing Waveform



DATA BUS I/O MODE TIMING WAVEFORMS (Cont.)

Peripheral Data Bus Input Timing Waveform

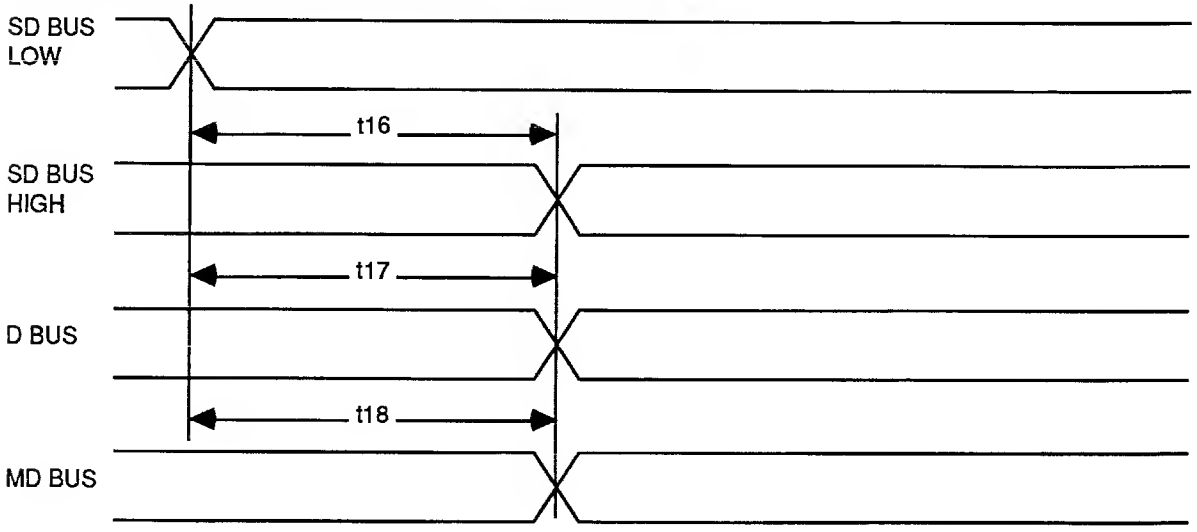


Note: This function is not available in a standard PC/AT system. It is specified here because the system can be configured to accommodate this function, although it is not tested for.

LOW BYTE TO HIGH BYTE CONVERSION MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t16	SD Low to SD High Data Out		55	ns	CL = 200 pF
t17	SD Low to D Bus High Data Out		45	ns	CL = 50 pF
t18	SD Low to MD Bus High Data Out		45	ns	CL = 100 pF

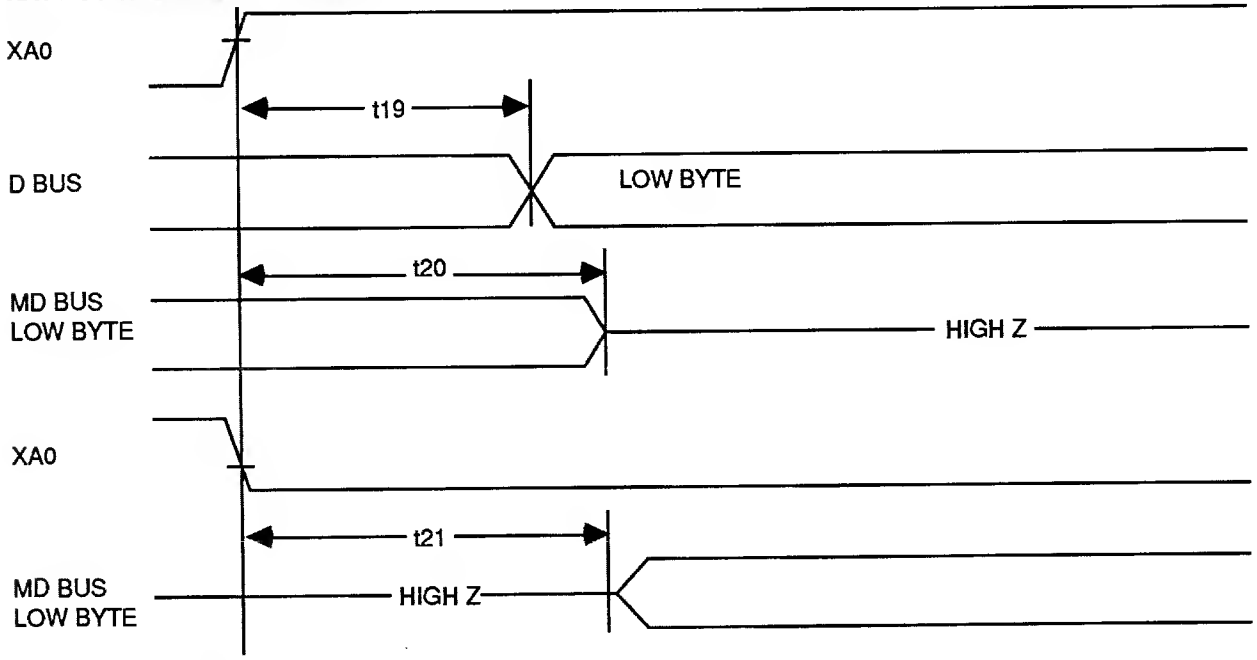
LOW BYTE TO HIGH BYTE CONVERSION TIMING WAVEFORM



XA0 BUS MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t19	XA0 to D Bus Data Out		30	ns	CL = 50 pF
t20	XA0 to MD Bus Low Byte Out to High Z		35	ns	
t21	XA0 to MD Bus Low Byte Out from High Z		35	ns	

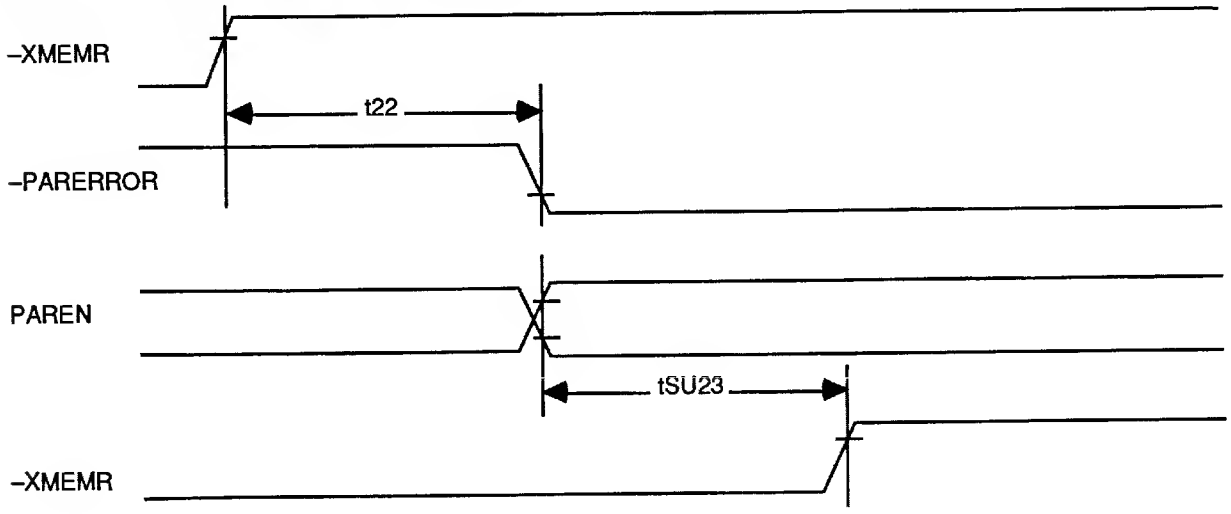
XA0 BUS TIMING WAVEFORM



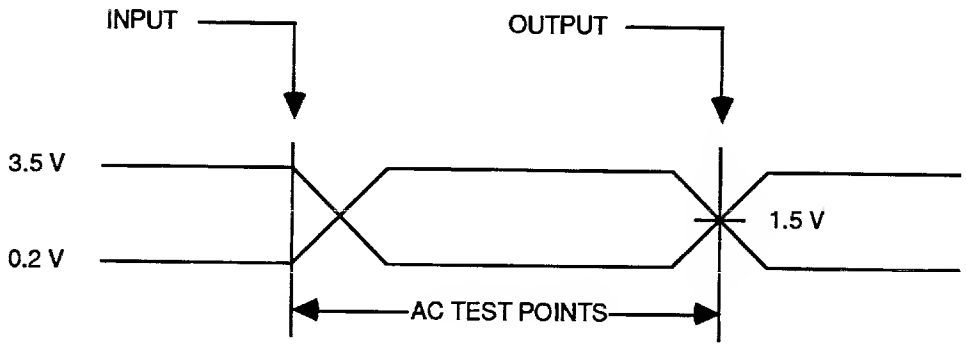
MEMORY READ MODE TIMING

Symbol	Parameter	Min	Max	Unit	Condition
t22	–XMEMR High to –PARERROR Out		25	ns	CL = 50 pF
tSU23	Setup PAREN to –XMEMR High	15		ns	

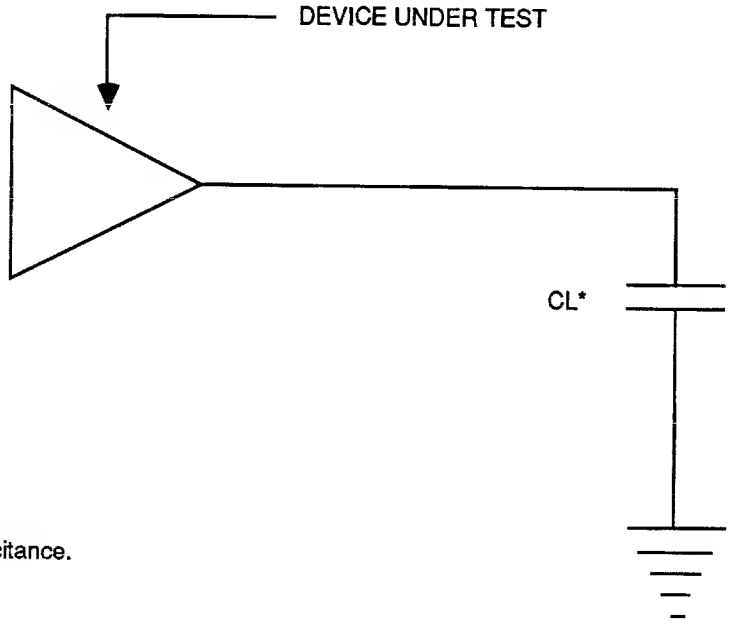
MEMORY READ MODE TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
34-37, 39-42, 44-47, 49-52	200
55-62, 64-71, 73-80	100
1-5, 7-14, 23, 28-29	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 20 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	CNTLOFF
VILC	Input Low Voltage	–0.5	0.6	V	CNTLOFF
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		100	mA	

Notes: 1. Pins 55-62, 64-71, and 73-80.
2. Pins 34-37, 39-42, 44-47, and 49-52.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

VL82C104

PC/AT-COMPATIBLE DATA BUFFER

FEATURES

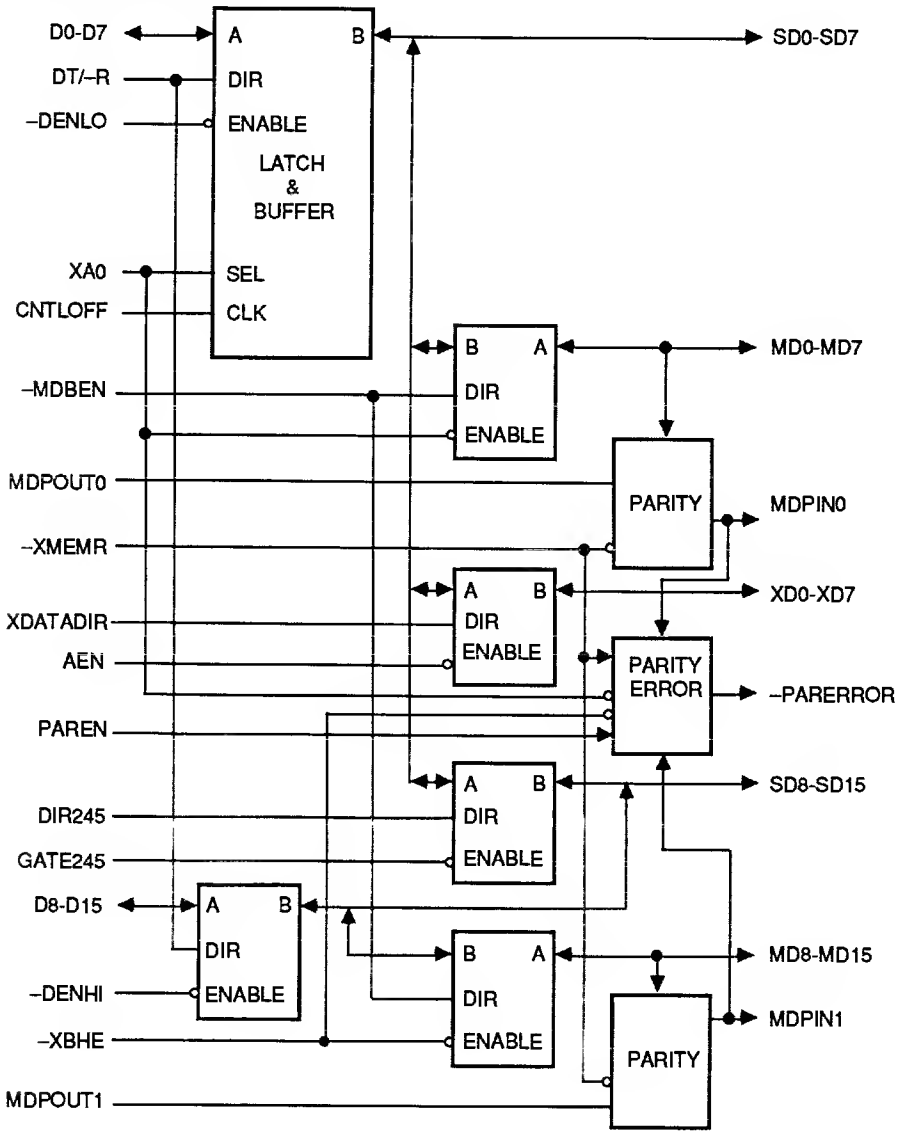
- Fully compatible with IBM PC/AT-type designs
- Completely performs data buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 12 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C104 PC/AT-Compatible Data Buffer provides a 16-bit CPU data bus I/O as well as 40 buffered drivers. The buffered drivers consist of 16 bidirectional system data bus drivers, each capable of sinking 20 mA (50 'LS loads) of current; eight bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and 16 memory data bus drivers, each capable of sinking 8 mA (20 'LS loads) of current. The VL82C104 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C104 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C104-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

4

VL82C201

PC/AT-COMPATIBLE SYSTEM CONTROLLER

FEATURES

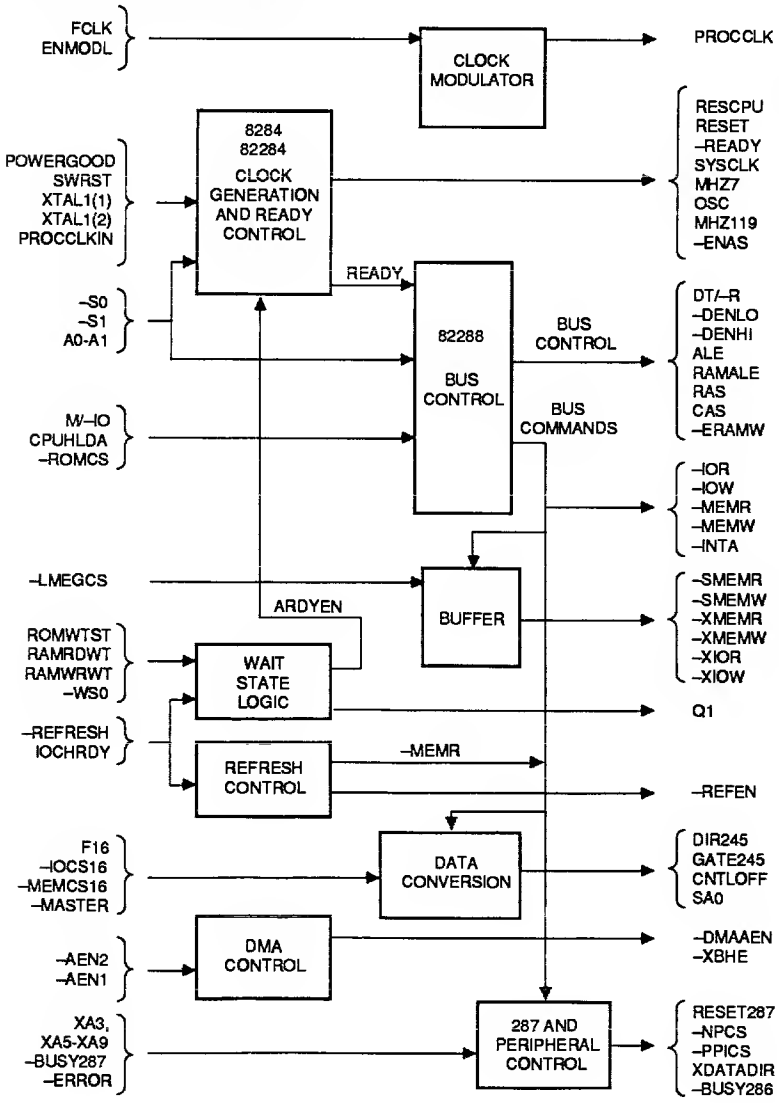
- Fully compatible with IBM PC/AT-type designs
- Replaces 36 integrated circuits on the PC/AT-type board
- Supports 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Sink 24 mA on slot driver outputs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C201 PC/AT-Compatible System Controller replaces an 82C284 Clock Controller and an 82C288 Bus Controller (both are used in '286-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately 30 other less complex integrated circuits used as wait state logic. The device accepts a user supplied PROCCLK or generates its own using an internal clock modulation circuit. It also accepts a 14.318 MHz crystal to control the video clock and supplies reset and clock signals to the I/O slots.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C201 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



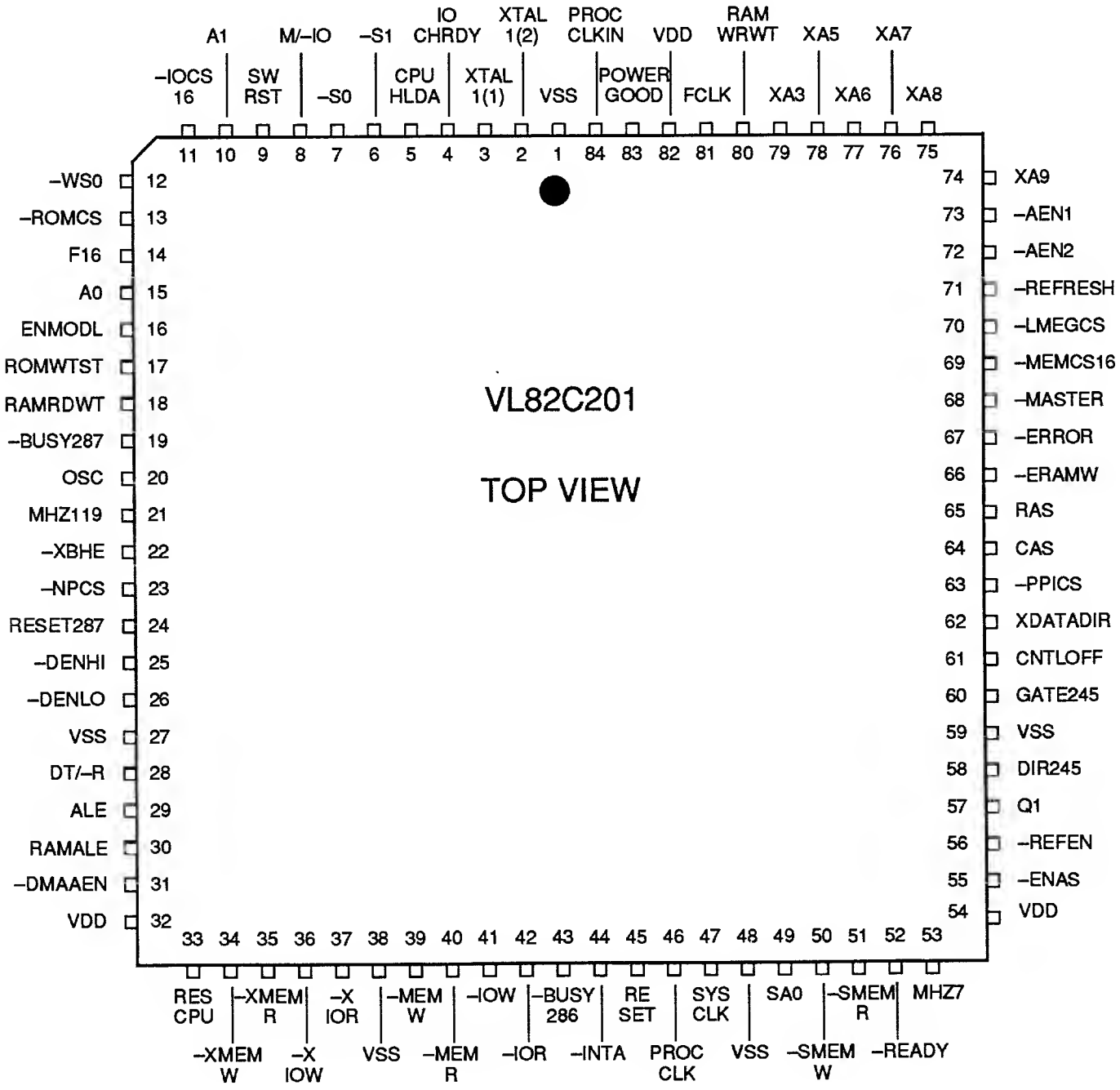
ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C201-16QC VL82C201-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C201-20QC VL82C201-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature:
QC = 0°C to +70°C
QI = –40°C to +85°C.

4

PIN DIAGRAM


VL82C201
TOP VIEW
1 A1
2 M/–IO
3 –S1
4 IO CHRDY
5 XTAL 1(2)
6 PROC CLKIN
7 VDD
8 RAM WRWT
9 XA5
10 XA7
11 –IOCS 16
12 SW RST
13 –S0
14 CPU HLDA
15 XTAL 1(1)
16 VSS
17 POWER GOOD
18 FCLK
19 XA3
20 XA6
21 XA8
22 –WS0
23 –ROMCS
24 F16
25 A0
26 ENMODL
27 ROMWTST
28 RAMRDWT
29 –BUSY287
30 OSC
31 MHZ119
32 –XBHE
33 –NPCS
34 RESET287
35 –DENHI
36 –DENLO
37 VSS
38 DT/–R
39 ALE
40 RAMALE
41 –DMAAEN
42 VDD
43 RES CPU
44 –XMEM R
45 –X IOR
46 –MEM W
47 –IOW
48 –BUSY 286
49 RE SET
50 SYS CLK
51 SA0
52 –SMEM R
53 MHZ7
54 VDD
55 –ENAS
56 –REFEN
57 Q1
58 DIR245
59 VSS
60 GATE245
61 CNTLOFF
62 XDATADIR
63 –PPICS
64 CAS
65 RAS
66 –ERAMW
67 –ERROR
68 –MASTER
69 –MEMCS16
70 –LMEGCS
71 –REFRESH
72 –AEN2
73 –AEN1
74 XA9
75 XA8
76 XA7
77 XA6
78 XA5
79 XA3
80 RAM WRWT
81 FCLK
82 POWER GOOD
83 VSS
84 XTAL 1(1)
–XMEM W
–X IOW
VSS
–MEM R
–IOR
–INTA
PROC CLK
VSS
–SMEM W
–READY

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
XTAL1(2)	2	O	Crystal 1 Output 2 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This is the crystal output. Typical load = 33 pF.
XTAL1(1)	3	I	Crystal 1 Input 1 - A parallel resonant fundamental mode crystal should be attached across XTAL1(1) and XTAL1(2). This input drives the internal oscillator and determines the frequency of OSC. Typical load = 33 pF.
IOCHRDY	4	I	I/O Channel Ready - This input is generated by an I/O device. When low, it indicates a not ready condition. This is used to extend memory or I/O accesses by inserting wait states. When high, this signal allows normal completion of a memory or I/O access.
CPUHLDA	5	I	CPU Bus Hold - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
–S1	6	I	Status 1 - An active low input/pull-up from the CPU in combination with –S0 and M/–IO determine which type of bus cycle to initiate. –S1 going active indicates a read cycle unless –S0 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or halt/shutdown operation.
–S0	7	I	Status 0 - An active low input/pull-up from the CPU in combination with –S1 and M/–IO determine which type of bus cycle to initiate. –S0 going active indicates a write cycle unless –S1 also goes active. Both status inputs active indicate an interrupt acknowledge cycle or a halt/shutdown operation.
M/–IO	8	I	Memory or I/O Select - This input indicates the type of bus cycle to be performed. If high, a memory cycle or halt/shutdown cycle is started. If low, then an I/O cycle or an interrupt acknowledge cycle will be initiated.
SWRST	9	I	This active high input signal will force a CPU reset when a low to high transition is detected.
A1	10	I	CPU Address Bus Bit 1 - This input is used to determine when to initiate a shutdown operation. A shutdown will be started when A1 is low, M/–IO is high, and both –S0 and –S1 go low.
–IOCS16	11	I	I/O Chip Select 16 - This active low input is generated by an I/O device for a 16-bit data bus access. This signal is used to determine the number of wait states and whether data conversion is necessary for I/O accesses.
–WS0	12	I	Wait State 0 - This active low input signal should have an external pull-up. A peripheral device can pull this signal low to force a zero wait state cycle.
–ROMCS	13	I	ROM Chip Select - This active low input is a signal generated from –LCS0ROM and –LCS1ROM and is used to indicate a ROM memory access.
F16	14	I	This input indicates an on-board memory access. It is used along with –ROMCS to determine whether a memory access is to ROM, on-board RAM or off-board RAM. It is also used to inhibit a command delay for memory accesses.
A0	15	I	CPU Address Bus Bit 0 - This input is used to generate enable signals for the data bus transceivers.
ENMODL	16	I	Enable Modulation - Is an input used to control the clock modulator on the VL82C201. When this signal is high, normal clock modulation can occur. When ENMODL is low, clock modulation is disabled and PROCCLK is forced to 1/4 the frequency of FCLK.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
ROMWTST	17	I	ROM Wait State - This input is used to select the desired number of ROM access wait states. ROMWTST low indicates two waits while ROMWTST high indicates three wait states.
RAMRDWT	18	I	RAM Read Wait State - This input indicates the number of wait states to be used for on-board RAM read cycles. A high indicates one wait state reads while a low indicates zero wait state reads. RAMRDWT also controls the timing on RAS and CAS during memory read cycles.
–BUSY287	19	I	Busy - A busy status input that is asserted by the 80287 to indicate that it is currently executing a command.
OSC	20	O	This is the buffered output of the XTAL1 oscillator.
MHZ119	21	O	This output is the OSC output clock divided by 12.
–XBHE	22	I/O	Transfer Byte High Enable - This active low I/O is used to enable –DENHI and determine when a 16-bit to 8-bit data conversion is needed. –XBHE is driven as an output during all DMA cycles. It is forced low if –AEN2 is active and it is driven as the inversion of SA0 if –AEN1 is active.
–NPCS	23	O	Numerical Processor Chip Select - This active low output is the chip select for the 80287 numerical processor.
RESET287	24	O	Reset 287 - This active high output is used to reset the 80287 numerical processor.
–DENHI	25	O	Data Bus Enable High - This active low output is used to enable the data bus transceiver on the high byte of the data bus.
–DENLO	26	O	Data Bus Enable Low - This active low output is used to enable the data bus transceiver on the low byte of the data bus.
DT/–R	28	O	Data Transmit/Receive - An output that determines the data direction to and from the local data bus. A high indicates a write bus cycle and a low indicates a read bus cycle. DT/–R is high when no bus cycle is active. –DENLO and –DENHI are always inactive when DT/–R changes state.
ALE	29	O	Address Latch Enable - A positive edge output that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
RAMALE	30	O	RAMALE is used to latch RAM address buffers. It is forced high at the end of any bus cycle. This allows the address for the next bus cycle to be passed to the system memory sooner than the ALE signal. RAMALE will go back low at the end of the status cycle for any bus cycle to latch the memory address until the end of the bus cycle.
–DMAAEN	31	O	DMA Address Enable - An active low output that is active whenever an I/O device is making a DMA access to the system memory. It will go low anytime –AEN1 or –AEN2 go low.
RESCPU	33	O	Reset CPU - This is the active high output system reset for the CPU. It is generated from POWERGOOD, SWRST or when a shut down status is generated by the CPU.
–XMEMW	34	I/O	Peripheral Bus Memory Write - An active low I/O that is the memory write command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–XMEMR	35	I/O	Peripheral Bus Memory Read - An active low I/O that is the memory read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–XIOW	36	I/O	Peripheral Bus Input/Output Write - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–XIOR	37	I/O	Peripheral Bus Input/Output Read - This active low I/O is the read command to and from the peripheral bus. This pin is configured as an output when –DMAAEN is high and an input when –DMAAEN is low.
–MEMW	39	I/O	Memory Write - This active low I/O is the memory write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–MEMR	40	I/O	Memory Read - This active low I/O is the memory read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive. –MEMR is also active during a refresh cycle.
–IOW	41	I/O	Input/Output Write - This is the active low I/O write command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–IOR	42	I/O	Input/Output Read - This is the active low I/O read command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
–BUSY286	43	O	Processor Extension Busy - This output goes to the –BUSY input of the 80286. If pulled low, this signal stops the 80286 program execution on all WAIT and some ESC instructions until it returns inactive (high).
–INTA	44	O	Interrupt Acknowledge - This active low output that is three-stated is the interrupt acknowledge command from the bus controller portion of the chip. It will be three-stated when CPUHLDA is asserted and CNTLOFF is inactive.
RESET	45	O	Reset - This active high output signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLKIN.
PROCCLK	46	O	Processor Clock - This is the output of the on-board clock modulator. When the clock modulator is enabled the frequency of PROCCLK will be FCLK/2 except for I/O cycles, off-board memory cycles, and DMA cycles. The frequency of PROCCLK will switch to FCLK/4 during those cycles.
SYSCLK	47	O	System Clock - This output is the main system clock. It is equal to half the PROCCLKIN frequency and is synchronized to the processor's T-states.
SA0	49	I/O	System Address Bus Bit 0 - SA0 is driven as an output anytime CPUHLDA is low, and will be an input at all other times. It is used internally to control the data bus enable signals and to determine the state of –XBHE during 8-bit DMA cycles.
–SMEMW	50	O	Memory Write - An active low three-stated output that is the memory write command to the expansion bus. Drives when –LMEGCS is low.
–SMEMR	51	O	Memory Read - An active low three-stated output that is the memory read command to the expansion bus. Drives when –LMEGCS is low.
–READY	52	O	Ready - When active, indicates that the current bus cycle is to be completed. –READY is an open drain output requiring an external pull-up resistor.
MHZ7	53	O	This output is the OSC output divided by 2. It is generated to provide a fixed clock frequency for the keyboard controller and 80287 coprocessor.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ENAS	55	O	Enable Address Strobe - This active low output is used to enable the address strobe on the real time clock device. It will go low the first time –S0 is asserted after a system reset.
–REFEN	56	O	Refresh Enable - An active low output. It will be asserted when a refresh cycle is needed for the DRAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle.
Q1	57		This active high output will go active during the second phase of a CPU bus cycle following the Ts state.
DIR245	58	O	Direction 245 - This output determines the direction of the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals.
GATE245	60	O	Gate 245 - This output enables the data bus transceiver which does conversions from high to low byte or low to high byte for 8-bit peripherals.
CNTLOFF	61	O	Control Off - This output is used to latch the lower byte data bus during high byte to low byte conversions.
XDATADIR	62	O	Transfer Data Direction - This output controls the direction of data flow through the transceiver between the X data bus and the lower byte of the S data bus. A high indicates data flow from the S bus to the X bus. A low indicates data flow from the X bus to the S bus.
–PPICS	63	O	Programmable Peripheral Interface Chip Select - This active low output is a decode of the XA bus. The decode is for address space 060 to 09F. –PPICS can only go active if CPUHLDA is low or –MASTER is low.
CAS	64	O	This is the output used to control the timing of the CAS signal to the DRAMs. CAS will go active (high) one clock cycle after RAS if a zero wait state cycle is selected, or 1 1/2 clock cycles if a one wait state cycle is selected. CAS will go back low at the end of the bus cycle.
RAS	65	O	This is the output used to control the timing of the row address strobe signal to the DRAMs. RAS will go high during the second phase of any memory status cycle. It will go back low two clock cycles later if a zero wait state cycle is selected or three clocks later if a one wait state cycle is selected.
–ERAMW	66	O	Early RAM Write - It is used to get an early write enable signal to the DRAMs to support zero wait state write cycles. It will go low during the second phase of any memory write status cycle. –ERAMW returns high at the end of the bus cycle.
–ERROR	67	I	Error - An error status input from the 80287. This reflects the ES bit of the 80287 status word and indicates that an unmasked error condition exists.
–MASTER	68	I	Master - This active low input is asserted by devices on the expansion bus to get control of the bus.
–MEMCS16	69		Memory Chip Select 16 - A low on this pin indicates that the off-board memory is 16-bits wide.
–LMEGCS	70	I	Lower Megabyte Chip Select - This input indicates that the lower memory address space (0-1 megabyte) is selected. When low, it enables the three-state drivers on –SMEMR and –SMEMW.
–REFRESH	71	I	Refresh - This active low input is used to initiate a refresh cycle for the dynamic RAMs.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–AEN2	72	I	Address Enable 2 - This active low input is from the DMA controllers and is used to generate –DMAAEN, control –XBHE, and disable the clock modulator.
–AEN1	73	I	Address Enable 1 - This active low input is from the DMA controllers and is used to generate –DMAAEN, control –XBHE, and disable the clock modulator.
XA5-XA9	78-74	I	Peripheral Address Bus Bits 5-9 - These inputs are used to decode chip select and reset signals for the coprocessor.
XA3	79	I	Peripheral Address Bus Bit 3 - This input is used in control of the coprocessor reset and chip select signals.
RAMWRWT	80	I	RAM Write Wait State - Indicates the number of wait states to be used for on-board RAM write cycles. A high indicates one wait state writes while a low indicates zero wait state writes. RAMWRWT also controls the timing on RAS and CAS during memory write cycles.
FCLK	81	I	This is the fast clock input to the clock modulator circuit. It should be driven from an external crystal oscillator at twice the frequency of the desired PROCCLK output.
POWERGOOD	83	I	System Power-on Reset - This input signal indicates that power to the board is stable. A Schmitt-trigger input is used so the input can be connected directly to an RC network.
PROCCLKIN	84	I	This is the main clock input to the VL82C201 and should be connected to the signal that drives the 80286 CLK pin. It can be connected to the PROCCLK output (Pin 46) if the internal clock modulator is used or can be connected to an externally generated clock.
VDD	32, 54, 82		System Power: 5 V
VSS	1, 27, 38, 48, 59		System Ground

4

FUNCTIONAL DESCRIPTION

The VL82C201 chip generates all the major clocks for an AT-compatible system design along with the command and control signals for both the system and peripheral buses. It interfaces with the CPU to determine the type of bus cycle to execute and generates the –READY signal to indicate that the current bus cycle can be terminated. It also contains logic to make conversions between 16-bit and 8-bit data accesses. Finally, it generates some of the control signals necessary for the 80287 Numerical Processor.

CLOCK GENERATION

The VL82C201 contains a clock modulator to control the processor clock signal and an oscillator to generate the OSC, MHZ7 and MHZ119 signals.

The oscillator is designed to use an external parallel resonant fundamental mode crystal. A 14.318 MHz crystal should be used to maintain compatibility and connected as shown in Figure 1. The variable capacitor is optional. It is used to make slight adjustments to the output frequency. The OSC output is generated directly from this oscillator for the system bus. The MHZ7 output is the oscillator frequency divided by 2 and can be used to drive the 8042 keyboard controller. The MHZ119 output is the oscillator frequency divided by 12 and is used by the Peripheral Controller chip.

The clock modulator portion of the VL82C201 is designed to gracefully switch the speed of the processor clock based on which type of bus cycle is going to be performed. The FCLK input to the modulator should be driven from an external crystal oscillator at a frequency that is two times the desired PROCCLK frequency. The clock modulator can be disabled by driving the input signal ENMODL low. When the clock modulator is disabled the PROCCLK output will be 1/4 the frequency of the FCLK input.

The clock modulator circuit uses the CPU status signals –S0, –S1, and M/–IO along with the signal F16 from the Memory Controller chip to determine which type of bus cycle is needed. Normally the PROCCLK output will be running at 1/2 the frequency of FCLK. When the processor signals an I/O

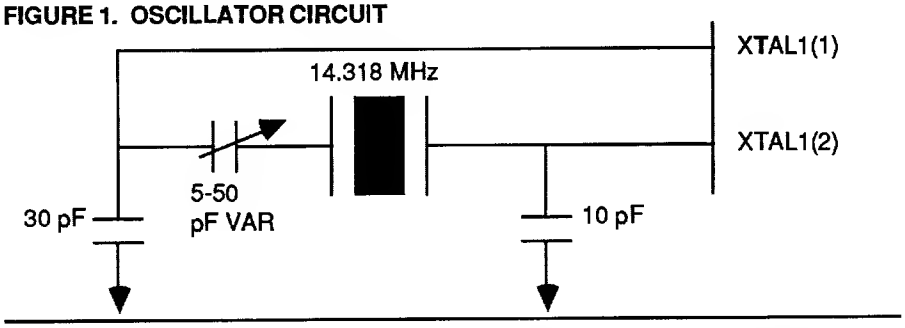
cycle, INTA cycle or off-board memory cycle the modulator will switch the processor clock to 1/4 the frequency of FCLK. The transition is made such that during the second phase of the status cycle PROCCLK will be three FCLK cycles long and all subsequent PROCCLK cycles will be four FCLK cycles long. If the bus cycle is an off-board memory access, the clock modulator will sample –READY to determine when to return PROCCLK to 1/2 the frequency of FCLK. If the bus cycle is an I/O access, the clock modulator will remain at the slow rate until a memory cycle occurs. The clock modulator will then speed up when it samples –READY at the end of the memory cycle.

The inputs –AEN1 and –AEN2 are also sampled by the clock modulator and PROCCLK is slowed to FLCK/4 anytime either of these signals are active.

To reduce clock skew and increase flexibility for the user the PROCCLKIN input is provided. This input should be connected to the same signal that is used to drive the CLK input of the processor. This guarantees that the VL82C201 is referenced to the same clock as the processor with no internal skews. The user can connect this input to the PROCCLK output if the clock modulator is to be used. PROCCLKIN can also be driven from a user supplied source if the clock modulator is not needed.

The SYSCLK output is derived from the PROCCLKIN input and is 1/2 the frequency of PROCCLKIN. SYSCLK is held low during reset and will not begin running until the first bus cycle is initiated by the CPU. It will then make its first low to high transition on the falling edge of PROCCLKIN during the start of the first TC cycle (see timing waveforms). This synchronization is done to ensure that the system clock is synchronized with the 80286 internal system clock.

FIGURE 1. OSCILLATOR CIRCUIT



RESET AND READY CONTROL

The 82284 megacell along with some support logic is used to control the system reset signals and –READY signal for the CPU. Two basic reset signals are generated for the system.

RESET is the system reset out of the 82284 megacell and is synchronized to PROCCLK. It is generated from the POWERGOOD input signal. The POWERGOOD pin has a Schmitt-trigger input so that an RC network can be used to generate the reset signals. RESCPU, the other reset output, is connected to the input on the 80286 processor. RESCPU will be active anytime RESET is active. It can also be generated from two other possible sources. The first is the SWRST input from the Memory Controller chip. A low to high transition is detected on this pin. When this occurs, RESCPU will go active after a minimum delay of 6.72 microseconds. RESCPU will also be generated if a shutdown command is issued from the CPU. In either case, the RESCPU output will pulse high for 16 PROCCLKIN cycles.

The –READY output is synchronized and controlled by the 82284 megacell. –READY is an open drain output connected directly to the CPU and requires an external pull-up resistor. A resistor value of 330 Ω is recommended. Bus cycle length is controlled by the –READY output. Bus cycles are lengthened and shortened internally by the VL82C201 depending on the type of bus cycle being executed. The length of a bus cycle can be shortened externally by pulling the –WS0 input low or lengthened by pulling the IOCHRDY input low. If IOCHRDY is pulled low the bus cycle will not be terminated until IOCHRDY is returned high.

COMMAND AND BUS CONTROL

The VL82C201 contains an 82288 bus controller megacell to generate all the bus command and control signals. The 82288 megacell generates the –MEMR, –MEMW, –IOR, and –IOW command signals and the DT/–R control signal.

The DEN output from the megacell is split into –DENLO and –DENHI for enables on the upper and lower bytes of the data bus. Internal circuitry is used to insert one PROCCLK cycle of command delay for all I/O cycles and off-board 8-bit memory cycles. Refer to the 82288 data sheet for complete operation of the 82288 megacell.

OPERATING MODES

The VL82C201 operates in four basic modes. First, and most common, is the CPU mode. This mode is active any time the input CPUHLDA is low. While in CPU mode the VL82C201 will drive both the CMD (–MEMR, –MEMW, –IOR, –IOW) bus and XCMD (–XMEMR, –XMEMW, –XIOR, –XIOW) bus. While in CPU mode, the outputs –MEMR, –MEMW, –SMEMR, and –SMEMW are disabled from going low for on-board memory accesses. They will go low for off-board memory cycles only. The outputs –XMEMR and –XMEMW will still go active for any memory cycle.

The other modes can only be active when CPUHLDA is high. Then the VL82C201 can be in DMA mode, –MASTER mode, or REFRESH mode. If the inputs –AEN1 or –AEN2 are active, the VL82C201 is in DMA mode and the CMD bus is driven from the inputs on the XCMD bus. If the –MASTER input is active, the VL82C201 is in –MASTER mode and the XCMD bus is driven from the inputs on the CMD bus. When the –REFRESH mode is active the –MEMR output will be driven to generate the refresh for the DRAMs but –MEMW, –IOR, and –IOW will be in a high impedance state. The XCMD pins will be configured as outputs driving whatever value is on the CMD pins.

SYSTEM BOARD MEMORY CONTROL

Timing control for the system board memory is controlled by four signals: RAMALE, RAS, CAS, and –ERAMW.

RAMALE is used by both the Memory Controller and Address Buffer chips to latch in current address values for generating address and chip select signals for the DRAMs. The RAMALE signal is forced high during reset to pass through the first address from the CPU. At the end of the first status cycle RAMALE will go low and will remain low until –READY is sampled low. After the first memory access RAMALE will always go high at the end of any bus cycle, when –READY is sampled low. RAMALE will go low latching in the current address at the end of any status cycle. This configuration will leave the RAMALE signal high during CPUHLDA cycles to allow addresses and chip select decodes to pass directly to the DRAMs for DMA or –MASTER accesses.

The RAS signal is used to generate the timing control for the DRAMs. It is an active high signal and should be gated with the RAS0 and RAS1 chip select signals out of the Memory Controller chip to generate the RAS signals to the DRAMs. The timing of RAS is controlled by the RAMWRWT, RAMRDWT, and CPUHLDA inputs.

The VL82C201 samples RAMRDWT during memory read cycles and RAMWRWT during memory write cycles to determine whether the cycle should be a zero or one wait state access. A low on these inputs selects zero wait states, while a high will select one wait state. Whenever CPUHLDA is low (inactive) RAS will always go active during the second phase of any memory access status cycle. If the current memory access should be a zero wait state cycle, RAS will return low two PROCCLKIN cycles later. For a one wait state access, RAS will return low three PROCCLKIN cycles later. This is done to generate timing that will meet specifications for the slower DRAMs typically used in one wait state designs. When CPUHLDA is high, the memory control logic samples the inputs on –XMEMR and –XMEMW for DMA cycles, or –MEMR and –MEMW for –MASTER cycles. RAS will go high on the first falling edge of PROCCLKIN when any memory read or write command is sampled active. RAS will return low two or three PROCCLKIN cycles later depending on the states of RAMRDWT and RAMWRWT as described above for the CPU accesses.

The CAS signal is also used to generate timing control for the DRAMs. It is an active high signal and should be gated with CAS0 and CAS1 chip select signals out of the Memory Controller chip to generate the CAS signals to the DRAMs. The timing of CAS is controlled by the RAMWRWT and RAMRDWT inputs.

RAMRDWT and RAMWRWT function the same as described above for the RAS signal to determine whether the current memory access should be zero or one wait states. For a zero wait state access CAS will go active one PROCCLKIN clock cycle after RAS goes active. During a one wait state access CAS will go active 1 1/2 PROCCLKIN clock cycles after RAS goes active. This is done to allow more row address hold time for the slower DRAMs that can be used in a one wait state system. CAS goes inactive (low) at the same time for both zero and one wait state accesses. When CPUHLDA is low, CAS will return inactive at the end of the bus cycle when –READY is sampled low. When CPUHLDA is high, CAS will return inactive on the falling edge of the first PROCCLKIN cycle when all the memory read and write commands are sampled inactive.

–ERAMW is an early write signal for the DRAMs to make sure the write signal is present before CAS. It will go low during the second phase of any memory write status cycle. –ERAMW returns high at the end of the bus cycle.

Note: Although RAMRDWT and RAMWRWT can be changed dynamically for each memory cycle, care must be taken to never allow RAMRDWT to be high and RAMWRWT to be low at the same time for more than 60 ns. This results in zero wait state write cycles and one wait state read cycles. This was determined to be an unrealistic operating mode and is used to put the VL82C201 into a test mode that will disrupt normal system operation.

WAIT STATE LOGIC

Wait states can be controlled from a number of different sources within the VL82C201. It is internally programmed to generate the wait states shown in Table 1 based on the appropriate input signals.

Any of these programmed values can be overridden by the inputs IOCHRDY and –WS0. IOCHRDY can be used to extend any bus cycle. When IOCHRDY is pulled low the current bus cycle will be maintained until it is returned high. A low on –WS0 will terminate the current bus cycle as soon as it is recognized by the VL82C201. These inputs need only be pulled low to modify the values shown in Table 1. IOCHRDY and –WS0 are mutually exclusive and only one of them should be pulled low within a given bus cycle. Refer to the timing diagrams for setup and hold requirements.

REFRESH CONTROL

The VL82C201 contains circuitry to control a refresh cycle in an AT-compatible design. When the input –REFRESH is pulled low, the VL82C201 will issue –REFEN to clock the refresh counter and enable the refresh addresses onto the memory address bus. It will also issue a –MEMR command. For correct operation –REFRESH should not be pulled low unless CPUHLDA is active.

DATA CONVERSION

A state machine for controlling the conversion between 16-bit data accesses from the CPU and 8-bit peripherals is contained in the VL82C201. This state machine will generate the control signals DIR245, GATE245, and CNTLOFF to the Data Buffer chip to route the data correctly for both read and write conversions. The conversion logic will signal the wait state logic to hold the CPU and start the read/write of the low data byte. It will then latch the low byte for a read operation, negate the bus control signals, switch SA0 to a high, and then perform the read/write operation for the high data byte. The VL82C201 also uses the DIR245 and GATE245 during 8-bit DMA cycles to route the lower byte on the system data

bus to or from the high or low byte of on-board memory.

NUMERICAL PROCESSOR AND PERIPHERAL CONTROL

The VL82C201 generates a reset signal and chip select signal for the 80287 Numerical Processor. The signal RESET287 is used to reset the 80287 and can be activated by a system reset or an I/O write to address 0F1 hex. –NPCS is used as a chip select for the 80287 and is decoded at addresses 0F8-0FF hex.

The VL82C201 also controls the –BUSY286 signal sent to the 80286 from the Numerical Processor. The 80287 will assert –BUSY287 whenever it is performing a task. This signal is passed to the 80286 by asserting the –BUSY286 output. Normally –BUSY286 will follow –BUSY287. However, if the –ERROR signal is asserted while the –BUSY287 signal is active, the –BUSY286 output will be latched low and will remain active until cleared by an I/O write cycle to address 0F0 hex or 0F1 hex.

TABLE 1. WAIT STATES

Access Type	RAM RDWT	RAM WRWT	ROM WTST	F16	–MEM CS16	–IO CS16	Number of Waits	Command Delay
INTA Cycles	X	X	X	X	X	X	4	Yes
8-Bit I/O	X	X	X	X	X	1	4	Yes
16-Bit I/O	X	X	X	X	X	0	1	Yes
Off-board 8-Bit Memory	X	X	X	0	1	X	4	Yes
Off-board 16-Bit Memory	X	X	X	0	0	X	1	No
On-board ROM Read	X	X	1	1	X	X	3	No
On-board ROM Read	X	X	0	1	X	X	2	No
On-board RAM Write	0	0	X	1	X	X	0	No
On-board RAM Write	X	1	X	1	X	X	1	No
On-board RAM Read	0	X	X	1	X	X	0	No
On-board RAM Read	1	1	X	1	X	X	1	No

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

CPU MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t1	PROCCLKIN Period	31		25		ns	
t2	PROCCLKIN High Pulse Width	11		9		ns	
t3	PROCCLKIN Low Pulse Width	7		6		ns	
t4	PROCCLK Rise Time		5		4	ns	1.0 V to 3.6 V, CL = 75 pF
t5	PROCCLK Fall Time		4		4	ns	3.6 V to 1.0 V, CL = 75 pF
t6	FCLK Period	15		12		ns	
t7	FCLK High Pulse Width	6		5		ns	
t8	FCLK Low Pulse Width	6		5		ns	
t9	OSC Rise/Fall Time		15		15	ns	
tD10	MHZ7 from OSC Delay		15		15	ns	
tD11	MHZ119 from OSC Delay		20		20	ns	
tD12	PROCCLK from FCLK Delay		20		17	ns	
tSU13	–S0, –S1 to PROCCLKIN Setup Time	11		9		ns	
tH14	–S0, –S1 from PROCCLKIN Hold Time	1		1		ns	
tSU15	M/–IO to PROCCLKIN Setup Time	20		20		ns	
tH16	M/–IO from PROCCLKIN Hold Time	3		3		ns	
tSU17	F16 to PROCCLKIN Setup Time	7		6		ns	
tH18	F16 from PROCCLKIN Hold Time	5		5		ns	
tSU19	POWERGOOD to PROCCLKIN Setup Time	20		20		ns	Note 1
tH20	POWERGOOD to PROCCLKIN Hold Time	5		5		ns	Note 1
tD21	RESET from PROCCLKIN Delay		24		24	ns	
tD22	RESCPU from PROCCLKIN Delay		17		15	ns	
tD23	SYSCLK from PROCCLKIN Delay		26		23	ns	
tD24	–ENAS from PROCCLKIN Delay		26		26	ns	
tSU25	M/–IO, A1 to –S0, –S1 Setup Time	15		15		ns	
tSU26	SWRST to PROCCLKIN Setup Time	20		20		ns	Note 1
t27	SWRST Pulse Width	60		60		ns	
tD28	ALE from PROCCLKIN Delay		18		16	ns	

Notes: 1. POWERGOOD and SWRST are asynchronous inputs. This specification is given for testing purposes only, to assure recognition at a specific PROCCLKIN edge.

CPU MODE TIMING (Cont.)

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD29	DT/–R Low from PROCCLKIN Delay		30		30		
tD30	DT/–R High from PROCCLKIN Delay		40		35		
tD31	–DENLO, –DENHI Low from PROCCLKIN Delay		33		30	ns	Write Cycles
tD32	–DENLO, –DENHI Low from PROCCLKIN Delay		40		35	ns	Read Cycles
tD33	–DENLO, –DENHI High from PROCCLKIN Delay		33		30	ns	Read and Write Cycles
tD34	–READY Active from PROCCLKIN Delay		16		15	ns	
tD35	–READY Inactive from PROCCLKIN Delay	5		3		ns	Note 2
tD36	XDATADIR from PROCCLKIN Delay		35		35		
tSU37	–IOCS16 to PROCCLKIN Setup Time	17		15		ns	
tH38	–IOCS16 from PROCCLKIN Hold Time	2		2		ns	
tSU39	IOCHRDY to PROCCLKIN Setup Time	15		12		ns	
tH40	IOCHRDY from PROCCLKIN Hold Time	2		2		ns	
tD41	–CMD, –XCMD, –SCMD from PROCCLKIN Delay		30		30	ns	Note 3
tSU42	–WS0 to PROCCLKIN Setup Time	15		12		ns	
tH43	–WS0 from PROCCLKIN Hold Time	3		3		ns	
tSU44	–MEMCS16 to PROCCLKIN Setup Time	15		12		ns	
tH45	–MEMCS16 from PROCCLKIN Hold Time	4		4		ns	
tSU46	A0 to PROCCLKIN Setup Time	20		20		ns	
tD47	SA0 from PROCCLKIN Delay		30		25		
tSU48	–XBHE to PROCCLKIN Setup Time	20		15			
tD49	–DENLO, –DENHI from PROCCLKIN Delay		45		40		Note 4
tD50	–CMD, –XCMD, –SCMD from PROCCLKIN Delay		40		35	ns	Note 4
tD51	Q1 from PROCCLKIN Delay		30		30	ns	

Notes: 2. –READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLKIN cycles. A 330 Ω resistor is recommended. This specification for –READY inactive indicates when the VL82C201 stops driving the output. It does not indicate that –READY has reached a certain voltage level.

3. –CMD refers to the signal pins –MEMR, –MEMW, –IOR, and –IOW. –SCMD refers to the signal pins –SMEMR and –SMEMW. –XCMD refers to the signal pins –XMEMR, –XMEMW, –XIOR, and –XIOW.

4. Caused by CNTLOFF during 16 to 8 bit conversions.

CPU MODE TIMING (Cont.)

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD52	CNTLOFF from PROCCLKIN Delay		30		30	ns	
tD53	DIR245 from PROCCLKIN Delay		45		45	ns	
tD54	GATE245 from PROCCLKIN Delay		45		45	ns	
tSU55	–ROMCS to PROCCLKIN Setup Time	15		12		ns	
tH56	–ROMCS from PROCCLKIN Hold Time	4		4		ns	
tSU57	ROMWTST to PROCCLKIN Setup Time	15		12		ns	
tH58	ROMWTST from PROCCLKIN Hold Time	8		8		ns	
tSU59	RAMRDWT, RAMWRWT to PROCCLKIN Setup Time	15		12		ns	
tH60	RAMRDWT, RAMWRWT from PROCCLKIN Hold Time	2		2		ns	
tD61	RAMALE from PROCCLKIN Delay		18		16	ns	
tD62	–ERAMW from PROCCLKIN Delay		18		16	ns	
tD63	RAS from PROCCLKIN Delay		18		16	ns	
tD64	CAS High from PROCCLKIN Low Delay		18		16	ns	0 Wait State Only
tD65	CAS High from PROCCLKIN High Delay		18		16	ns	1 Wait State Only
tD66	CAS Low from PROCCLKIN Low Delay		18		16	ns	0 and 1 Wait State
tD67	–INTA from PROCCLKIN Delay		30		30	ns	
tD68	–BUSY286 from –BUSY287 Delay		20		20	ns	
tH69	–ERROR form –BUSY287 Hold Time	5		5		ns	
tSU70	–ERROR to –BUSY287 Setup Time	10		10		ns	
tD71	–BUSY286 from –IOW Delay		25		25	ns	
tD72	RESET287 from –IOW Delay		25		25	ns	
tSU73	XA Input to –IOW Setup Time	10		10		ns	
tH74	XA Inputs from –IOW Hold Time	5		5		ns	
tD75	XA Inputs to –NPCS Delay		30		30	ns	
tD76	XA Inputs to –PPICS Delay		25		25	ns	

DMA MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD79	–DMAAEN from –AEN1, –AEN2 Delay		20		20	ns	
tD80	XDATADIR from –XIOR Delay		30		30	ns	
tD81	–CMD, –SCMD from –XCMD Delay		30		30	ns	
tD82	–XBHE from SA0 Delay		30		30	ns	Note
tD83	DIR245 from –XMEMR Delay		30		30	ns	
tD84	GATE245 from –XMEMR, –XMEMW, or –XIOR Delay		35		35	ns	

Note: During –AEN2, –XBHE is low. During –AEN1, –XBHE follows SA0 inverted.

BUS MASTER MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD85	–XCMD from –CMD Delay		25		25	ns	
tD86	–SCMD from –CMD Delay		30		30	ns	
tD87	XDATADIR from –IOR Delay		30		30	ns	

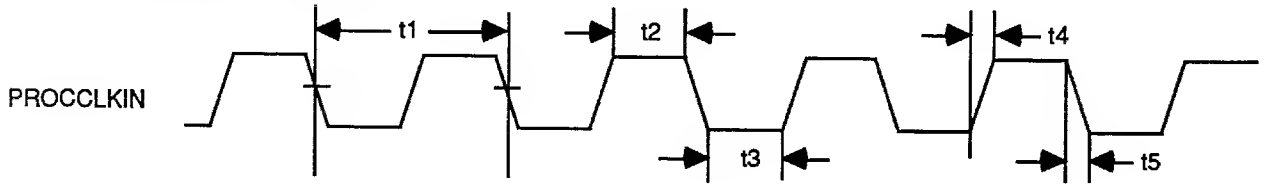
REFRESH MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU88	–REFRESH to PROCCLKIN Setup Time	20		20		ns	
tD89	–REFEN from PROCCLKIN Delay		30		30	ns	
tD90	–MEMR, –XMEMR, –SMEMR from PROCCLKIN Delay		40		40	ns	During –REFRESH

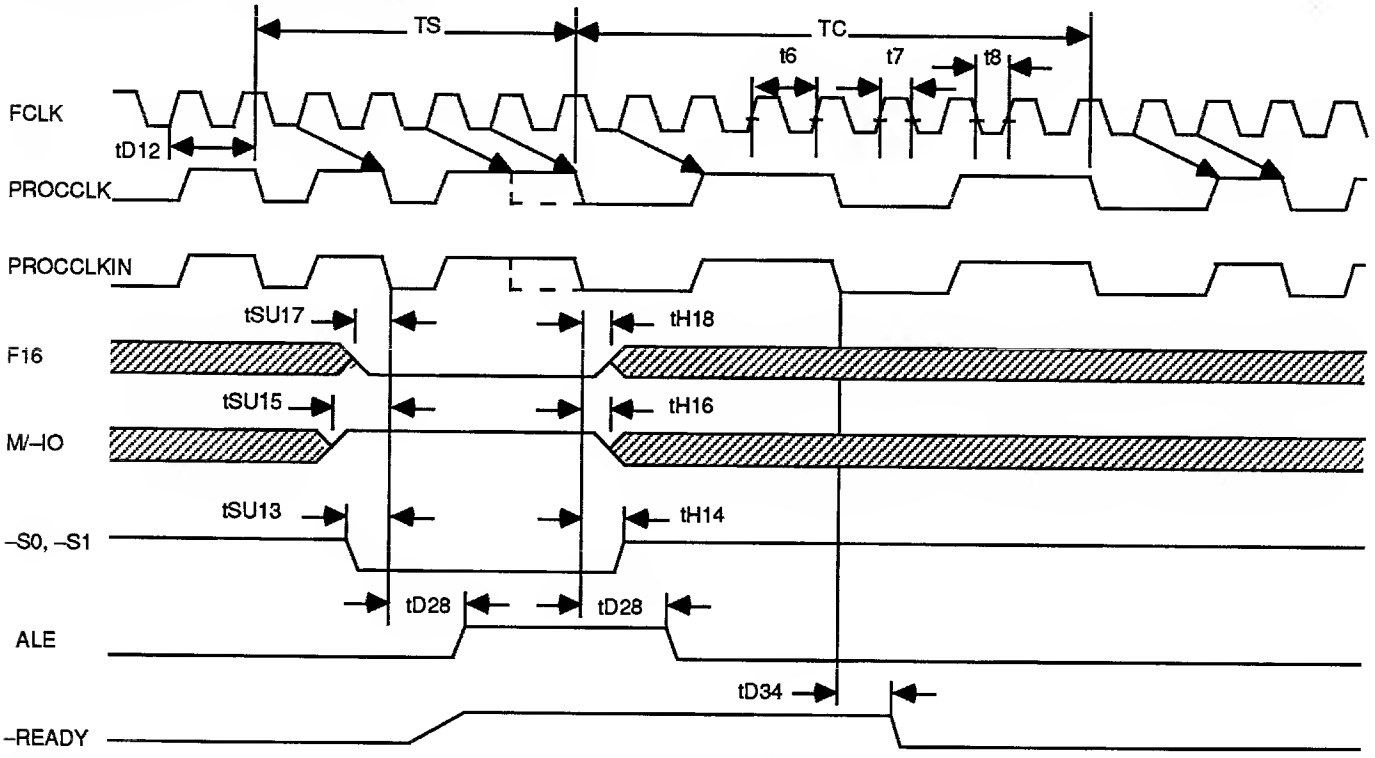
MEMORY CONTROL TIMING DURING DMA OR MASTER MODES

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU91	–MEMR, –XMEMR, –MEMW, –XMEMW to PROCCLKIN Setup Time	17		17		ns	
tH92	–MEMR, –XMEMR, –MEMW, –XMEMW to PROCCLKIN Hold Time	2		2		ns	
tSU93	F16 to –MEMR, –XMEMR Setup Time	5		5		ns	
tH94	F16 from –MEMR, –XMEMR Hold Time	10		10		ns	
tD95	DT/–R from –MEMR, –XMEMR Delay		30		30	ns	
tD96	–DENLO from SA0 Delay		30		30	ns	
tD97	–DENHI from –XBHE Delay		35		35	ns	

PROCCLK TIMING WAVEFORMS

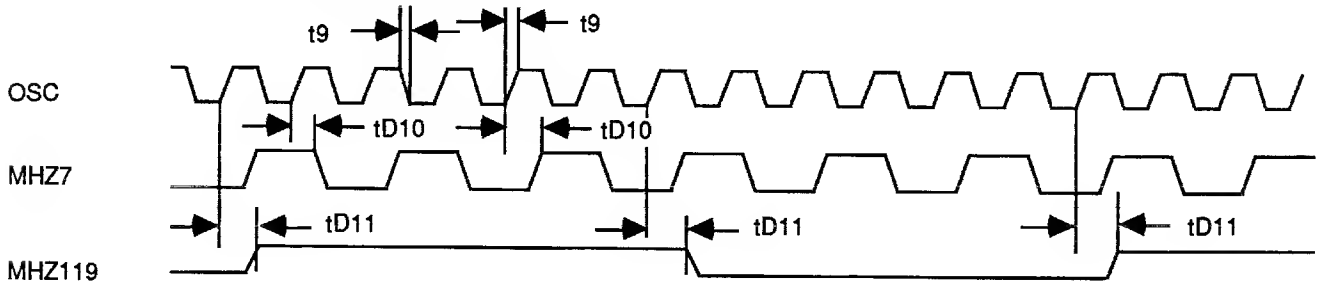


CLOCK MODULATION WAVEFORM

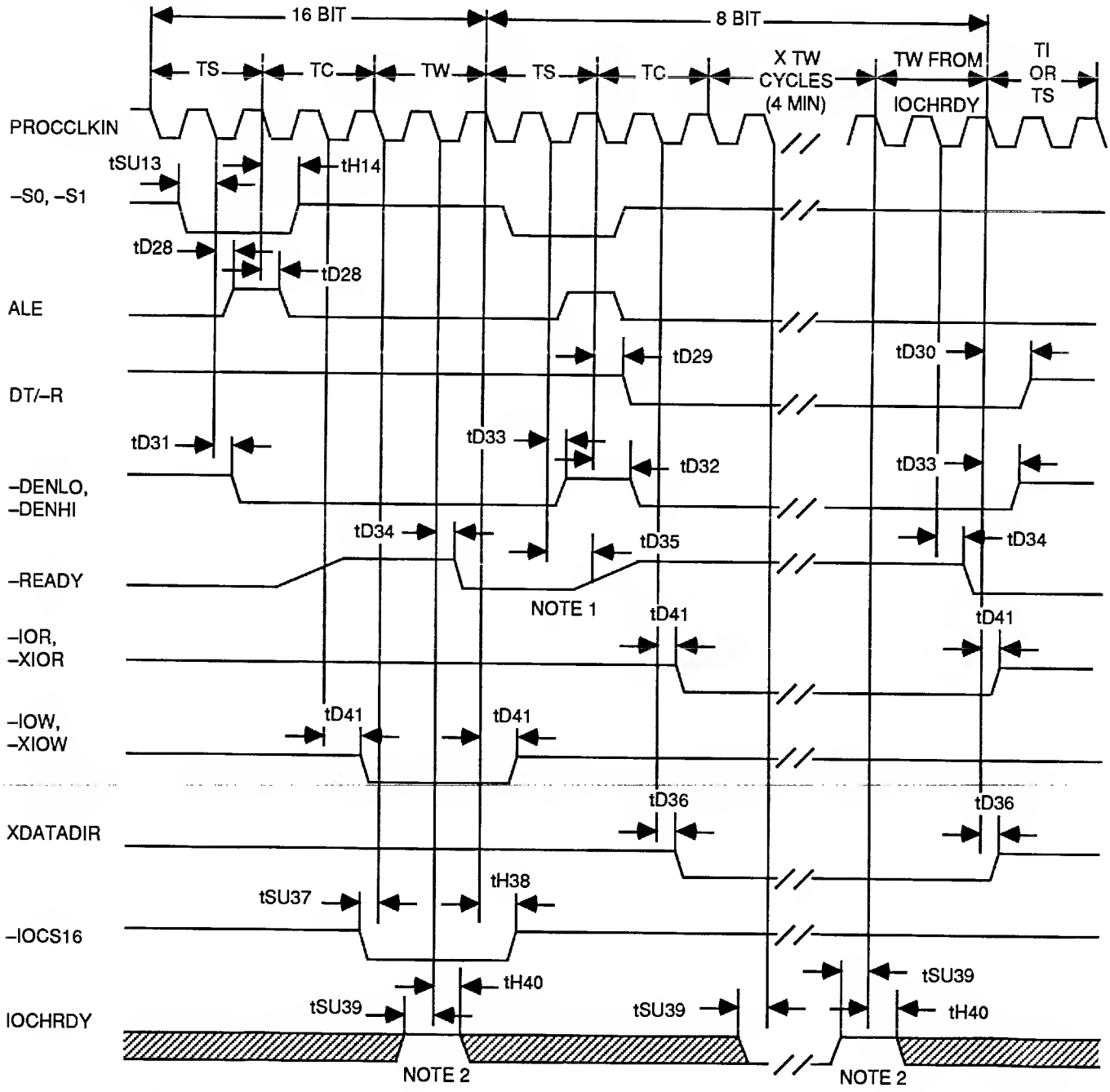


Note: Timing is shown for an off-board memory cycle. The same clock transitions will occur if M/–IO is sampled low, regardless the state of F16.

CRYSTAL DERIVED CLOCK WAVEFORMS



I/O TIMING WAVEFORM

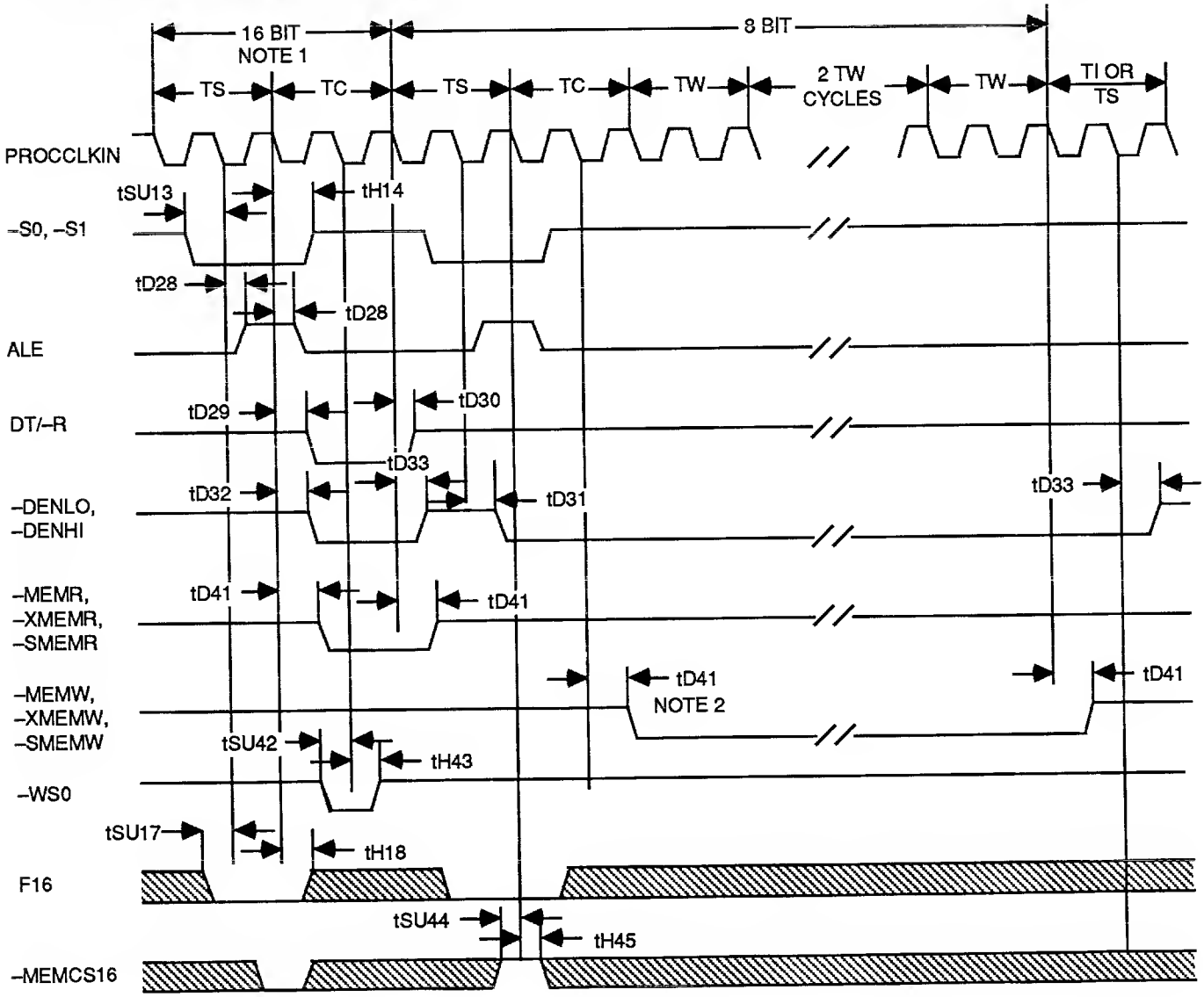


Notes: 1. -READY is an open drain output and requires a pull-up resistor that pulls the signal high within two PROCCLK cycles. A 300 Ω resistor is recommended.

2. IOCHRDY is sampled for the first time in the middle of the first wait state. If it is sampled high, 16-bit bus cycles will terminate with only one wait state. From then on IOCHRDY is sampled at the end of each wait state cycle. When IOCHRDY is sampled high, the bus cycle will terminate one wait state cycle later.

   For 8-bit bus cycles IOCHRDY is sampled for the first time at the end of the third wait state cycle. If it is sampled high, the bus cycle will terminate in four wait states. Otherwise, the bus cycle will be extended until IOCHRDY is sampled high.

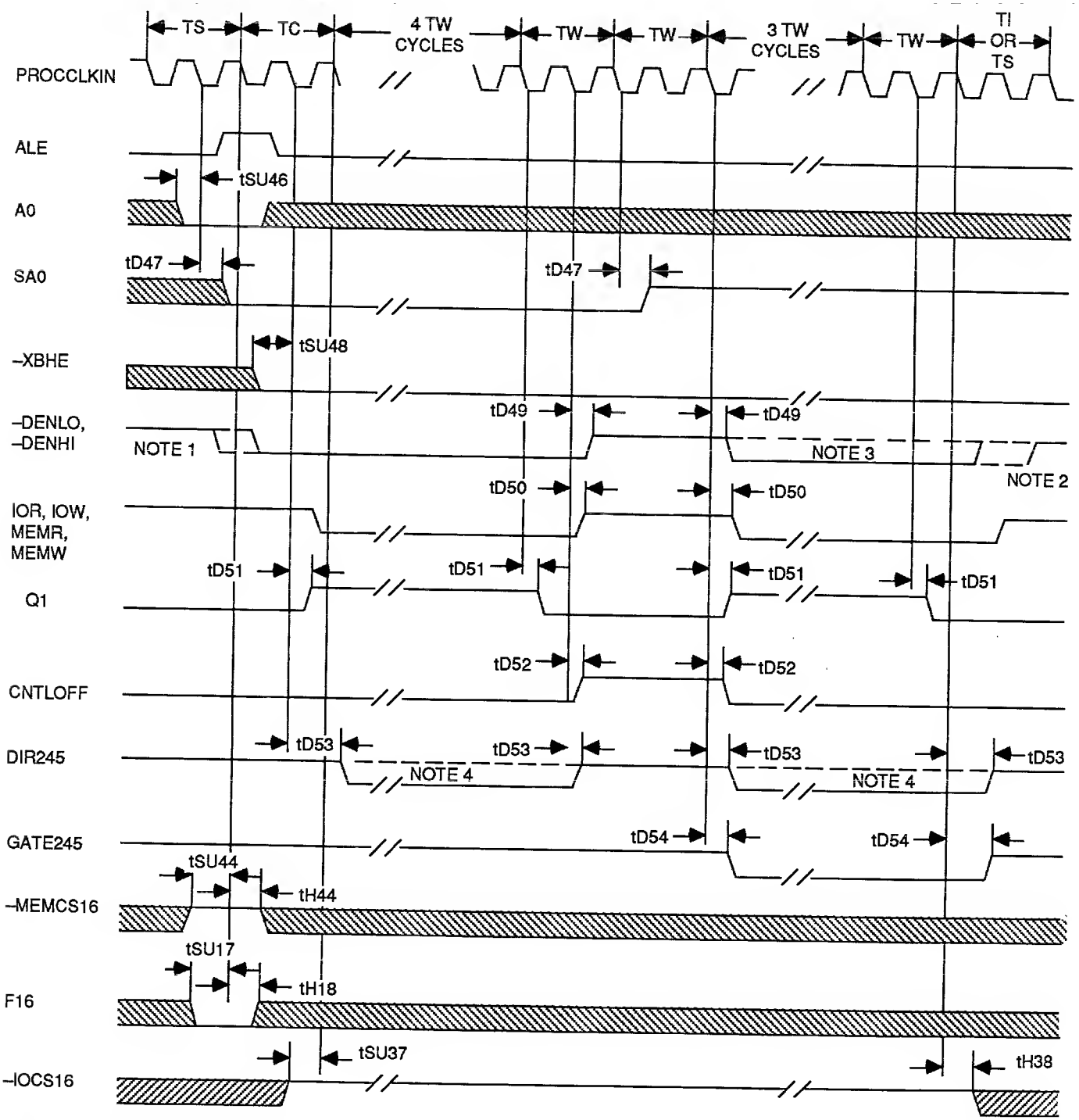
OFF-BOARD MEMORY TIMING WAVEFORM



Notes: 1. This 16-bit cycle is shown as zero wait states terminated by the –WS0 input. Normal off-board memory cycles are one wait state.

2. A command delay is shown on the 8-bit write cycle. Command delays will exist for both reads and writes on the 8 bit cycles. A command delay is not generated for 16-bit reads or writes.

CONVERSION TIMING WAVEFORM



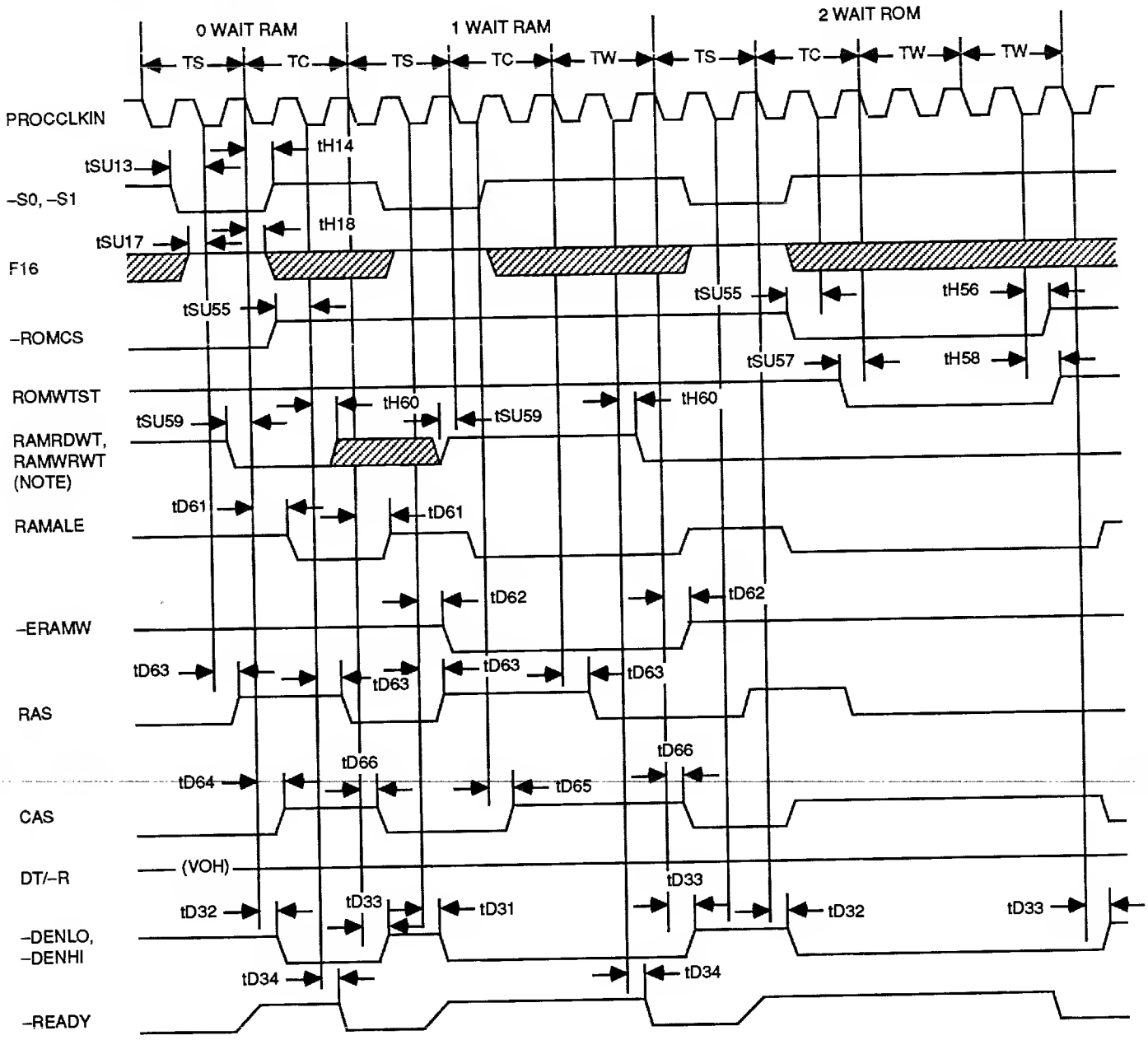
Notes: 1. The first transition shown here is for write cycles. The –DEN signals will go active one PROCCLKIN cycle later for read cycles.

2. The first transition shown here is for read cycles. The –DEN signals will go inactive one PROCCLKIN cycle later for write cycles.

3. –DENLO will not go active during the second half of a conversion cycle for I/O write or memory write commands.

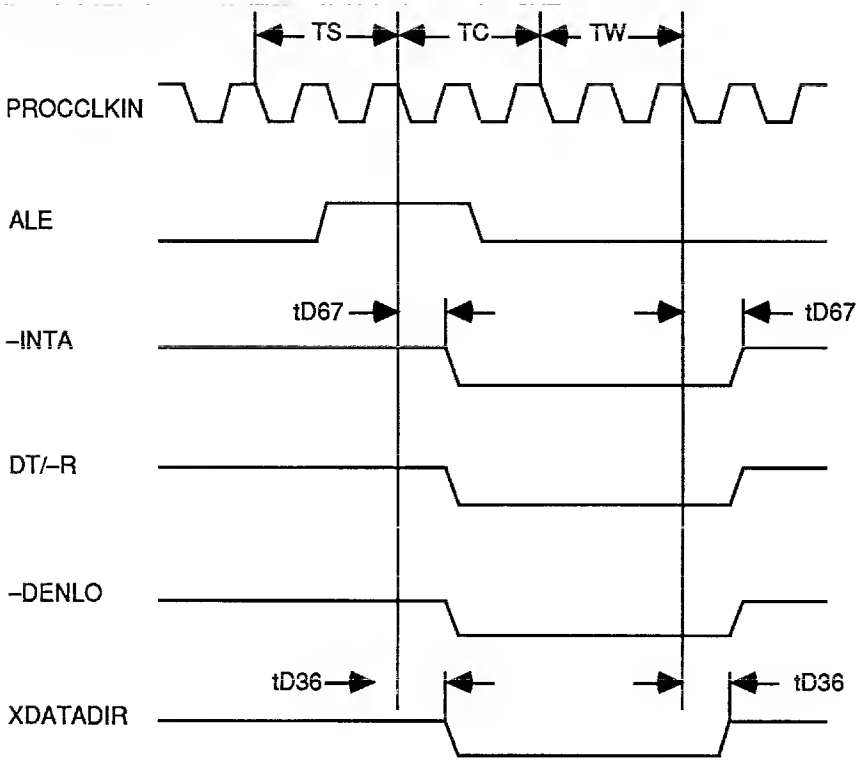
4. DIR245 goes low for a write cycle. It will remain high for read cycles.

ON-BOARD MEMORY TIMING

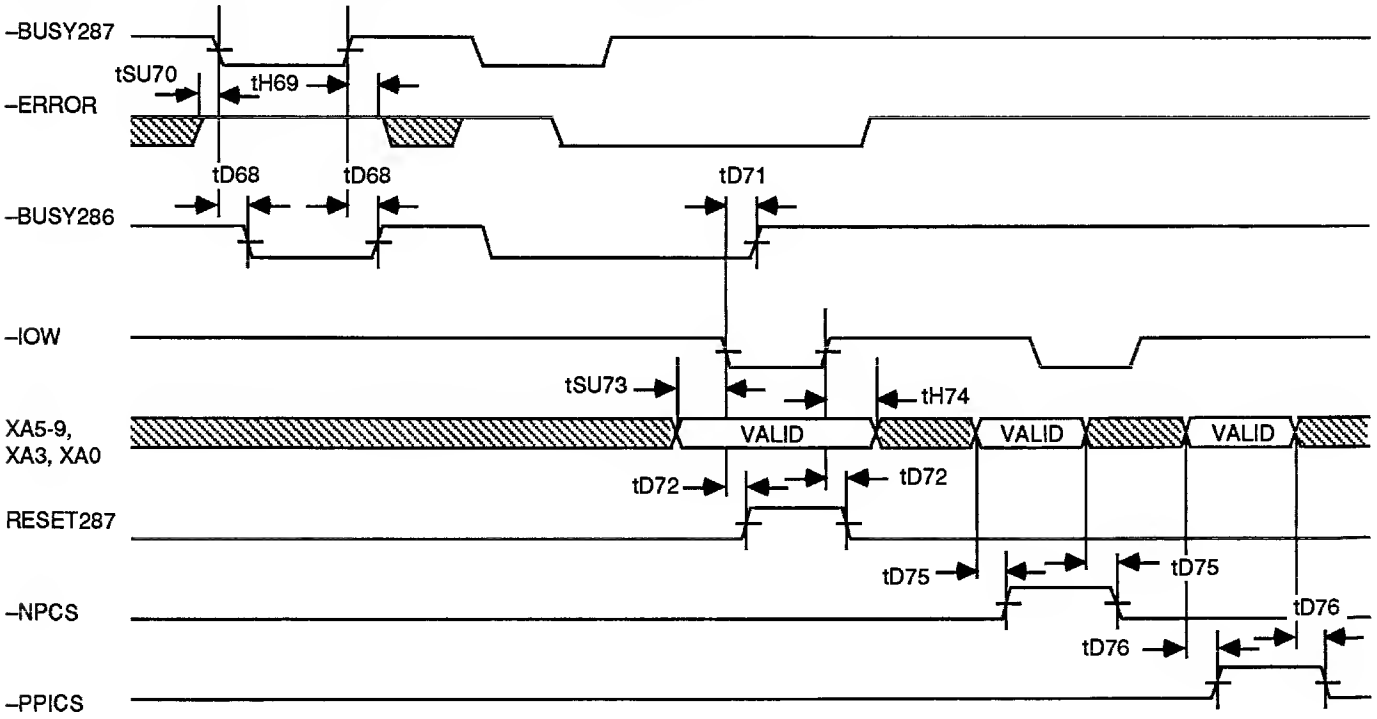


Note: Although RAMRDWT and RAMWRWT can be changed dynamically for each memory cycle, care must be taken to never allow RAMRDWT to be high and RAMWRWT to be low at the same time for more than 60 ns. This results in zero wait state write cycles and one wait state read cycles. This was determined to be an unrealistic operating mode and is used to put the VL82C201 into a test mode that will disrupt normal system operation.

INTA TIMING WAVEFORM

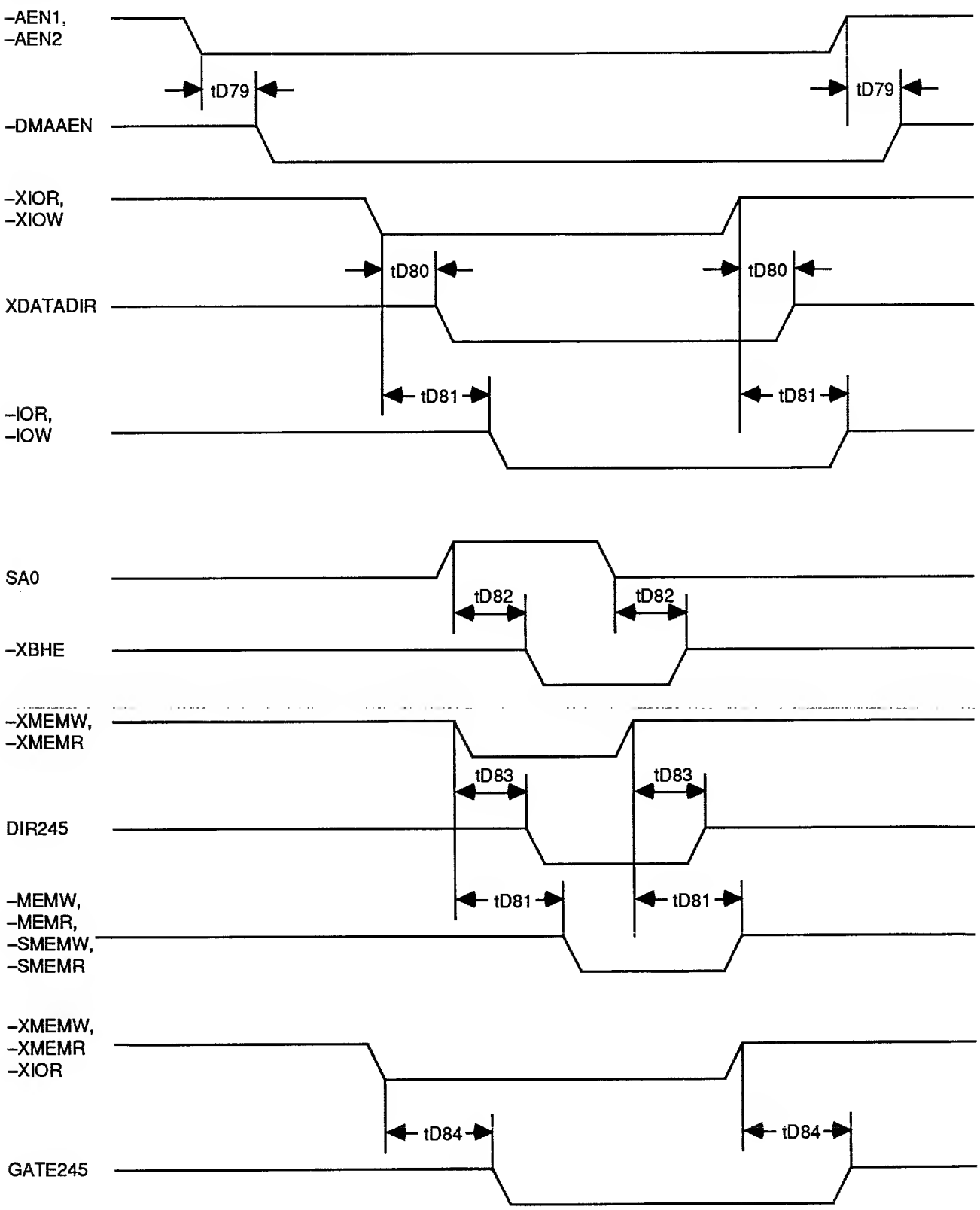


NUMERICAL PROCESSOR INTERFACE TIMING WAVEFORM

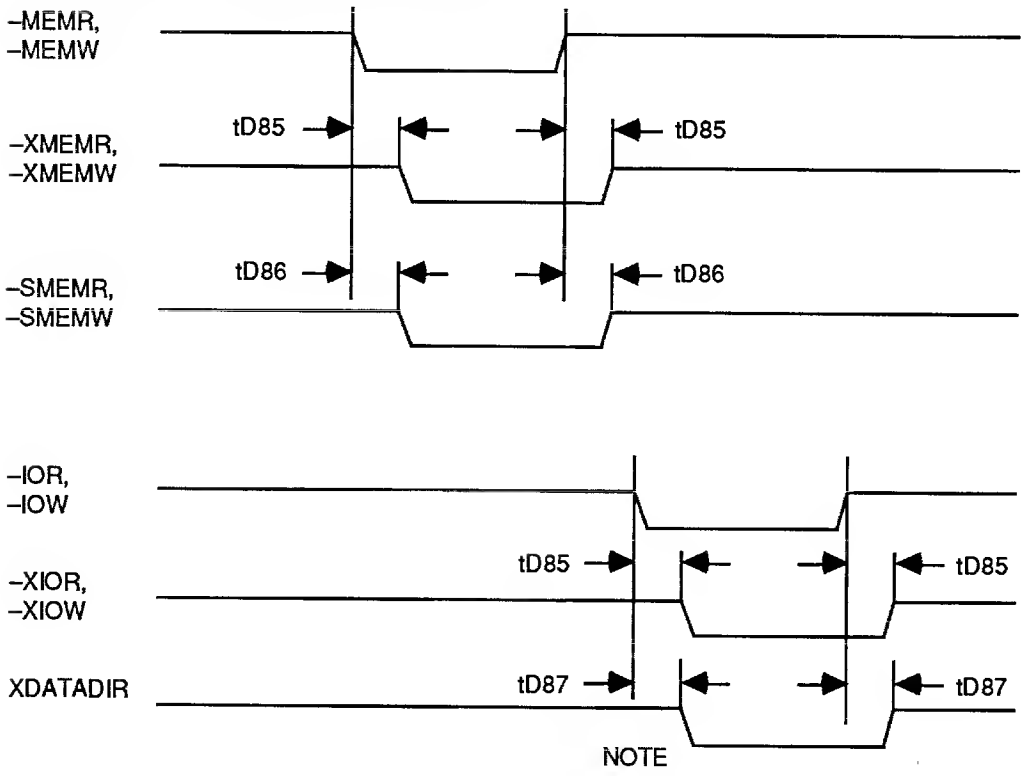


4

DMA MODE TIMING WAVEFORMS

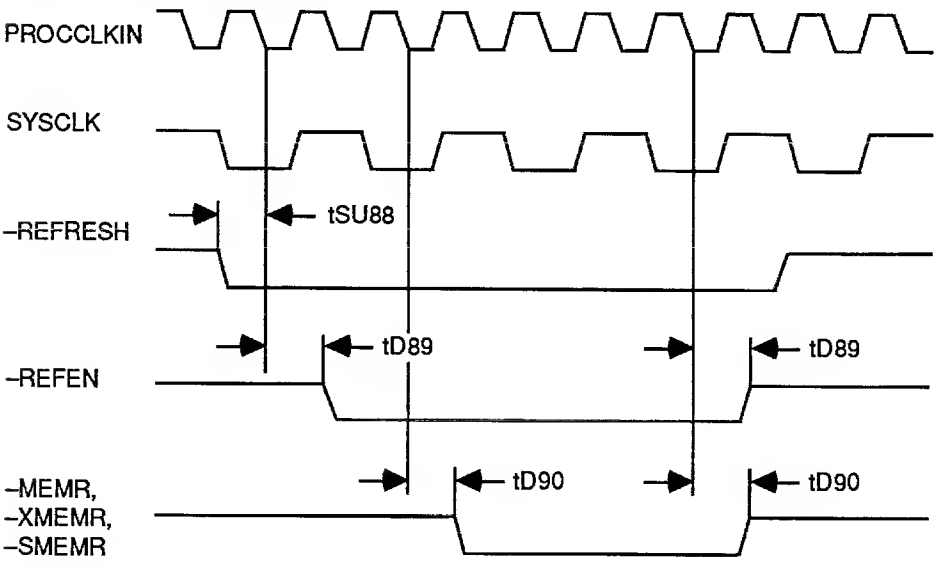


BUS MASTER MODE TIMING WAVEFORM

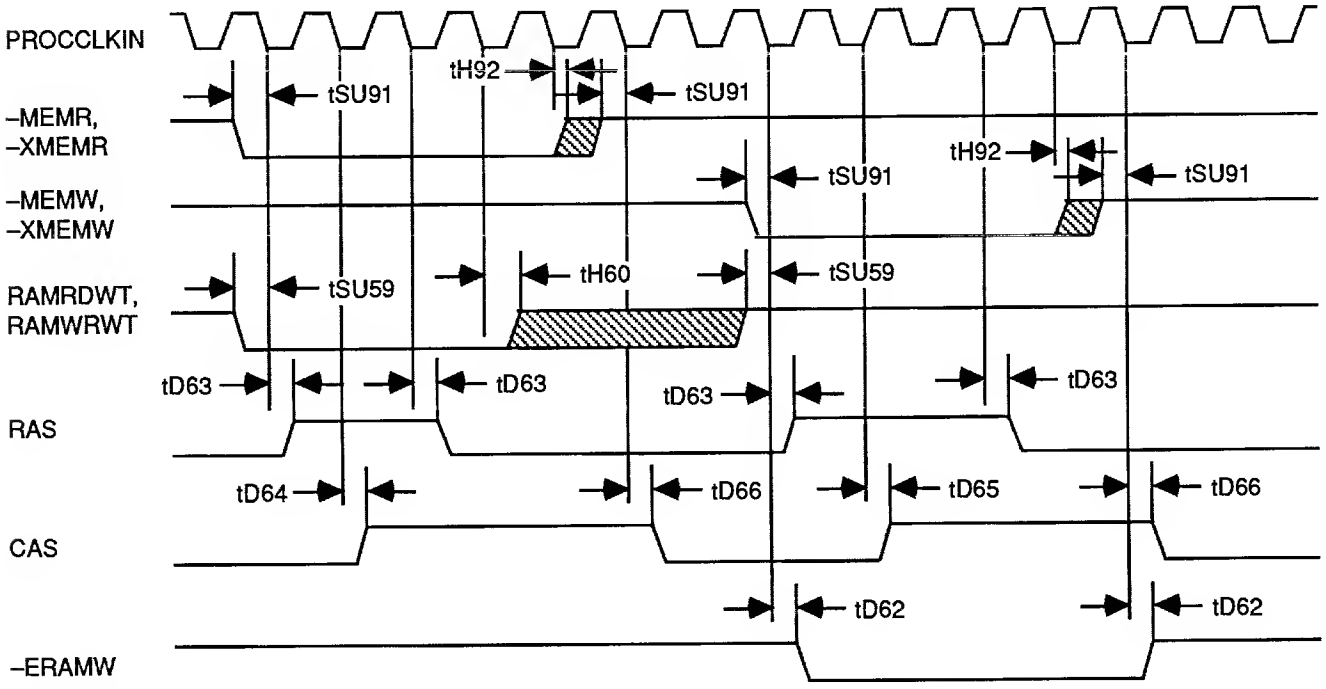


Note: XDATADIR goes low only for -IOR when XA9, XA8 are low and -NPCS is not active.

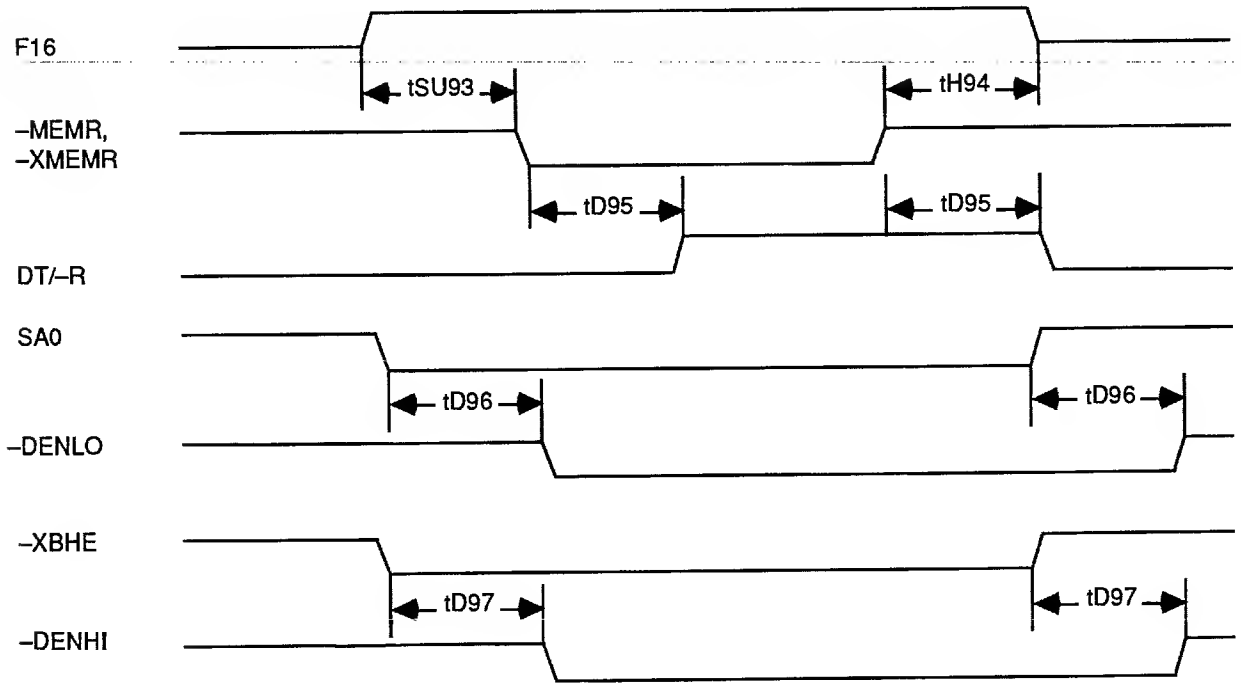
REFRESH TIMING WAVEFORM



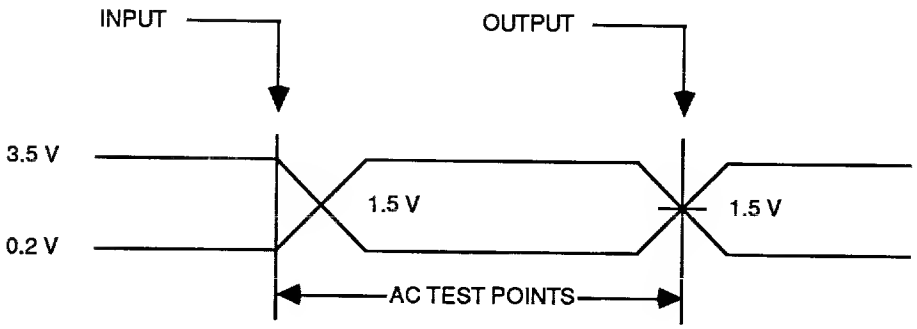
MEMORY CONTROL TIMING WAVEFORMS DURING DMA OR MASTER MODES



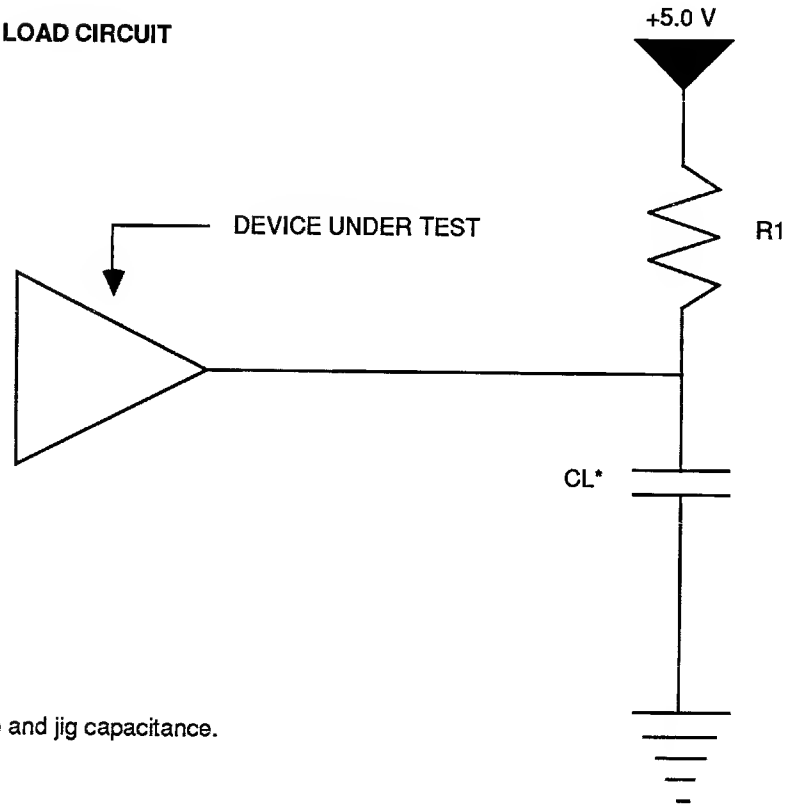
BUS CONTROL TIMING WAVEFORMS DURING DMA OR MASTER MODES



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
20, 39-42, 45, 47, 49-51	200
46, 52	75
21-26, 28-31, 33-37, 43, 44, 53, 55-58, 60-66	50

Test Pin	R1 (Ω)
71	600
34-37, 39-42, 44, 50, 51	10K

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C,QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 24 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 8 mA, Note 2
VIH	Input High Voltage	2.0	VDD + 0.5	V	Except POWERGOOD, PROCCLKIN
VIL	Input Low Voltage	–0.5	0.8	V	
VIHS	Input High Voltage	4.0	VDD + 0.5	V	POWERGOOD, Schmitt-trigger
VIHC	Input High Voltage	3.8	VDD + 0.5	V	PROCCLKIN
VILC	Input Low Voltage	–0.5	0.6	V	PROCCLKIN
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	Except –S1, –S0, XTAL1(1)
ILIS	Input Leakage Current	–0.5	0.01	µA	–S1, –S0, Note 3
ILIX	Input Leakage Current	–40	40	µA	XTAL1(1)
ICC	Power Supply Current		40	mA	Note 4

Notes: 1. Pins 20, 39-42, 45, 47, 49-52.
2. All other pins.
3. –S1 and –S0 have small pull-up resistors to VDD and source up to 0.5 mA when pulled low.
4. Inputs = VSS or VDD, outputs are not loaded.

VL82C202

PC/AT-COMPATIBLE MEMORY CONTROLLER

FEATURES

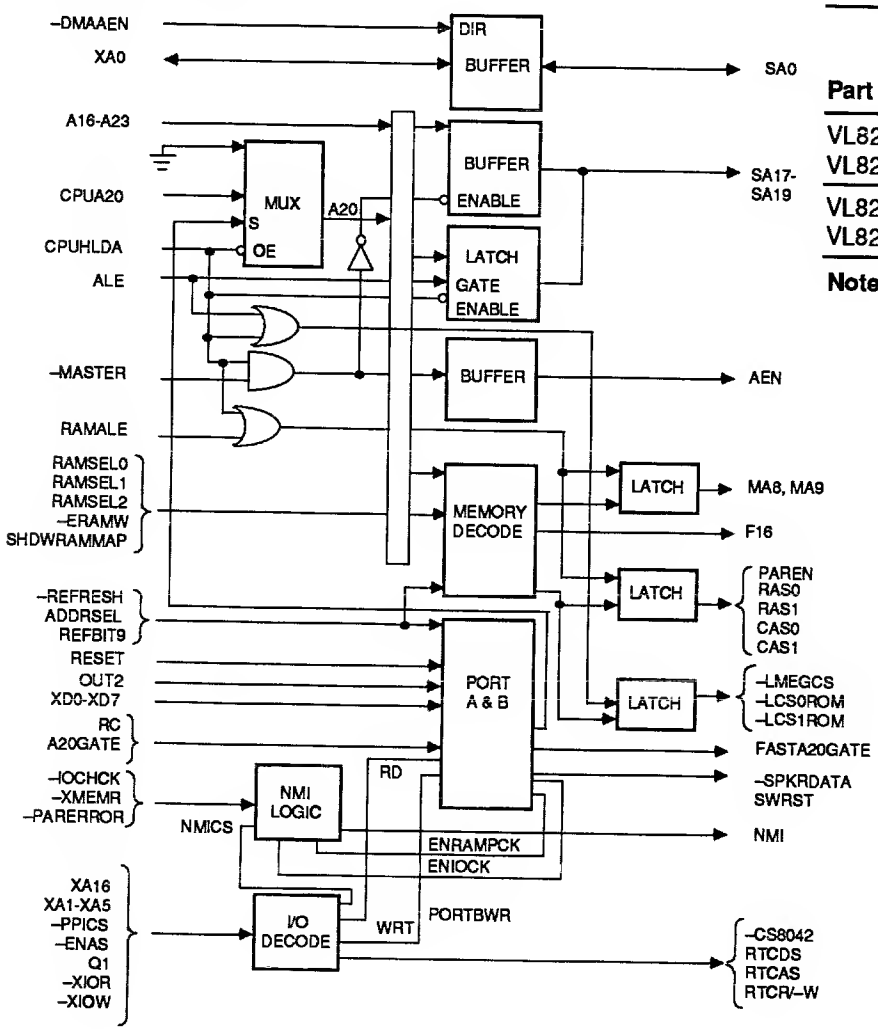
- Fully compatible with IBM PC/AT-type designs
- Completely performs memory control function in IBM PC/AT-compatible systems
- Replaces 20 integrated circuits on PC/AT-type motherboard
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C202 PC/AT-Compatible Memory Controller generates the row and column decodes necessary to support the dynamic RAMs used in PC/AT-type systems. In addition, the device allows six motherboard memory options for the user, from 512K-bytes up to a full 8M-byte system. In addition, the VL82C202 provides the chip select for the ROM and RAM memory, and drives the system's speaker. The optional Shadow RAM feature allows up to 384K-bytes of memory space to be copied to and executed out of high speed DRAM instead of slower EPROM.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C202 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



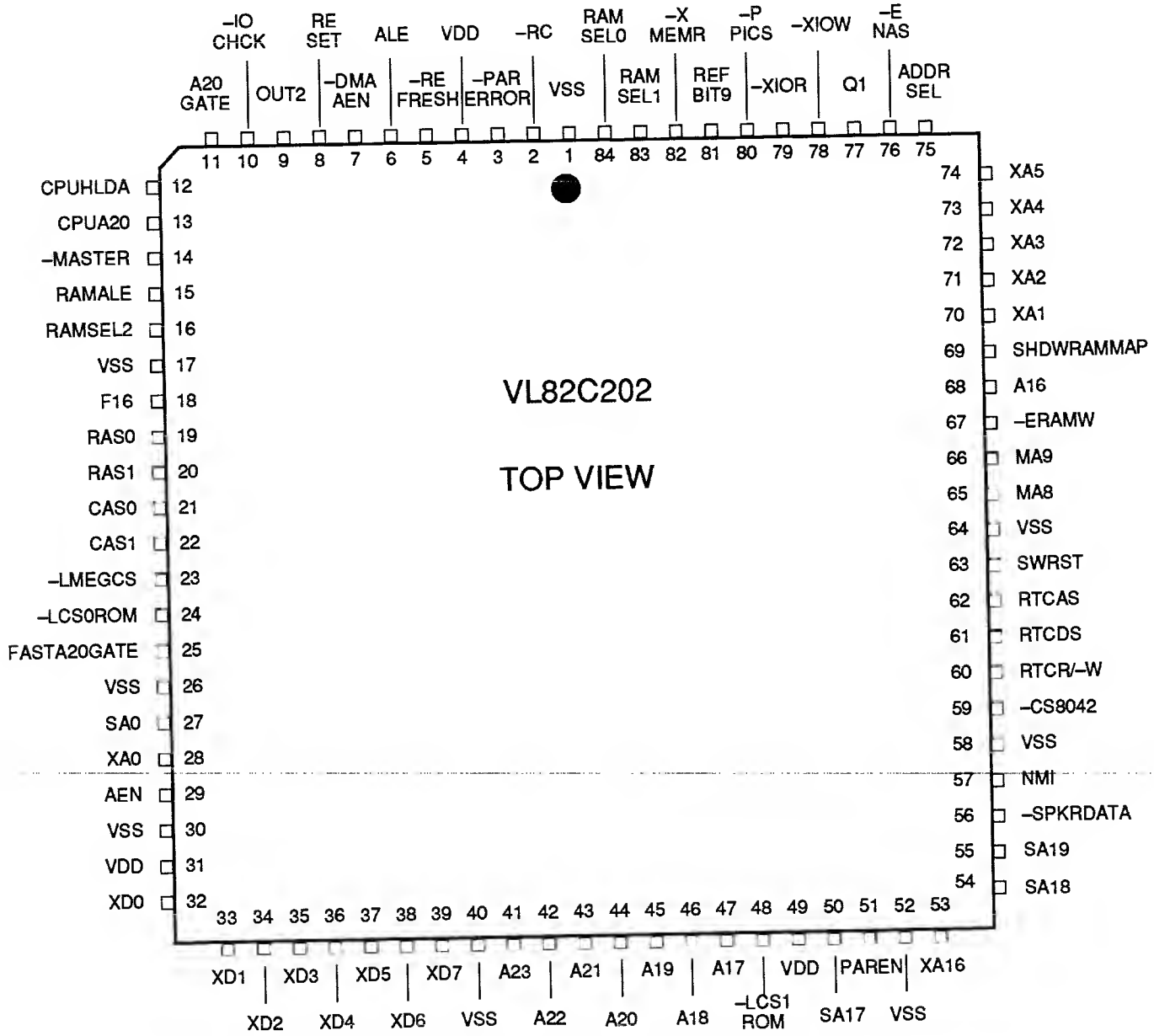
ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C202-16QC VL82C202-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C202-20QC VL82C202-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

4

PIN DIAGRAM


VL82C202
TOP VIEW
1 –IOCHCK
2 RESET
3 ALE
4 VDD
5 –RC
6 RAMSEL0
7 –XMEMR
8 –PPICS
9 –XIOW
10 –ENAS
11 A20GATE
12 OUT2
13 –DMAAEN
14 –REFRESH
15 –PARERROR
16 VSS
17 RAMSEL1
18 REFBIT9
19 –XIOR
20 Q1
21 ADDRSEL
22 XA5
23 XA4
24 XA3
25 XA2
26 XA1
27 SHDWRAMMAP
28 A16
29 –ERAMW
30 MA9
31 MA8
32 VSS
33 SWRST
34 RTCAS
35 RTCDS
36 RTCR/–W
37 –CS8042
38 VSS
39 NMI
40 –SPKRDATA
41 SA19
42 SA18
43 XA16
44 PAREN
45 VDD
46 A17
47 A19
48 A21
49 A23
50 XD7
51 XD5
52 XD3
53 XD1
54 XD2
55 XD4
56 XD6
57 VSS
58 A22
59 A20
60 A18
61 –LCS1ROM
62 SA17
63 VSS
64 XA0
65 SA0
66 VSS
67 VDD
68 XD0
69 FASTA20GATE
70 –LCS0ROM
71 –LMEGCS
72 CAS1
73 CAS0
74 RAS1
75 RAS0
76 F16
77 VSS
78 RAMSEL2
79 RAMALE
80 –MASTER
81 CPUA20
82 CPUHLDA

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–RC	2	I	This active low input signal will force a CPU reset when active. It is generated by the keyboard controller and its inverse is OR'ed with Port A bit 0 to form output signal SWRST (pin 63).
–PARERROR	3	I	Parity Error - A low true input used to indicate that a memory parity error has occurred.
–REFRESH	5	I	Refresh - An active low input used to initiate a refresh cycle for the dynamic RAMs.
ALE	6	I	Address Latch Enable - This is a positive edge input that controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle.
–DMAAEN	7	I	DMA Address Enable - This is an active low input. It is active whenever DMA is making an access to the system memory.
RESET	8	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK.
OUT2	9	I	Out 2 - The output of the timer controller. It can be read by the CPU on Port B.
–IOCHCK	10	I	I/O Channel Check - This active low input is asserted by devices on the expansion bus. It will generate a non-maskable interrupt if NMI is enabled. –IOCHCK can be read by the CPU on Port B.
A20GATE	11	I	A20 Gate - Used to select the proper value for address bit 20. CPUA20 is transmitted as A20 if A20GATE is high or Port A bit 1 is high, otherwise A20 is forced low.
CPUHLDA	12	I	CPU Bus Hold Acknowledge - This input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
CPUA20	13	I	CPU Address Bus Bit 20 - It is transmitted out as A20 if A20GATE is high or if Port A, bit 1 is high.
–MASTER	14	I	Master - An active low input. It is asserted low by devices on the expansion bus. A low indicates that another device is active.
RAMALE	15	I	RAMALE is used to latch RAM address buffers. It is forced high at the end of any bus cycle and will go back low at the end of the status cycle.
RAMSEL2	16	I	RAM Select 2 - Used with RAMSEL0 and RAMSEL1 to select the system RAM configuration.
F16	18	O	An output that indicates an access to on-board memory.
RAS0	19	O	An active high output used to enable the Row Address Strobe to DRAM banks 0 and 3.
RAS1	20	O	An active high output used to enable the Row Address Strobe to DRAM banks 1 and 2.
CAS0	21	O	An active high output used to enable the Column Address Strobe to DRAM banks 0 and 2.
CAS1	22	O	An active high output used to enable the Column Address Strobe to DRAM banks 1 and 3.
–LMEGCS	23	O	Lower Megabyte Chip Select - An active low output that indicates that the lower memory address space (0-1 megabyte) is selected.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–LCS0ROM	24	O	Latched Chip Select 0 for ROM - An active low output that is the latched chip select for the low 64K-bytes of ROM address space.
FASTA20GATE	25	O	This active high output is the OR of Port A bit 1 and input pin A20GATE.
SA0	27	I/O	System Address Bus Bit 0 - This signal will be an output with the value of XA0 when –DMAAEN is low. It will be an input and drive XA0 when –DMAAEN = 1.
XA0	28	I/O	Peripheral Address Bus Bit 0 - This signal is an output driven by SA0 when –DMAAEN = 1, and an input driving SA0 when –DMAAEN = 0.
AEN	29	O	Address Enable - This is an output signal for the expansion bus. It will go low when –MASTER is active or CPUHLDA is inactive.
XD0-XD7	32-39	I/O	Peripheral Data Bus Bits 0-7 - These are data bits for the peripheral bus. They are outputs when Port A or Port B is being read; otherwise they are inputs.
A16-A19, A21-A23	68, 47-45, 43-41	I	CPU Bus Bits 16-19 and 21-23 - These are the upper bits of the CPU address bus.
A20	44	I/O	Address Bus Bit 20 - Normally an output driven by CPUA20 (see above), but is an input when CPUHLDA = 1 and –MASTER = 1.
–LCS1ROM	48	O	Latched Chip Select 1 for ROM - The active low latched chip select output for the high 64K-bytes of ROM address space.
PAREN	51	O	Parity Check Enabled - Logical OR of CAS0 and CAS1, indicates a RAM memory access so parity check is enabled.
SA17-SA19	50, 54, 55	TSO	System Address Bus Bits 17-19 - A17-A19 are latched by ALE and transmitted out on these outputs when CPUHLDA is inactive. They are driven directly by A17-A19 when CPUHLDA is active and –MASTER is inactive. They are three-stated when –MASTER is active.
XA16	53	I	Peripheral Address Bus Bit 16 - This selects between 64K blocks of memory when CPUHLDA is high.
–SPKRDATA	56	O	Speaker Data - Output to be buffered and sent to the speaker.
NMI	57	O	Non-Maskable Interrupt - This output is the non-maskable interrupt signal for the CPU.
–CS8042	59	O	Chip Select Signal for the Keyboard Controller - This active low output is the chip select signal for the keyboard controller programmable interface device.
RTCR/–W	60	O	Real Time Clock Signal for Read/Write - This is the read/write select output signal for the real time clock. A high indicates a read operation and a low, a write operation.
RTCDS	61	O	Real Time Clock Data Strobe - This is the data strobe for the real time clock.
RTCAS	62	O	Real Time Clock Address Strobe - This is the address strobe for the real time clock.
SWRST	63	O	Software Reset - An active high output that goes to the System Controller chip, where it generates a reset pulse. SWRST is the logical OR of Port A bit 0 and the inverse of input –RC.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MA8, MA9	65, 66	O	DRAM Memory Address Bus Bits 8-9 - These outputs are the 8th and 9th bits of the DRAM memory address. They are located on the VL82C202 to allow system address mapping. REFBIT9 is multiplexed into MA8 during a refresh cycle.
–ERAMW	67	I	Early RAM Write - This active low input indicates a memory write command. It is used primarily during the mapping of the ROM into the Shadow RAM.
A16	68	I	CPU Address Bus Bit 16 - Used to select between 64K blocks when CPUHLDA is low.
SHDWRAMMAP	69	I	Shadow RAM Map - An active high input that selects the Shadow RAM Map option. Normally tied to VSS or VDD.
XA1-XA5	70-74	I	Peripheral Address Bus Bits 1-5 - Inputs used to decode addresses for Port A and Port B, peripheral control signals for the keyboard controller and the real time clock.
ADDRSEL	75	I	Address Select - This input is a multiplex row/column select for the Memory Address Bus drivers.
–ENAS	76	I	Enable Address Strobe - This active low input is used to enable the address strobe on the real time clock. It will go low the first time –S0 is asserted after a system reset.
Q1	77	I	Goes active during the second phase of a CPU bus cycle following the TS state. It is used by the VL82C202 chip to generate the address strobe for the real time clock.
–XIOW	78	I	Input/Output Write - The active low input indicates an I/O write command. Used to generate selects for the keyboard controller, real time clock, Port A and Port B.
–XIOR	79	I	Input/Output Read - The active low input indicates an I/O read command. Used to generate selects for the 8042, 146818, Port A and Port B.
–PPICS	80	I	Programmable Peripheral Interface Chip Select - An active low input used to generate the chip select for the keyboard coontroller.
REFBIT9	81	I	Refresh Bit 9 - The carry out of the refresh counter. It is used with the Address Buffer to generate a refresh for 1M DRAMs. It is multiplexed out as MA8 when –REFRESH is active.
–XMEMR	82	I	Memory Read - An active low input indicates a memory read command. This pin is used to determine the direction of data on the memory data bus and to clock in parity check results.
RAMSEL1	83	I	RAM Select 1 - This input is used with RAMSEL0 and RAMSEL 2 to designate the system RAM configuration.
RAMSEL0	84	I	RAM Select 0 - This input is used with RAMSEL1 and RAMSEL 2 to designate the system RAM configuration.
VDD	4, 31, 49		System Power: 5 V
VSS	1, 17, 26, 30 40, 52, 58, 64		System Ground

4

FUNCTIONAL DESCRIPTION

The VL82C202 Memory Controller provides address buffering for the upper address bits on the system and CPU address buses. It generates chip selects for the four possible RAM banks and the two possible ROM banks. The VL82C202 also contains Port A register bits 0 and 1 and the Port B register. It also generates chip select decodes for the keyboard controller and real time clock.

MEMORY DECODES

The upper address bits A16-A23 and XA16 are used to decode chip selects for all on-board memory. The three wire option inputs RAMSEL2, RAMSEL1, and RAMSEL0 are used to select one of six possible memory configurations. Refer to Figure 1.

RAM SELECTS

The memory mapping options shown in Figure 1 are used to generate the enable signals for the RAS and CAS pulses to the DRAMs. These signals will be active anytime the decode on address bits A16-A23 fall in the ranges shown in the memory maps. The signals are latched by the input signal RAMALE. The latches will be transparent while RAMALE is high and hold the value in the latch while RAMALE is low. The latch clocks will also be forced high when CPUHLDA is active making the latches transparent during all hold acknowledge operations.

When –REFRESH is active address bits A16-A23 are ignored and both RAS0 and RAS1 are forced active (high) while CAS0 and CAS1 are forced inactive (low).

MA8 AND MA9

A16-A23 are also used to generate the four address bits of the DRAM. These address bits are also latched by the combination of RAMALE and CPUHLDA as described for the RAM selects. The four latched address bits are then multiplexed out on MA8 and MA9. MA9 is needed only if a memory mapping option using 1M-bit DRAMs is selected. REFBIT9 is multiplexed out onto MA8 during refresh cycles.

ROM SELECTS

The ROM address space is decoded from A16-A23 and latched by ALE. These latches are also forced transparent when CPUHLDA is active in the same manner as the latches for the RAM chip selects. This latched value is then split into the two signals –LCS0ROM and –LCS1ROM using the A16 or XA16 inputs. If XA16 or A16 is low, –LCS0ROM will go active any time the ROM address space is decoded. If XA16 or A16 is high, –LCS1ROM is decoded. In this configuration –LCS0ROM selects the address space from 0E 0000 to 0E FFFF while –LCS1ROM selects the address space 0F 0000 to 0F FFFF.

The ROM address space is duplicated at FE 0000 to FF FFFF and the chip selects will go active in the same manner as described above in this address space.

UPPER ADDRESS BUFFERS

The VL82C202 provides buffer drive capability to drive the card slots on the signals SA17-SA19.

A17-A19 are latched by ALE and driven onto the SA17-SA19 bus whenever CPUHLDA is low. When CPUHLDA is high and –MASTER is high, the latch is bypassed and A17-A19 is driven directly to SA17-SA19. SA17-SA19 will be left floating when CPUHLDA is high and –MASTER is low.

ADDRESS BIT 20

Address bit 20 is handled differently than the other address bits. The A20 signal will be generated directly from CPUA20 (which should be connected to A20 on the 80286 CPU) if the input A20GATE is high or if Port A, bit 1 is set high. If A20GATE is low and Port A, bit 1 is low, the A20 signal is forced low.

ADDRESS BIT 0

A buffer transceiver between XA0 and SA0 is also provided on the VL82C202. If the input –DMAAEN is high, signal flow is from SA0 to XA0. If –DMAAEN is low, signal flow is from XA0 to SA0.

PORT A

The Port A register at address 92 hex contains two bits, b0 and b1. Bit 0, when set high, causes output SWRST to go high. Bit 1 provides the alternate A20 function and when set high, input CPUA20 is transmitted out as A20. If bit 1 and input A20GATE are both low, then output A20 is forced low.

Both bits are cleared on reset. When this register is read bits 2-7 are always forced low.

PORT B

The Port B register in an AT-compatible design is located on the VL82C202. It can be read or written to with an I/O command to address 61 hex. Port B is used to control the speaker and mask out NMI sources. It can be read to find status of –REFRESH, speaker data, and possible sources of NMI.

I/O DECODES

The VL82C202 provides the chip select signals for the on-board I/O peripherals (keyboard controller and real time clock).

NMI LOGIC

The logic necessary to control the Non-Maskable Interrupt (NMI) signal to the processor is contained in the VL82C202. An NMI can be caused by a parity error from the system board DRAM or if an I/O adapter pulls the input –IOCHCK low. These two possible sources can be individually enabled to cause an NMI by setting the appropriate bits in the Port B register. At power-up time, the NMI signal is masked off. NMI can be masked on by writing to I/O address 070 hex with bit 7 low, or masked off by writing to I/O address 070 hex with bit 7 high.

SHADOW RAM

In PC/AT-type memory systems, the memory space between 0A 0000h and 0F FFFFh is reserved for the graphics display buffer, the I/O adapter ROM and the system board ROM. VLSI's Shadow RAM option allows the system designer to copy these blocks into fast RAM memory for higher performance. The 384K-bytes are partitioned into six 64K blocks for maximum flexibility. When the memory is configured with Shadow RAM the selected blocks of 64K-bytes of RAM co-reside over the 64K-bytes of ROM or graphics buffer.

The Shadow RAM option is controlled by two 6-bit configuration registers and is selected by input pin 69, SHDWRAM-MAP tied high.

The two configuration registers, the Read Enable Register (RER) and the Write Protect Register (WPR), define whether an access to a block is to be treated normally (–LCSROMx and –LMEGCS are generated) or directed to Shadow RAM (F16 and CASx are generated), and if the block is writeable.

The two configuration registers are located at I/O address 09Fh. To prevent spurious access, eight consecutive writes to this address are required to "unlock" the registers. The ninth write places the configuration data in the RER and the tenth places data in the WPR. Both registers are cleared by RESET. A read of this address will access first the RER, then the WPR. See the text below for a complete description of these registers.

As an example of how to implement this feature, assume we want to map the BIOS at 0E 0000h to 0F FFFFh into Shadow Ram, define the blocks from 0A 0000h to 0B FFFFh as on-board RAM and leave blocks 0C xxxxh and 0D xxxxh as they are. First, read and write the entire address space between 0E 0000h and 0F FFFFh. Since the configuration registers are cleared by RESET, all reads are from ROM and all writes go to RAM (refer to Table 1). After the copying is complete with interrupts disabled, write eight times to 09Fh to unlock the configuration registers, then write data 33h (RER) and write again data 30H (WPR) to enable the blocks correctly. Now reads to blocks 0A xxxxh, 0B xxxxh, 0E xxxxh, and 0F xxxxh are from the RAM while accesses to blocks 0C xxxxh and 0D xxxxh are directed to the I/O channel. Writes to blocks 0A xxxxh and 0B xxxxh are allowed and writes to blocks 0E xxxxh and 0F xxxxh do not access the Shadow RAM since the Write Protect bits for these blocks have been set.

ACCESSING THE CONFIGURATION REGISTERS

The Read Enable Register (RER) and Write Protect Register (WPR) are located at I/O address 09Fh. The first –IOR to 09Fh accesses the RER and the next –IOR to the same address accesses the WPR. Additional reads follow this RER then WPR sequence. The bit that selects the next accessed register is cleared by Reset or by any –IOW.

Eight consecutive I/O writes to 09Fh are required to unlock the configuration registers. The ninth I/O write to 09Fh accesses the RER and the tenth the WPR. An internal counter keeps track of the number of I/O writes to address 09Fh. This counter is cleared by an –IOW to any address except 09Fh, by any –IOR or by RESET. It also clears on the tenth consecutive I/O write to this address (i.e., after both registers have been written). These registers are cleared on RESET (except for bits 6 and 7, which are unused and always read out high).

SYSTEM TESTING

The VL82C202 offers a test mode that allows the system designer to three-state all output and I/O pins. Unused memory select options 000 or 100 force this mode.

4

TABLE 1. SHADOW RAM

SHDW RAMMAP	–ERAM W	Read Enable Register Bit	Write Protect Register Bit	Address = 0A 0000 - 0F FFFF Address = FE 0000 - FF FFFF F16 (Note 1)	RAS x	CAS x	–LCS ROM X (Note 2)	–LMEG CS	Comments
0	X	X	X	0	0	0	0	0	Shadow Mode Not Selected, Normal Access
1	0	0	0	0	1	1	1	0	Slow Shadow RAM Write
1	0	0	1	0	1	0	1	0	Slow Shadow RAM Write (Protected)
1	0	1	0	1	1	1	1	1	Fast Shadow RAM Write
1	0	1	1	1	1	0	1	1	Fast Shadow RAM Write (Protected)
1	1	0	0	0	1	0	0	0	Normal Read
1	1	0	1	0	1	0	0	0	Normal Read
1	1	1	0	1	1	1	1	1	Fast Shadow RAM Read
1	1	1	1	1	1	1	1	1	Fast Shadow RAM Read

Notes: 1. F16 is always generated by blocks 0E 0000 - 0F FFFF and FE 0000 - FF FFFF.
2. –LCSROMx is active only for blocks 0E 0000 - 0F FFFF and FE 0000 - FE FFFF.

TABLE 2. SHADOW RAM CONFIGURATION REGISTERS

	b7	b6	b5	b4	b3	b2	b1	b0
Read Enable Register	1	1	F	E	D	C	B	A
Write Protect Register	1	1	F	E	D	C	B	A

- A → Selects Block 0A xxxx
- B → Selects Block 0B xxxx
- C → Selects Block 0C xxxx
- D → Selects Block 0D xxxx
- E → Selects Block 0E xxxx, FE xxxx
- F → Selects Block 0F xxxx, FF xxxx

FIGURE 1. SUPPORTED DRAM CONFIGURATIONS AND RAS/CAS GENERATION

MEMORY ADDRESS (64K BLOCKS)	TOTAL DRAM		512K BYTES		1M BYTES		2M BYTES			2M BYTES		4K BYTES		8M BYTES	
	DRAM TYPE		256K		256K		256K			1M		1M		1M	
	NO. OF DRAMS		18		36		72			18		36		72	
	RAMSEL (2, 1, 0)	000	001		010 (1)		011		100	101		110		111	
	SHDW RAM MAP	X	0	1	0	1	0	1	X	0	1	0	1	0	1
	00-07	TEST MODE	RAS0 CAS0	N/U	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	TEST MODE	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0
	08-09				RAS1 CAS1	RAS1 CAS1	RAS1 CAS0	RAS1 CAS0							
	0A-0D					RAS1* CAS1		RAS1* CAS1			RAS0* CAS0		RAS1* CAS1		RAS1* CAS1
	0E-0F				ROM		ROM			ROM		ROM		ROM	
	10-13				RAS1 CAS1		RAS1 CAS0	RAS1 CAS0							
	14-15														
	16-1D						RAS0 CAS1	RAS0 CAS1		RAS0 CAS0		RAS0 CAS0	RAS0 CAS0	RAS0 CAS0	RAS0 CAS0
	1E-1F							RAS1 CAS1							
	20-23						RAS1 CAS1								
	24-25														
	26-3F											RAS1 CAS1	RAS1 CAS1	RAS1 CAS0	RAS1 CAS0
	40-45														
	46-65													RAS0 CAS1	RAS0 CAS1
	66-7F														RAS1 CAS1
	80-85													RAS1 CAS1	

*See Shadow RAM description.

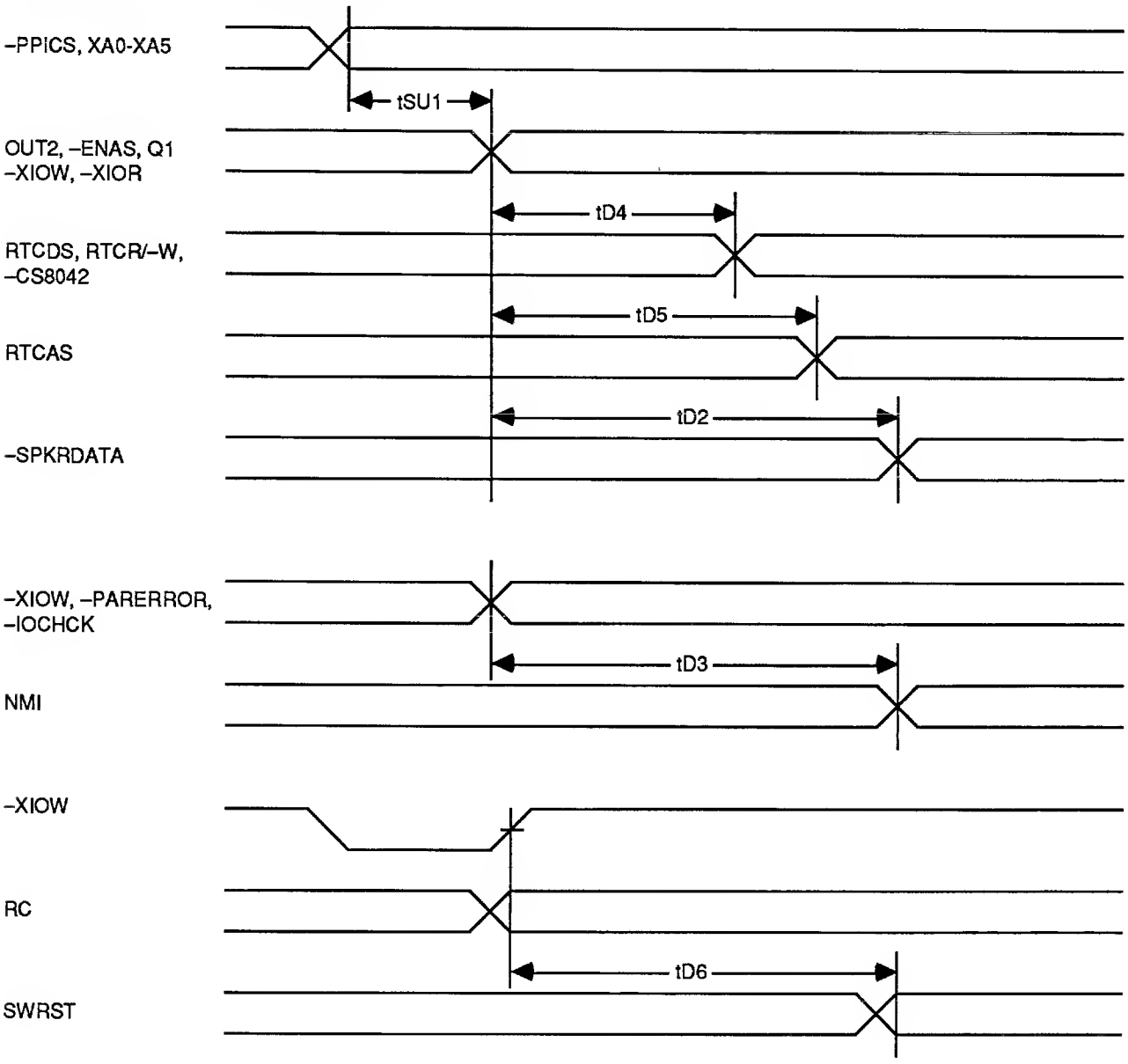
(1) This map is also useable for a 64K-byte map using a combination of 256K and 64K DRAMs.

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ± 5%, VSS = 0 V

PERIPHERAL CONTROL TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU1	–PPICS, XA Setup to –XIOW	8		8		ns	
tD2	SPKRDATA Output Delay		40		40	ns	CL = 50 pF
tD3	NMI Output Delay		40		40	ns	CL = 100 pF
tD4	RTCDS, RTCR/–W, –CS8042 Output Delay		30		30	ns	CL = 50 pF
tD5	RTCAS Output Delay		35		35	ns	CL = 50 pF
tD6	SWRST Delay		40		40	ns	CL = 50 pF

PERIPHERAL CONTROL TIMING WAVEFORMS

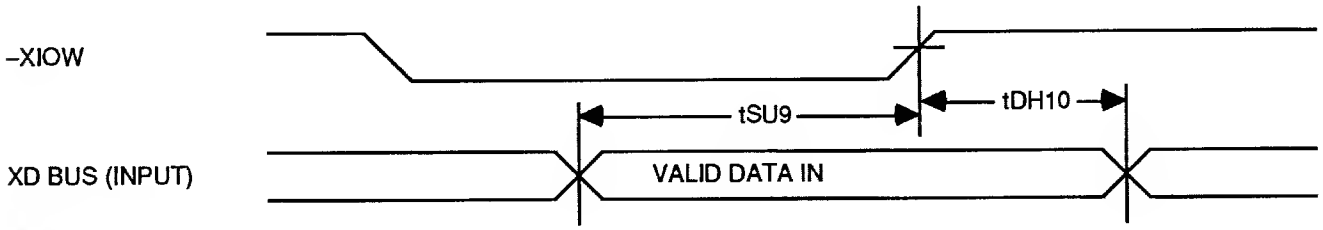


XD BUS TIMING

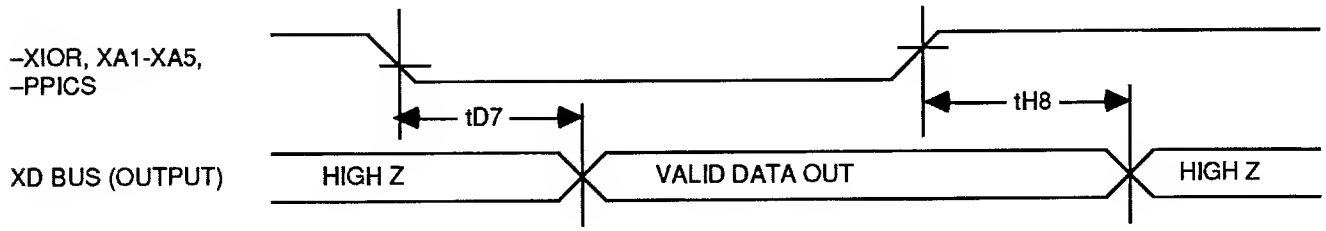
Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD7	XD Bus Delay		40		40	ns	XD = Output
tH8	XD Bus Hold Time	6		6		ns	XD = Output
tSU9	XD Bus Setup Time	20		20		ns	XD = Input
tH10	XD Bus Hold Time	12		12		ns	XD = Input

XD BUS TIMING WAVEFORMS

Input



Output



ADDRESS CONTROL TIMING

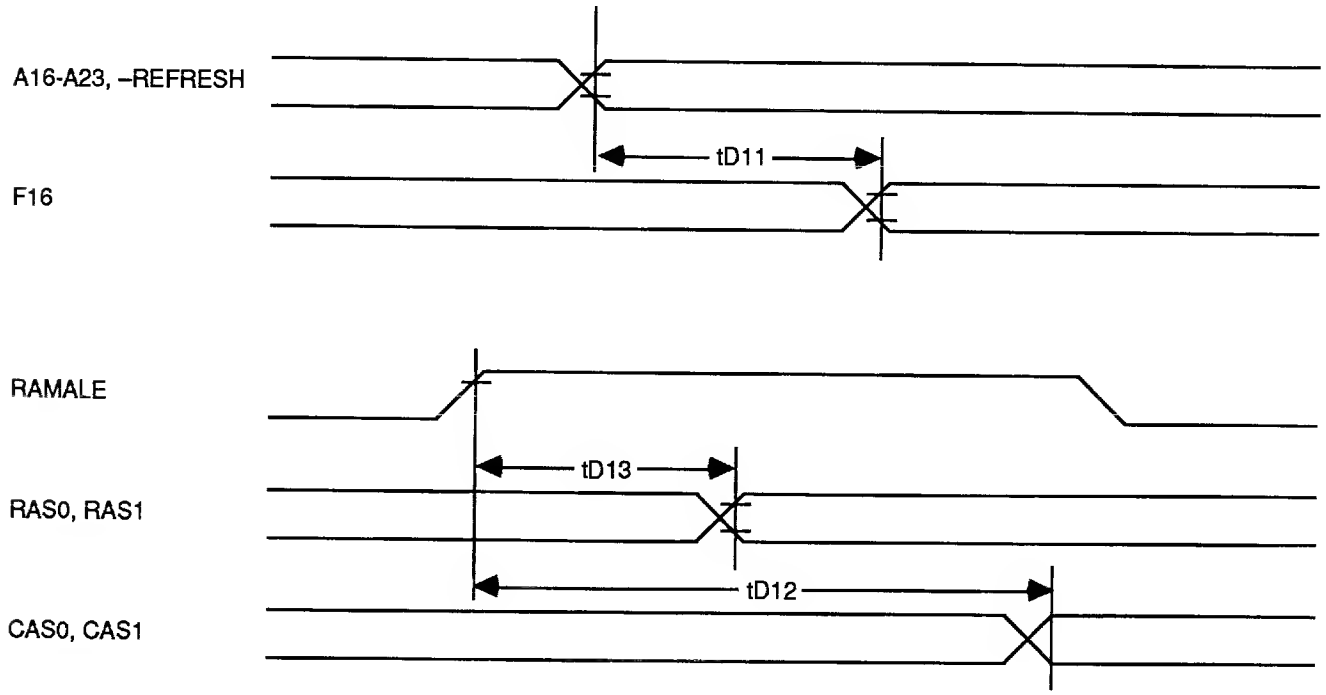
Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD11	F16 Output Delay		25		21	ns	CL = 50 pF
tD12	CAS0, CAS1 Delay from RAMALE		30		20	ns	CL = 50 pF
tD13	RAS0, RAS1 Delay from RAMALE		18		18	ns	CL = 50 pF
tD14	–LMEGCS Delay from ALE		25		22	ns	CL = 50 pF
tD15	–LCS1ROM, –LCS0ROM Delay from ALE		25		25	ns	CL = 50 pF
tD16	AEN Output Delay		30		30	ns	CL = 150 pF
tD17	CAS Delay from –ERAMW in Shadow Mode		17		13	ns	
tD18	–LCSxROM Delay from –ERAMW		28		28	ns	

Note: RAMSEL0, RAMSEL1, and RAMSEL2 are assumed setup one processor clock before the user generates any memory control signals. If the test mode is not used, these pins are usually strapped to VDD or VSS.

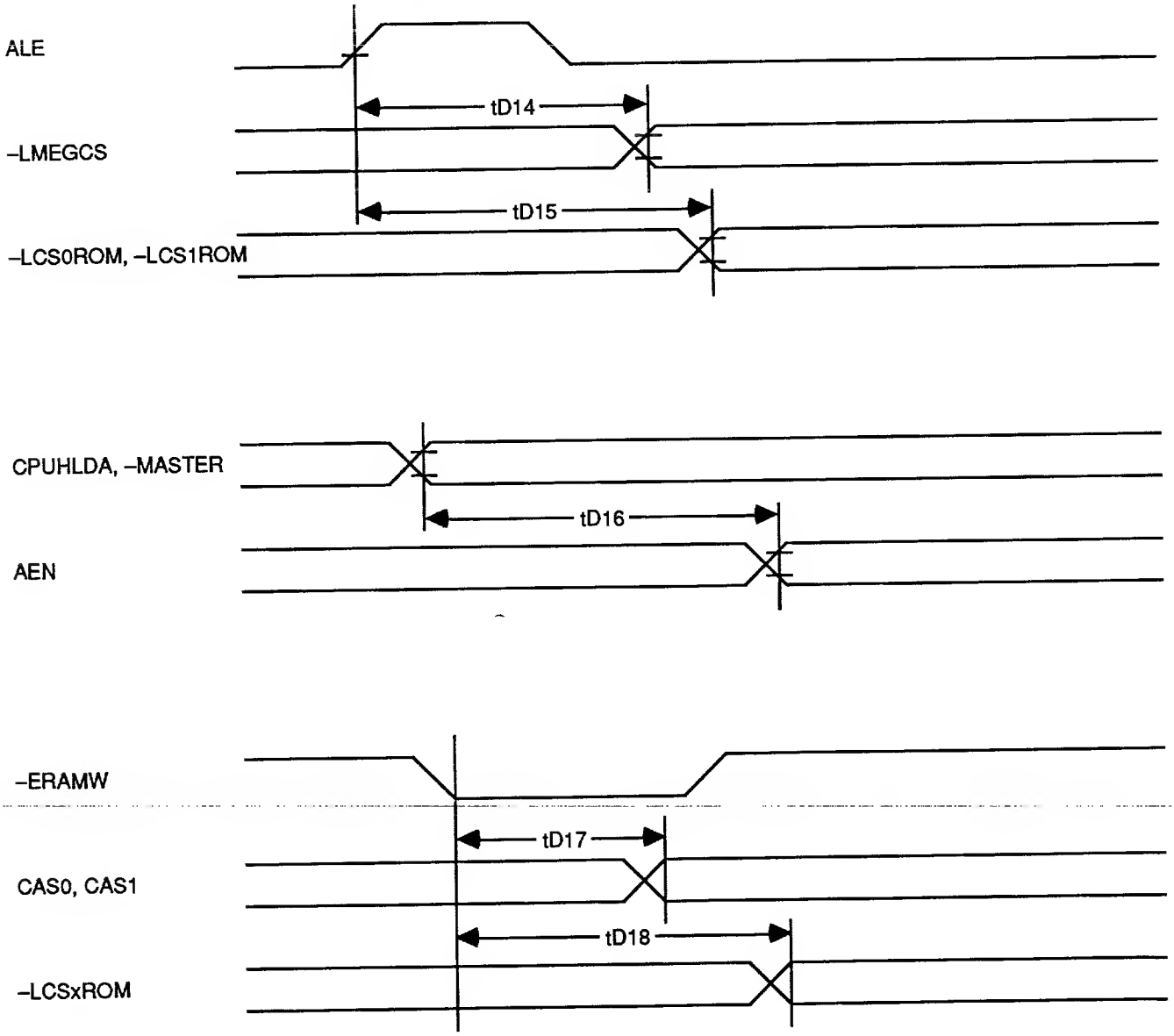
Input SHDWRAMMAP should be tied to VDD or VSS.

4

ADDRESS CONTROL TIMING WAVEFORMS



ADDRESS CONTROL TIMING WAVEFORMS (Cont.)



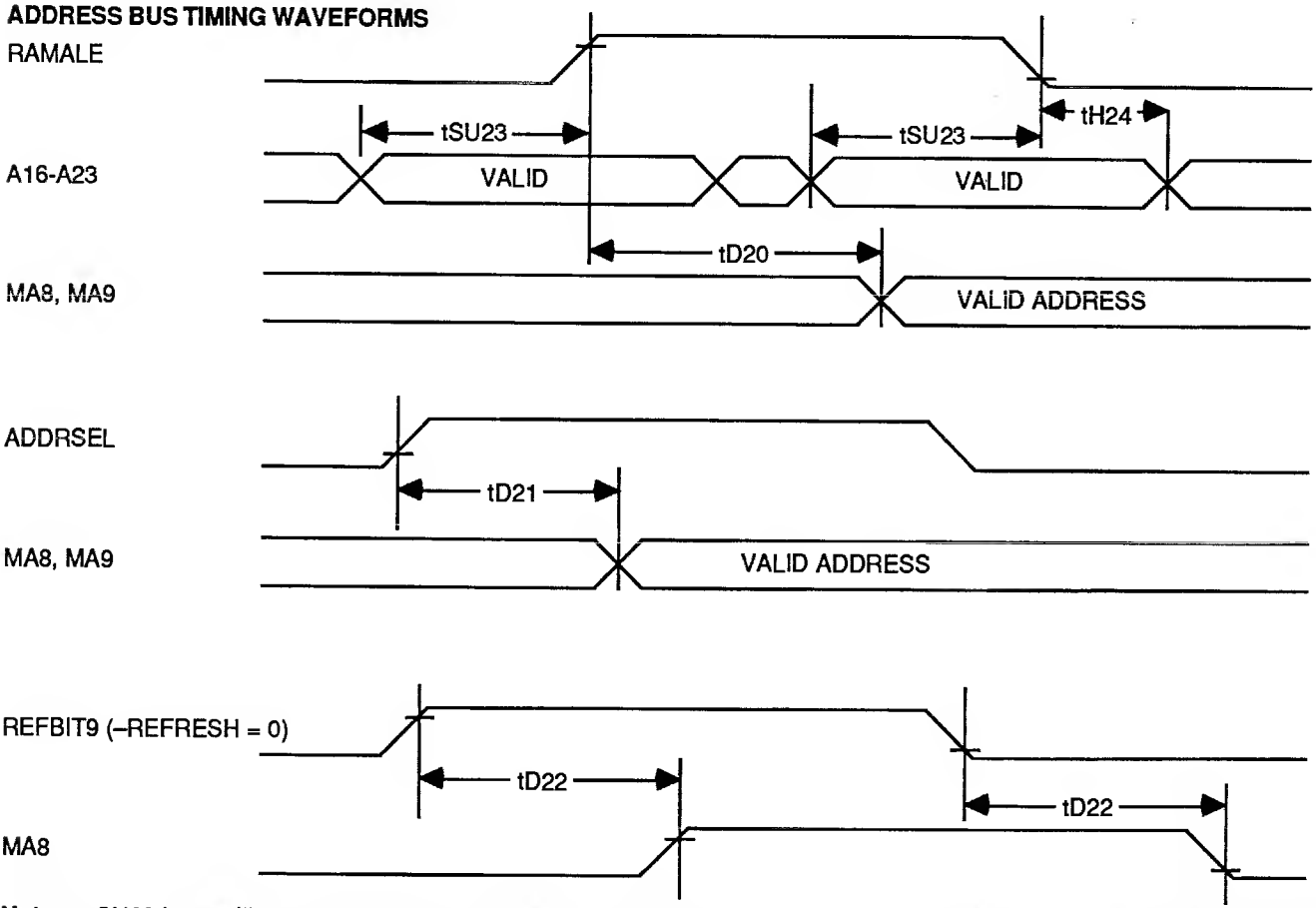
ADDRESS BUS TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD20	MA8, MA9 Delay from RAMALE		22		18	ns	
tD21	MA8, MA9 Delay from ADDRSEL		17		17	ns	Note
tD22	MA8 Delay from REFBIT9		25		25	ns	–REFRESH = 0
tSU23	A16-A23 Setup to ALE, RAMALE	25		25		ns	
tH24	A16-A23 Hold	10		10		ns	
tD25	XA0/SA0 Delay		35		35	ns	CL = 200 pF SA0, CL = 100 pF XA0
tD26	SA17-SA19		40		35	ns	CL = 200 pF SA0, CPUHLDA = 1, –MASTER = 1
tD27	SA17-SA19 Delay from ALE		35		30	ns	CPUHLDA = 0
tD28	A20 Delay		35		30	ns	CL = 50 pF

Note: tD21 delay may be derated by a factor of .04 ns/pF for heavier loads.

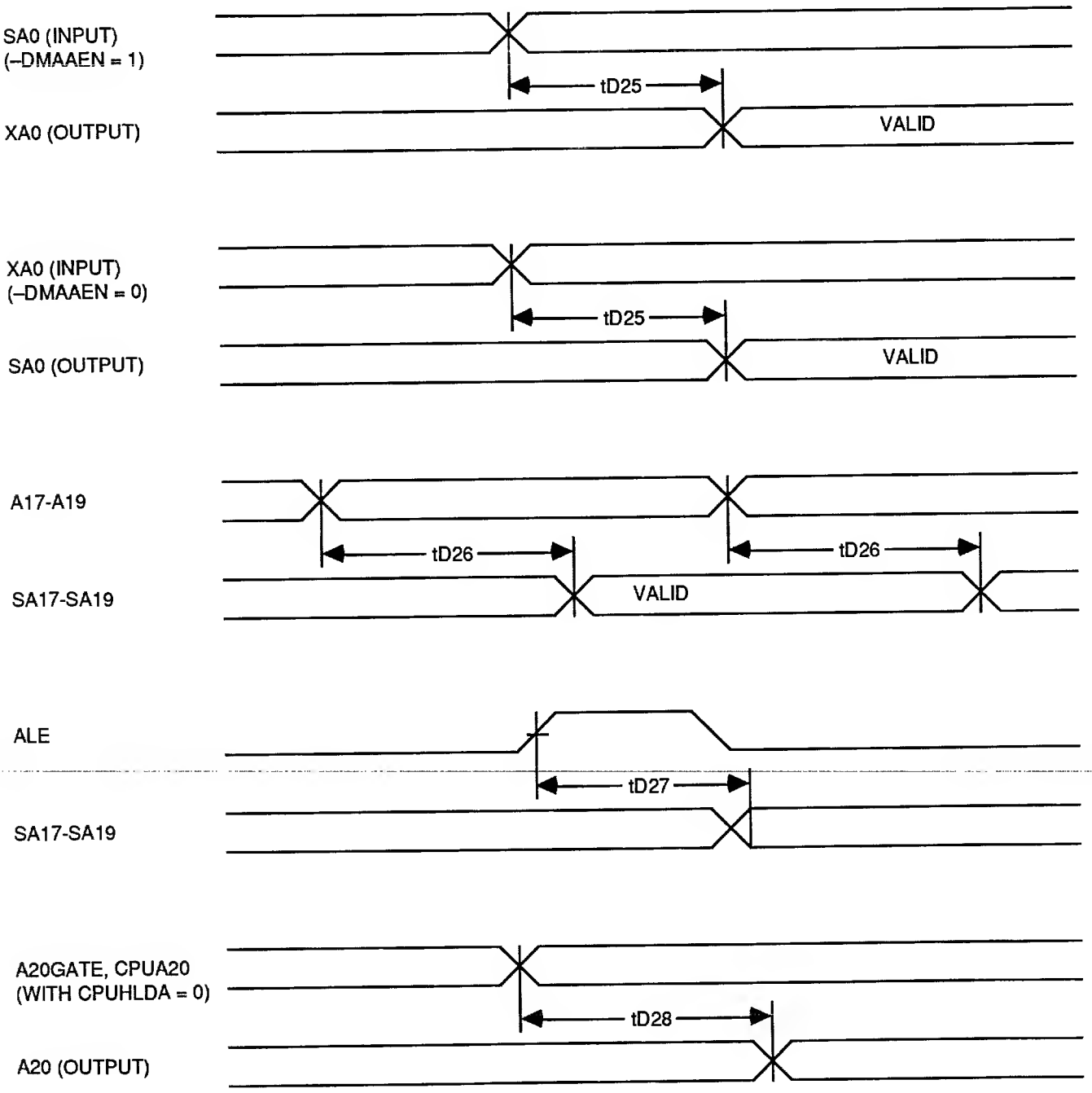
4

ADDRESS BUS TIMING WAVEFORMS



Note: tSU23 is specified with respect to the falling edge of RAMALE to guarantee the correct address decodes will be latched in. tSU23 is shown with respect to the rising edge of RAMALE to show time required for address decodes such that propagation delays tD20 and tD13 will be valid. The time does not have to be met with respect to the rising edge for correct functionality.

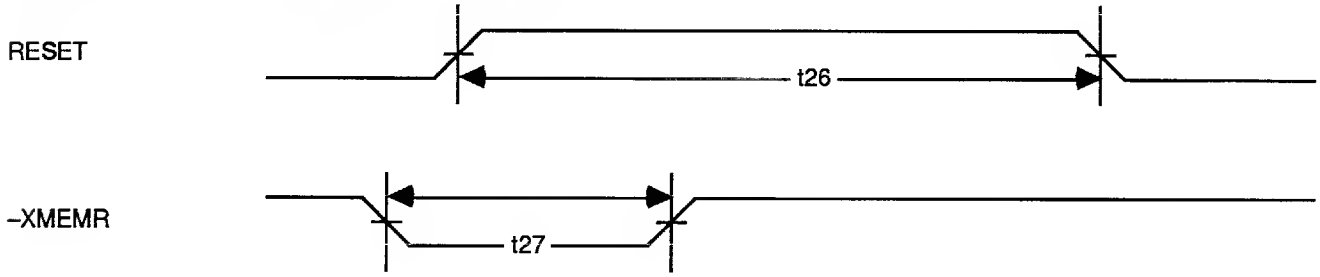
ADDRESS BUS TIMING WAVEFORMS (Cont.)



MISCELLANEOUS INPUT TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t26	Min High (Active) Time on RESET	100		100		ns	
t27	Min Low Time for –XMEMR	40		40		ns	

MISCELLANEOUS INPUT TIMING WAVEFORMS

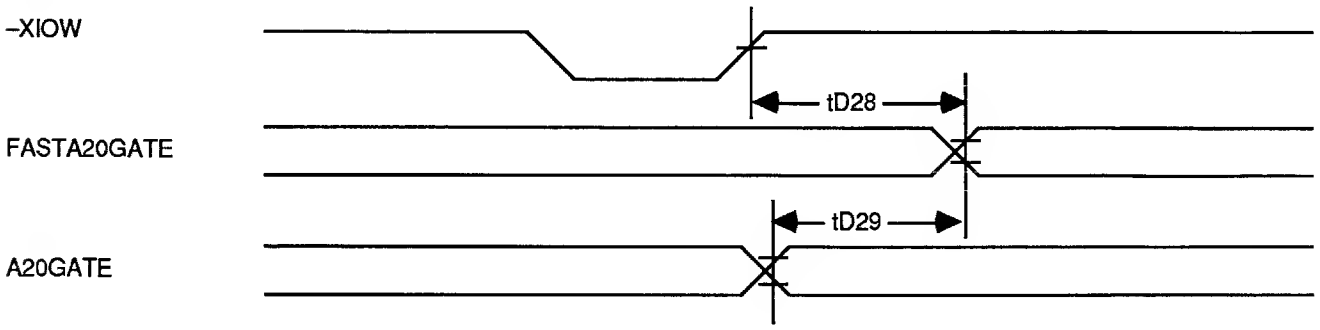


4

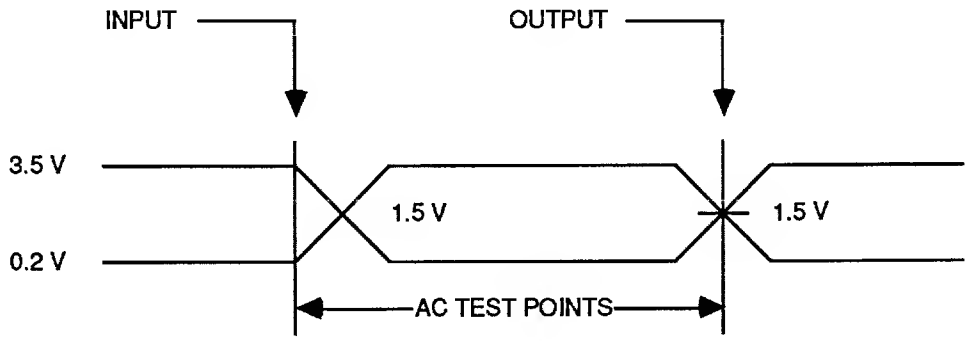
FASTA20GATE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tD28	FASTA20GATE Delay from –XIOW		40		40	ns	I/O Write to Port A, CL = 50 pF
tD29	FASTA20GATE Delay from A20GATE		35		35	ns	CL = 50 pF

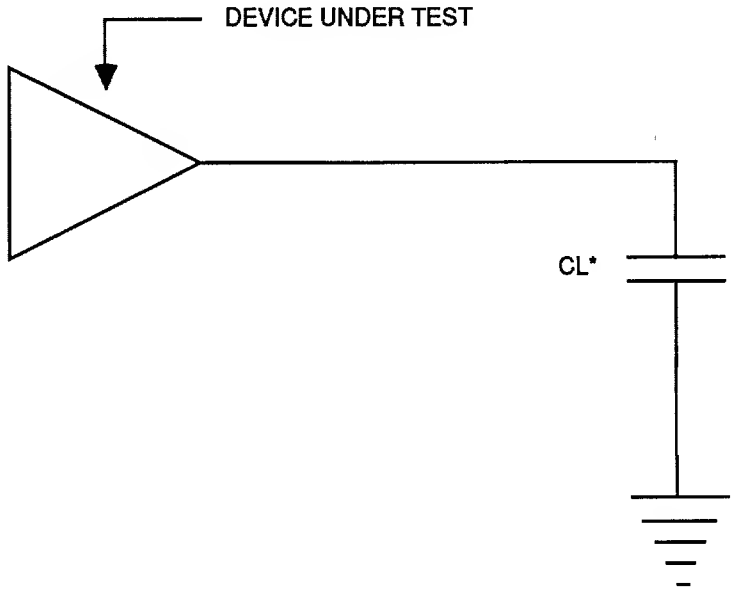
FASTA20GATE TIMING WAVEFORMS



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
27, 29, 50, 54, 55	200
65, 66	150
28, 32-39	100
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C, to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	SA0, SA17-SA19, AEN, CL = 200 pF, IOL = 20 mA
VOL2	Output Low Voltage		0.45	V	MA8, MA9, CL = 150 pF, IOL = 8 mA
VOL3	Output Low Voltage		0.45	V	F16, XA0, XD0-XD7, CL = 100 pF, IOL = 8 mA
VOL4	Output Low Voltage		0.45	V	All Other Pins, CL = 50 pF, IOL = 2 mA
VIH	Input High Voltage	3.8	VDD + 0.5	V	ALE, RAMALE
VIL	Input Low Voltage	–0.5	0.6	V	ALE, RAMALE
VIHC	Input High Voltage	2.0	VDD + 0.5	V	All Other Pins
VILC	Input Low Voltage	–0.5	0.8	V	All Other Pins
CO	Output Capacitance		16	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		25	mA	Note

Note: Inputs = VSS or VDD, outputs are not loaded.

NOTES:

VL82C203

PC/AT-COMPATIBLE ADDRESS BUFFER

FEATURES

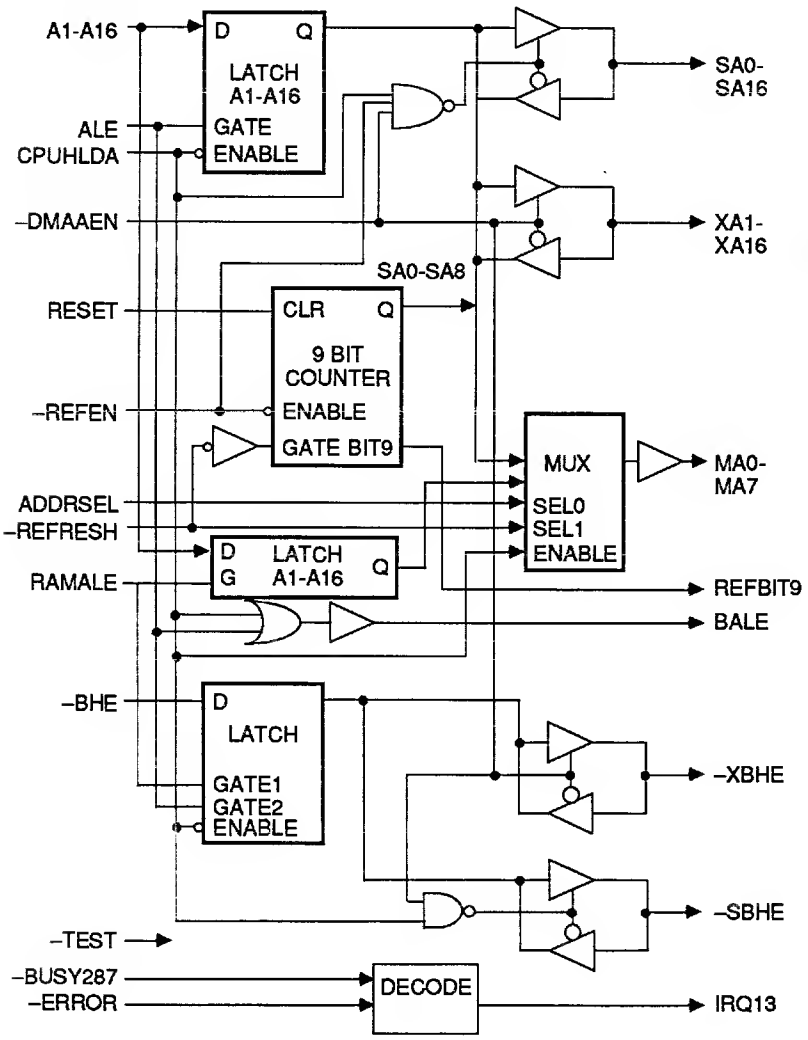
- Fully compatible with IBM PC/AT-type designs
- Completely performs address buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C203 PC/AT-Compatible Address Buffer provides the system with a 16-bit address bus input from the CPU to 41 buffered drivers. The buffered drivers consist of 17 bidirectional system bus drivers, each capable of sinking 24 mA (60 'LS loads) of current and driving 200 pF of capacitance on the backplane; 16 bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and eight memory bus drivers, also capable of sinking 8 mA of current. On-chip refresh circuitry supports both 256K-bit and 1M-bit DRAMs. The VL82C203 provides addressing for the I/O slots as well as the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C203 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



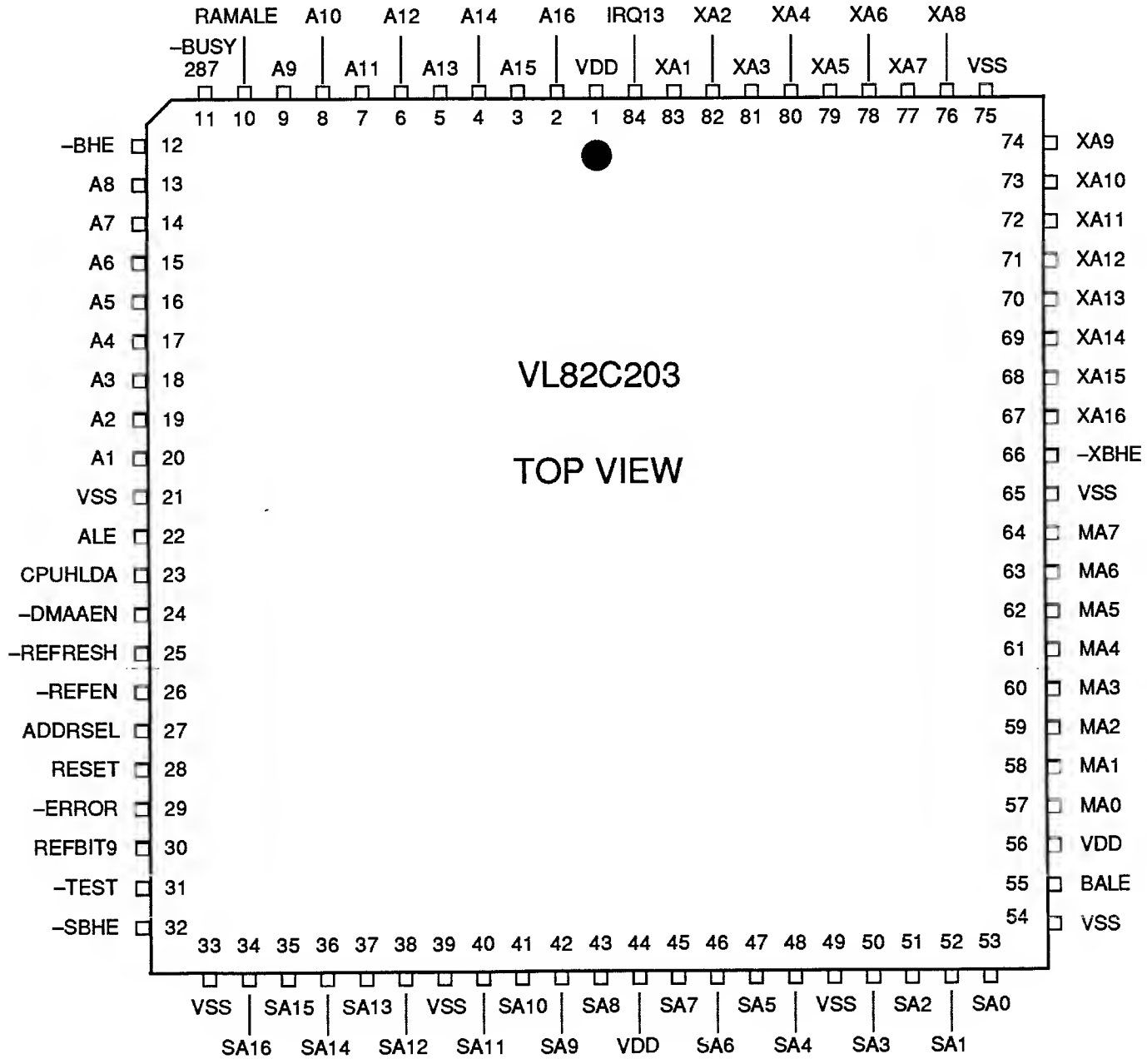
ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C203-16QC VL82C203-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C203-20QC VL82C203-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

4

PIN DIAGRAM


RAMALE 11
A10 10
A12 9
A14 8
A16 7
IRQ13 6
XA2 5
XA4 4
XA6 3
XA8 2
–BUSY 287
A9 1
A11 84
A13 83
A15 82
VDD 81
XA1 80
XA3 79
XA5 78
XA7 77
VSS 76
–BHE 12
A8 13
A7 14
A6 15
A5 16
A4 17
A3 18
A2 19
A1 20
VSS 21
ALE 22
CPUHLDA 23
–DMAAEN 24
–REFRESH 25
–REFEN 26
ADDRSEL 27
RESET 28
–ERROR 29
REFBIT9 30
–TEST 31
–SBHE 32
74 XA9
73 XA10
72 XA11
71 XA12
70 XA13
69 XA14
68 XA15
67 XA16
66 –XBHE
65 VSS
64 MA7
63 MA6
62 MA5
61 MA4
60 MA3
59 MA2
58 MA1
57 MA0
56 VDD
55 BALE
54 VSS
VL82C203
TOP VIEW
33 VSS
34 SA16
35 SA15
36 SA14
37 SA13
38 SA12
39 VSS
40 SA11
41 SA10
42 SA9
43 SA8
44 VDD
45 SA7
46 SA6
47 SA5
48 SA4
49 VSS
50 SA3
51 SA2
52 SA1
53 SA0

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
A1-A16	20-13, 9-2	I	CPU Address Bus Bits 1-16 - The lower 16 bits of the CPU address bits. These are multiplexed to the system address bus for the slots SA1-SA16, the memory address bus MA0-MA7, and the peripheral address bus XA1-XA16.
RAMALE	10	I	RAM Address Latch Enable - RAMALE is used to latch RAM address buffers. It is forced high at the end of any bus cycle. This allows the address for the next bus cycle to be passed to the system memory sooner than the ALE signal. RAMALE will go back low at the end of the status cycle for any bus cycle to latch the memory address until the end of the bus cycle. The memory address latches are open when RAMALE is in the high state.
–BUSY287	11	I	Busy 287 - This active low input is asserted by the 80287 to indicate that it is currenty executing a command.
–BHE	12	I	Bus High Enable - This is the active low input signal from the 80286 microprocessor which is used to indicate a transfer of data on the upper byte on the data bus, D8-D15.
ALE	22	I	Address Latch Enable - This positive edge input controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle. All latches are open when ALE is in the high state.
CPUHLDA	23	I	CPU Hold Acknowledge - This active high input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
–DMAAEN	24	I	DMA Address Enable - This is an active low input which is active whenever an I/O device is making a DMA access to the system memory.
–REFRESH	25	I	Refresh - An active low input which is used to initiate a refresh cycle for the dynamic RAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle.
–REFEN	26	I	Refresh Enable - An active low input that will be asserted when a refresh cycle is needed for the DRAMs.
ADDRSEL	27	I	Address Select - This is a multiplex select for the memory address bus drivers. When ADDRSEL is low, the lower order address bits are selected. When high, the high order address bits are selected.
RESET	28	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK and used to reset the refresh counter.
–ERROR	29	I	Error - This is an active low input which indicates an error has occurred within the 80287 coprocessor.
REFBIT9	30	I	Refresh Bit 9 - This is the MSB of the refresh counter. When used with the Memory Controller chip a refresh address will be generated for 1M byte DRAMs.
–TEST	31	I	Test - This is an active low input which is used to three-state all outputs of the VL82C203 device. This is for system level test where it is necessary to overdrive the outputs of the VL82C203. When –TEST is low, all outputs and bidirectional pins of the VL82C203 will be three-stated. This pin should be pulled up via a 10K Ω pull-up resistor in a standard system configuration.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SBHE	32	I/O	System Bus High Enable - This is the system I/O signal used to indicate transfer of local data on the upper byte on the local data bus, D8-D15. –SBHE is active low and will be in input mode during bus hold acknowledge.
SA0-SA16	53-50, 48-45 43-40, 38-34	O	System Address Bus Bits 0-16 - SA0 will be active only during a refresh cycle otherwise it will be three-stated (input mode).
BALE	55	O	Buffered Address Latch Enable - An active high output that is used to latch valid addresses and memory decodes from the 80286. System addresses SA0–SA16 are latched on the falling edge of BALE. During a DMA cycle BALE is forced active high.
MA0-MA7	57-64	O	DRAM Memory Address Bus Bits 0-7 - This 8-bit output is multiplexed using ADDRSEL to give a full 16-bit address.
XA1-XA16	83-76, 74-67	I/O	Peripheral Address Bus Bits 1-16 - These I/Os are used to control the coprocessor, keyboard, ROM memory and the DMA controllers.
–XBHE	66	I/O	Transfer Byte High Enable - This is an active low I/O used to allow the upper data byte to be transferred through the bus transceivers.
IRQ13	84	O	This is an active high output which indicates an error has occurred within the 80287 coprocessor.
VDD	1, 44, 56		System Supply: 5 V
VSS	21, 33, 39 49, 54, 65, 75		System Ground

FUNCTIONAL DESCRIPTION

The VL82C203 is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Address Buffer replaces several bus transceivers and address data latches located within the PC/AT-type system. The DRAM refresh circuitry is also located on this device.

The primary function of the Address Buffer is to multiplex the 80286 microprocessor address lines (A1-A16) to the system address bus (SA0-SA16), the peripheral address bus (XA1-XA16), and the memory address bus (MA0-MA7). This is accomplished through positive edge triggered latches and a group of data multiplexers. The two groups of latches can be seen in the block diagram of the device. One set of latches have their output enabled with CPUHLDA and are gated with ALE. This set of latches drive the SA and XA bus outputs. Another parallel set of latches are multiplexed into the MA lines and are gated with RAMALE. RAMALE is an early ALE signal. This allows more setup time for the address to be multiplexed to the DRAMs. If the VL82C203 is not used in conjunction with the other PC/AT-devices, RAMALE and ALE should be wired together to provide maximum PC/AT-compatibility.

The device also provides for address flow between the SA, XA, and MA buses and the –XBHE and –SBHE signals. The –XBHE signal is gated with the RAMALE input while the –SBHE is gated with the ALE input. This control flow is arbitrated with the CPUHLDA, –DMAAEN, and –REFEN inputs and is shown in Table 1.

TABLE 1. INTERNAL BUS CONTROL DECODE

CPU HLDA	–DMA AEN	–REF EN	A	SA	XA	MA	–XBHE	–SBHE
0	X	X	I	O	O	O	O	O
1	0	1	I	O	I	O	I	O
1	1	0	I	O	O	O	O	I
1	1	1	I	I	O	O	O	I

I = Input Mode
O = Output Mode
X = Don't Care

Memory addresses are multiplexed from the SA and A bus sources and are controlled via the CPUHLDA, –REFRESH, and ADDRSEL inputs. The mapping and control is shown in Table 2.

A 9-bit refresh counter is provided on this device. This allows support for DRAMs of up to 1M bit in size. The refresh counter is clocked on the rising edge of the –REFRESH input. A latched register inside the counter latches in the current state of the counter on the falling edge of –REFEN and transfers this value to the internal bus which routes to the SA and MA bus outputs. The SA0 output is provided only for refresh purposes and is driven only during this time. During a refresh the SA and MA bus outputs are driven from the output of the refresh counter latch Q0-Q8. Refer to Table 3 for the mapping of the refresh counter to the bus lines.

Note that all SA bus lines are driven during a refresh cycle. ADDRSEL is not normally toggled during a refresh cycle but is shown in Table 3 for completeness of the logic implementation. The REFBIT9 signal is the Q8 output of the refresh counter. This is required only for the refresh of 1M bit DRAMs.

TABLE 2. MEMORY ADDRESS MAPPING

Mux Control Input			MA Bus	
CPUHLDA	–REFRESH	ADDRSEL	MA7	MA0-MA6
1	0	0	SA8	SA1-SA7
1	0	1	SA16	SA9-SA15
0	X	0	A8	A1-A7
0	X	1	A16	A9-A15

X = Don't Care

TABLE 3. REFRESH ADDRESS MAPPING

Mux Control Input			MA Bus		SA Bus	
CPU HLDA	–REF EN	ADDR SEL	MA7	MA0-MA6	SA9-SA15	SA0-SA8
1	0	0	Q0	Q1-Q7	0	Q0-Q8
1	0	1	0	0	0	Q0-Q8

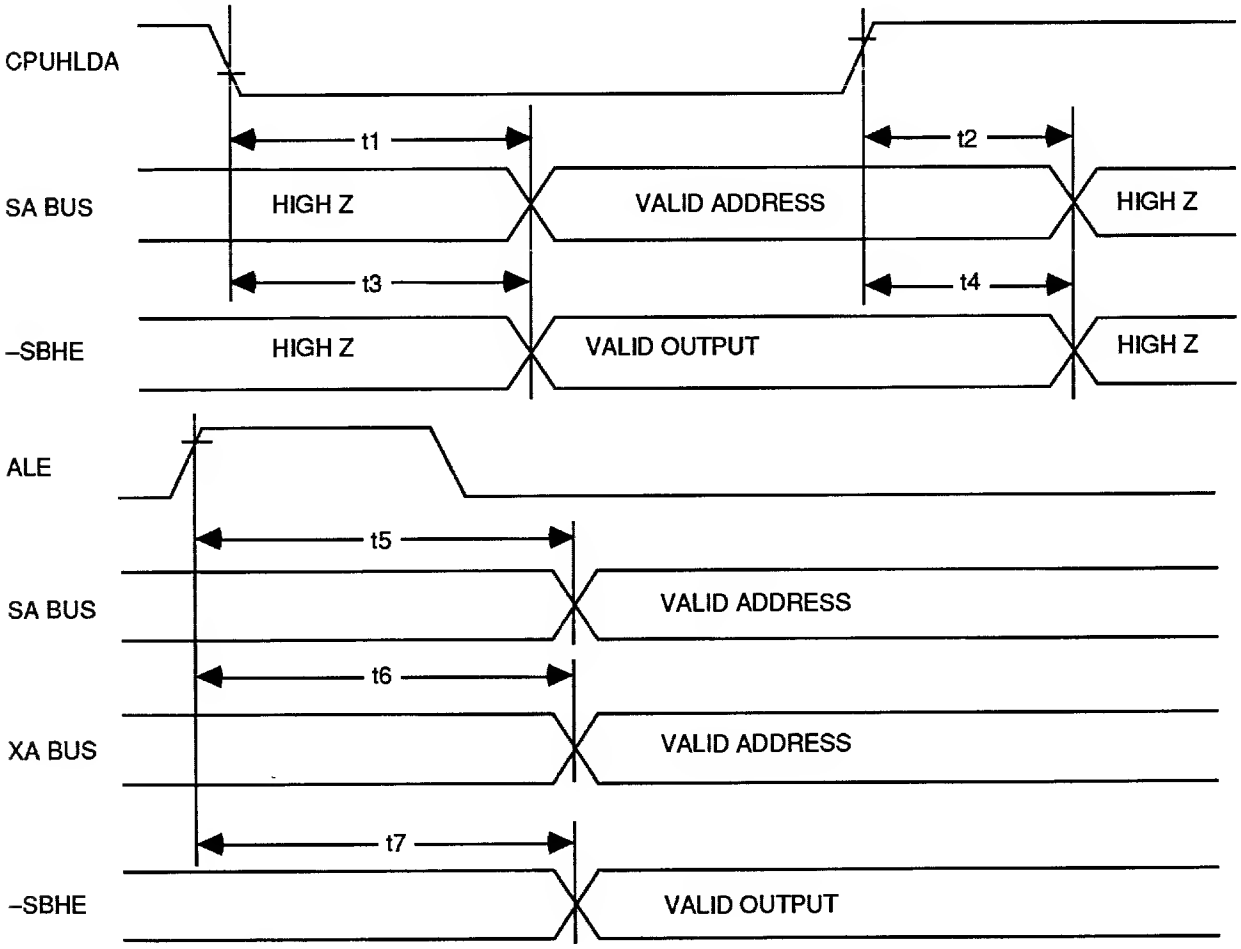
The –TEST pin has been added to enhance system level testing of the VL82CPCAT-16/-20 chip sets. When this pin is active (0), all outputs and bidirectional pins are placed in three-state. This allows a board level test system to overdrive outputs of the VL82C203 without damage to the device. When –TEST is active, the internal bus is driven to the state of the system address bus (SA0-SA16).

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ± 5%, VSS = 0 V

CPU MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t1	CPUHLDA to SA Bus from High Z to Valid Add Out		35		35	ns	
t2	CPUHLDA to SA Bus High Z State		35		35	ns	
t3	CPUHLDA to –SBHE from High Z to Valid Out		35		35	ns	
t4	CPUHLDA to –SBHE High Z State		35		35	ns	
t5	ALE to SA Bus Valid Address		40		40	ns	CL = 200 pF
t6	ALE to XA Bus Valid Address		40		40	ns	CL = 100 pF
t7	ALE to –SBHE Bus Valid Address		40		40	ns	CL = 200 pF

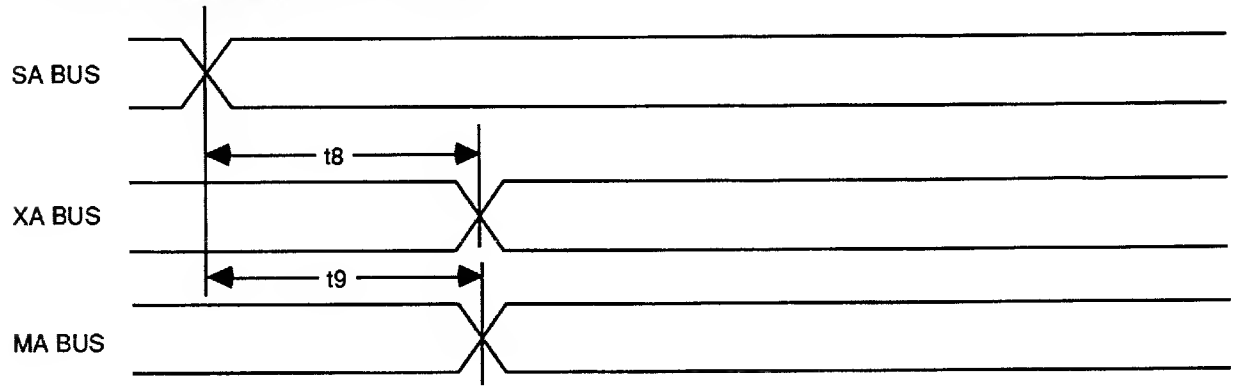
CPU MODE TIMING WAVEFORMS



SYSTEM BUS MODE TIMING

Symbol	Parameter	16 MHz Min	16 MHz Max	20 MHz Min	20 MHz Max	Unit	Condition
t8	SA Bus In to XA Bus Out		40		40	ns	CL = 100 pF
t9	SA Bus In to MA Bus Out		40		40	ns	CL = 300 pF

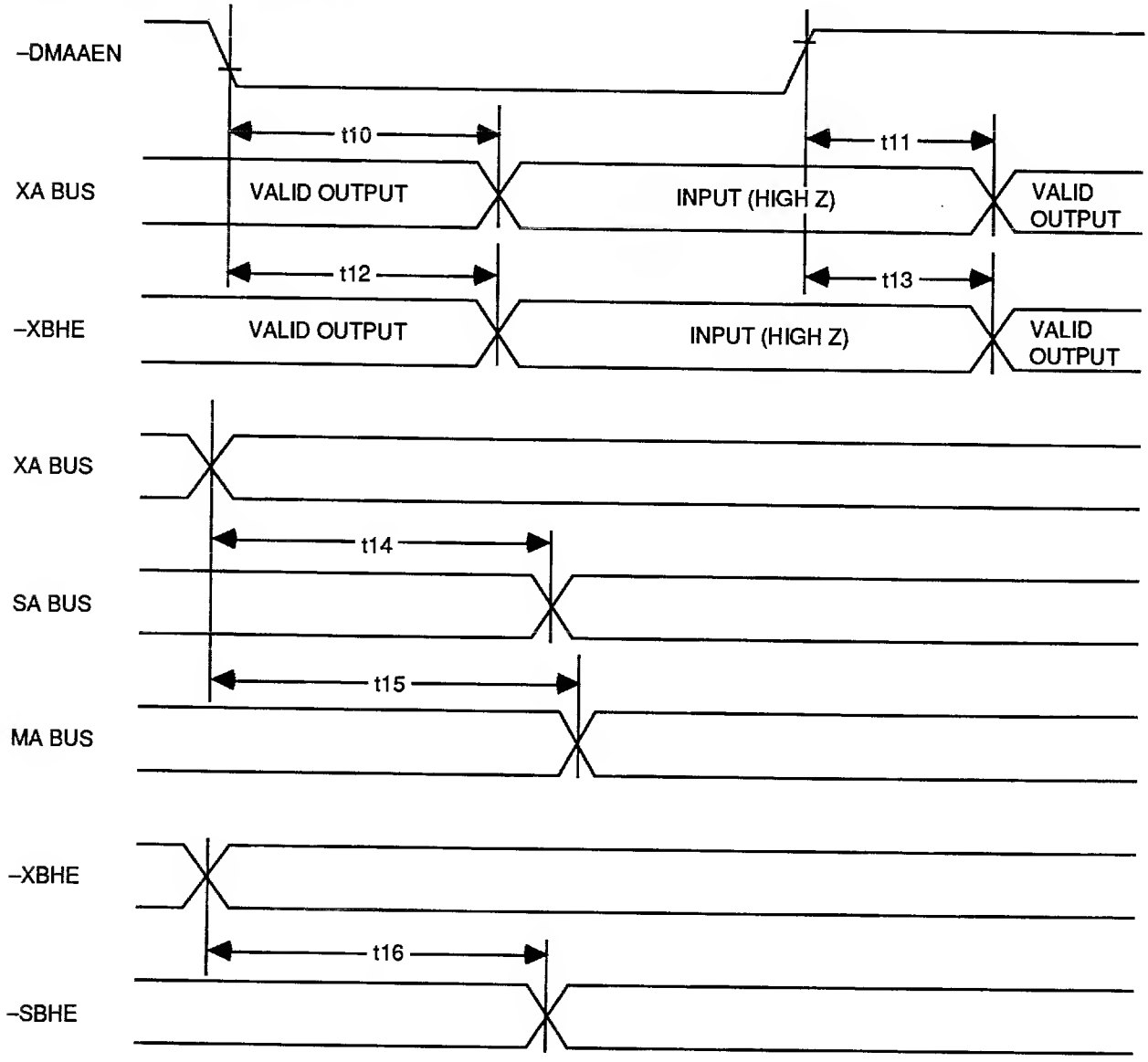
SYSTEM BUS MODE TIMING WAVEFORM



DMA MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t10	–DMAAEN to XA Bus High Z State		35		35	ns	
t11	–DMAAEN to XA Bus from High Z to Valid Add Out		35		35	ns	
t12	–DMAAEN to –XBHE High Z State		35		35	ns	
t13	–DMAAEN to –XBHE from High Z to Valid Output		35		35	ns	
t14	XA Bus to SA Bus Out		40		40	ns	CL = 200 pF
t15	XA Bus In to MA Bus Out		40		40	ns	CL = 300 pF
t16	–XBHE In to –SBHE Out		40		40	ns	CL = 200 pF

DMA MODE TIMING WAVEFORMS

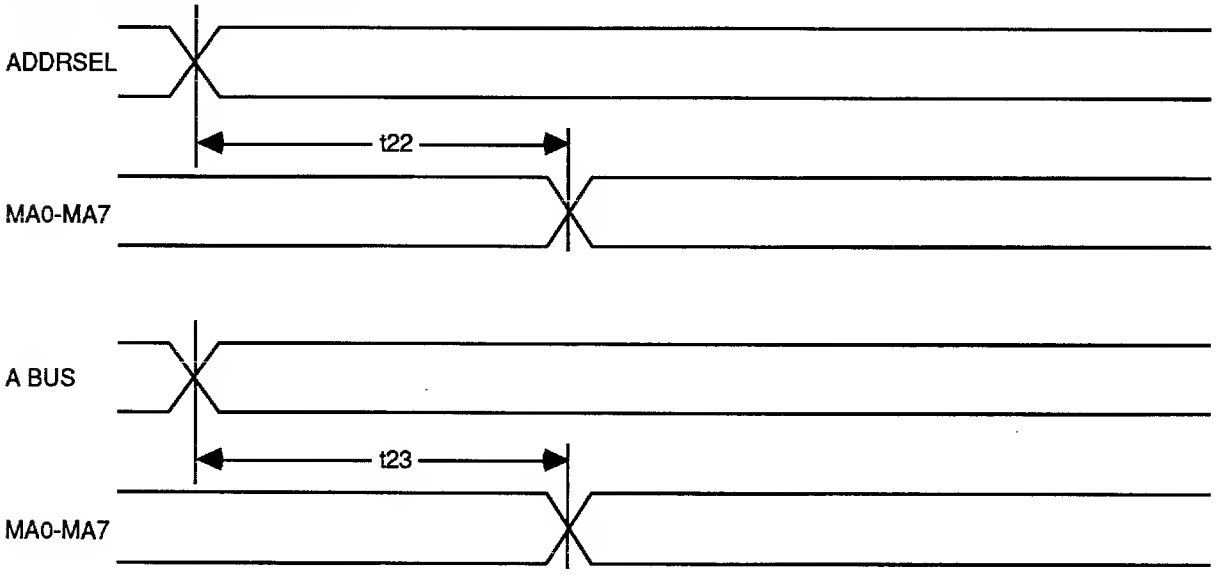


ADDRESS TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t22	ADDRSEL to MA Bus Out	4	19	4	19	ns	CL = 300 pF
t23	A Bus to MA Bus Out		25		25	ns	CL = 300 pF

Note: t22 delay may be derated by a factor of .04 ns/pF for heavier loads.

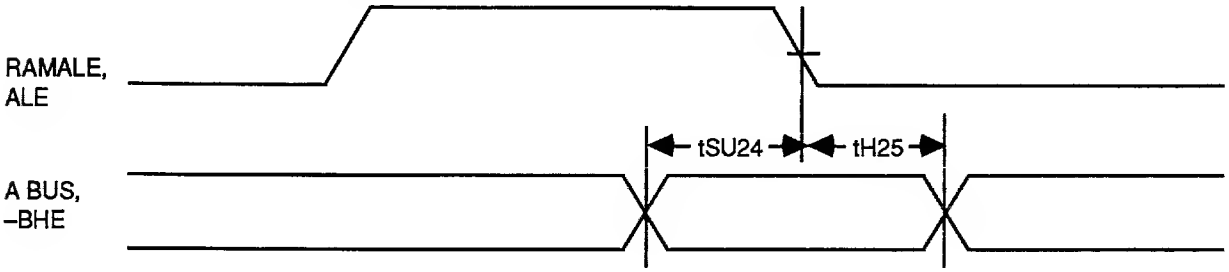
ADDRESS TIMING WAVEFORM



SETUP & HOLD TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU24	A Bus to RAMALE and –BHE to ALE Setup Timing	10		10		ns	
tH25	A Bus to RAMALE and –BHE to ALE Hold Timing	10		10		ns	

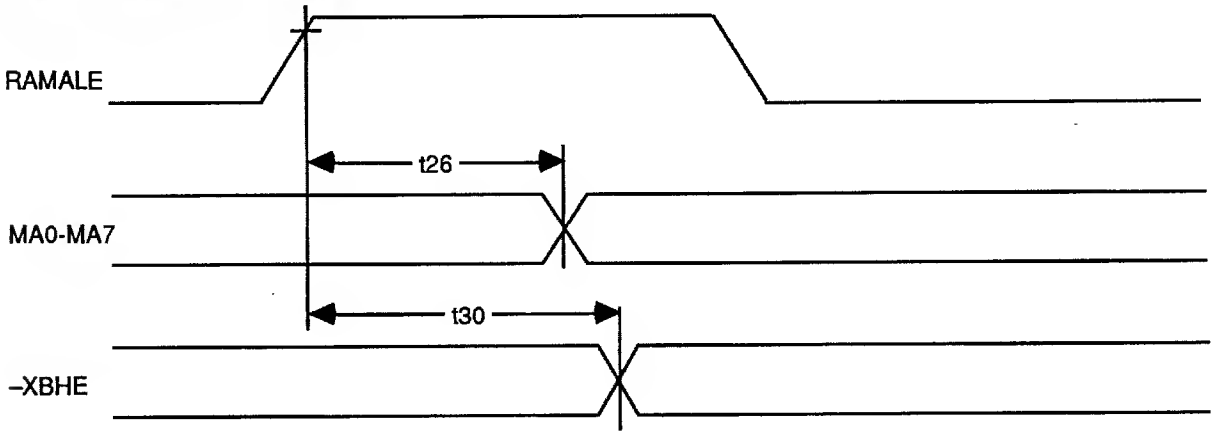
SETUP & HOLD TIMING WAVEFORM



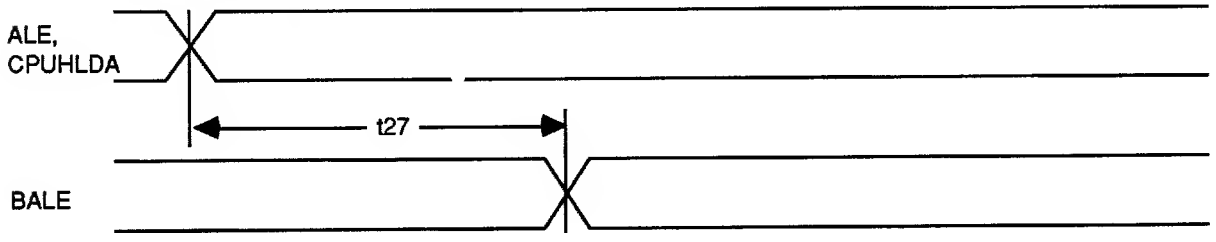
RAMALE, BALE & IRQ13 TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t26	RAMALE to MA Bus Out		20		18	ns	CL = 300 pF
t27	ALE, CPUHLDA to BALE Out		25		25	ns	CL = 200 pF
t28	–ERROR to IRQ13 Out		30		30	ns	CL = 50 pF
t29	–BUSY287 to IRQ13 Out		30		30	ns	CL = 50 pF
t30	RAMALE to –XBHE		25		25	ns	CL = 100 pF

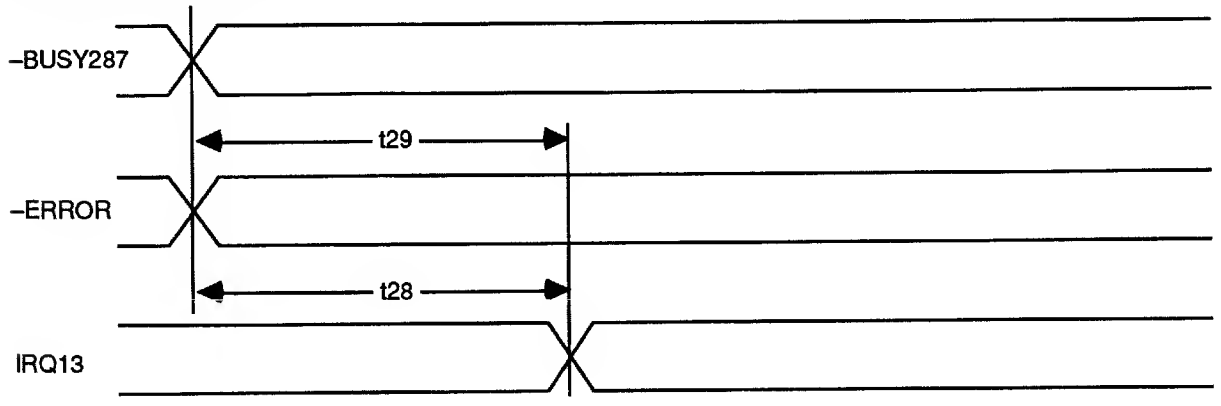
RAMALE TIMING WAVEFORM



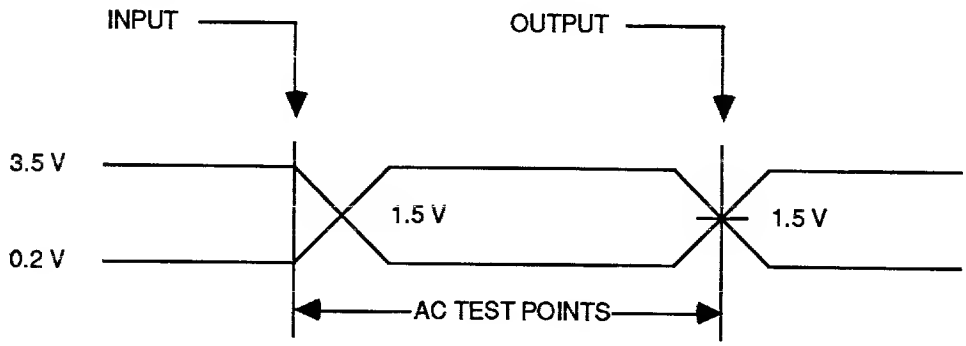
BALE TIMING WAVEFORM



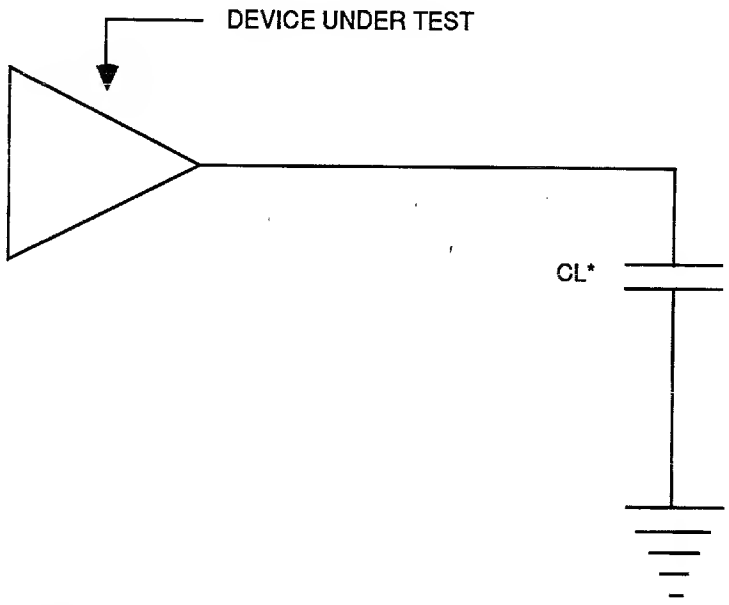
IRQ13 TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
32, 34-38, 40-43, 45-48, 50-53, 55	200
57-64	300
66-74, 76-83	100
84, 30	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ± 5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 24 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	ALE, RAMALE
VILC	Input Low Voltage	–0.5	0.6	V	ALE, RAMALE
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		20	mA	@ 1 MHz Test Rate

Notes: 1. Pins 57-64, 66-74, and 76-83.
2. Pins 32, 34-38, 40-43, 45-48, and 50-53, 55.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

VL82C204

PC/AT-COMPATIBLE DATA BUFFER

FEATURES

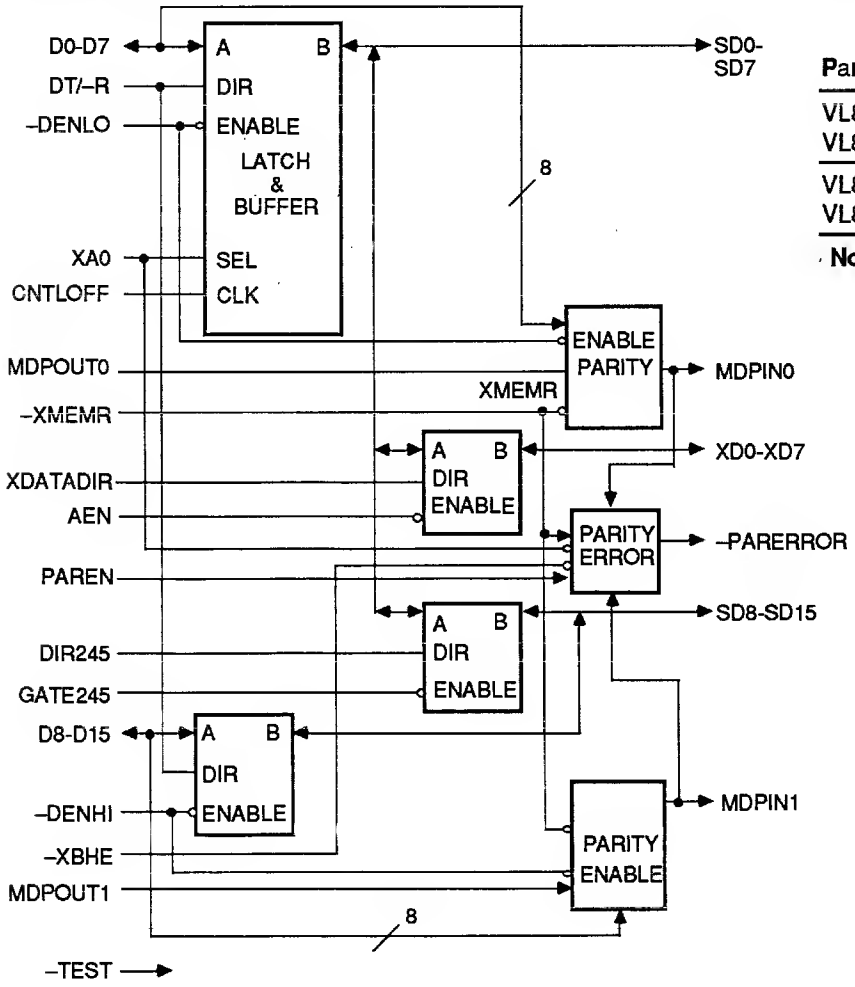
- Fully compatible with IBM PC/AT-type designs
- Completely performs data buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C204 PC/AT-Compatible Data Buffer provides a 16-bit CPU data bus I/O as well as 24 buffered drivers. The buffered drivers consist of 16 bidirectional system data bus drivers, each capable of sinking 24 mA (60 'LS loads) of current; eight bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current. The VL82C204 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 68-pin plastic leaded chip carrier (PLCC) package. The VL82C204 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



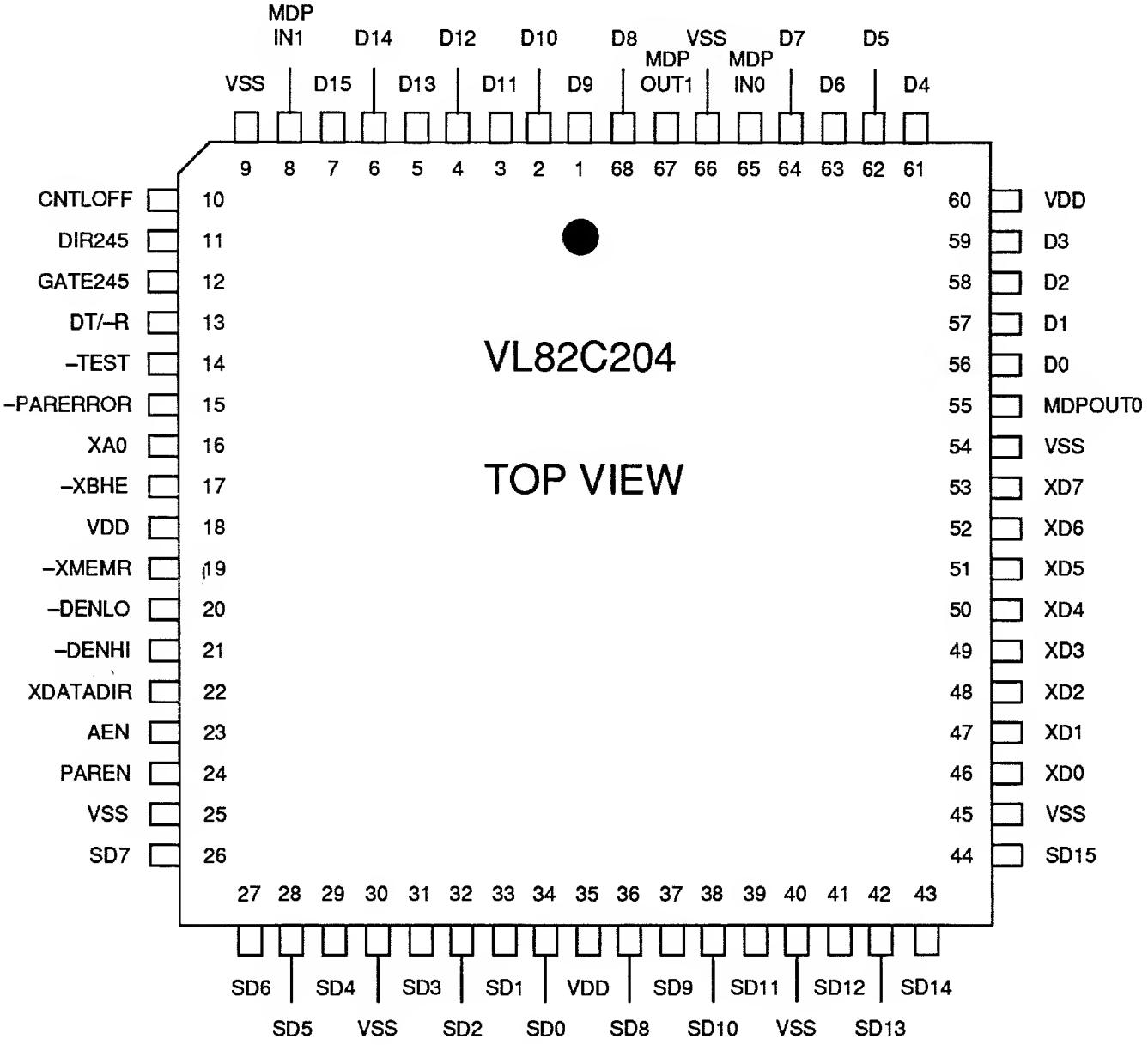
ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C204-16QC VL82C204-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C204-20QC VL82C204-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

4

PIN DIAGRAM


VL82C204
TOP VIEW
1 MDPOUT1
2 D9
3 D11
4 D13
5 D15
6 VSS
7 D14
8 MDPIN1
9 D12
10 D10
11 D8
12 VSS
13 D7
14 MDPIN0
15 MDPOUT0
16 D6
17 D5
18 D4
19 VDD
20 D3
21 D2
22 D1
23 D0
24 MDPOUT0
25 VSS
26 XD7
27 XD6
28 XD5
29 XD4
30 XD3
31 XD2
32 XD1
33 XD0
34 VSS
35 SD15
36 SD14
37 SD13
38 SD12
39 SD11
40 SD10
41 SD9
42 SD8
43 SD7
44 SD6
45 SD5
46 VSS
47 SD4
48 SD3
49 SD2
50 SD1
51 SD0
52 VDD
53 CNTLOFF
54 DIR245
55 GATE245
56 DT/-R
57 -TEST
58 -PARERROR
59 XA0
60 -XBHE
61 VDD
62 -XMEMR
63 -DENLO
64 -DENHI
65 XDATADIR
66 AEN
67 PAREN
68 VSS

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CNTLOFF	10	I	This input is used as a clock to latch the current data on the low byte of the system or peripheral data bus. Data is latched and output to D0-D7 on the rising edge of CNTLOFF and is independent of the status of DT/–R, XA0, or –DENLO.
DT/–R	13	I	Data Transmit (high)/Receive (low) - This input is a signal from the bus controller. It establishes the direction of data flow to or from the system data bus.
–TEST	14	I	Test - This is an active low input which is used to three-state all outputs of the VL82C204 device. This is for system level test where it is necessary to overdrive the outputs of the VL82C204. When –TEST is low, all outputs and bidirectional pins of the VL82C204 will be three-stated. This pin should be pulled up via a 10K Ω pull-up resistor in a standard system configuration.
–DENLO	20	I	Data Enable Low - An active low input that enables a low byte data transfer on the CPU data bus low byte transceiver. When –DENLO is inactive, low byte parity is disabled.
XA0	16	I	Peripheral Address Bus Bit 0 - This is the LSB of the peripheral address bus. The signal is used throughout the system to indicate low or high byte data transfers. It is used to select latched or immediate data out of the CPU low byte bus transceiver. It also enables low byte parity checking.
XDATADIR	22	I	Transceiver Data Direction - This input is used to select the direction of the peripheral data bus transceiver. When XDATADIR is low, it indicates an I/O read from the XD bus or an interrupt acknowledge cycle. When XDATADIR is high, it indicates data on the SD bus should be placed on XD bus.
AEN	23	I	Address Enable - An active high input that is used to disable the peripheral data bus transceiver while the DMA controller is using the peripheral data bus for address information.
DIR245	11	I	Direction 245 - An input control signal used to set the direction of the high/low system data bus transceiver. This is used for high to low, or low to high data byte moves.
GATE245	12	I	Gate 245 - An active low input that enables the high/low system data transceiver.
–DENHI	21	I	Data Enable High - An active low input that enables a high byte data transfer on the CPU data bus high byte transceiver. When –DENHI is inactive, high byte parity is disabled.
–XBHE	17	I	Transfer Bus High Enable - An active low that indicates a transfer of data on the upper byte of the memory data bus. It also enables high byte parity checking.
–XMEMR	19	I	Memory Read Enable - An active low input signal that indicates when a memory read cycle is occurring. It is used to disable the MDPOUTx signals during a memory write and to latch in the detected parity error signal during a memory read.
MDPOUT0	55	I	Memory Data Parity Out 0 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the low byte of data read from memory.
MDPOUT1	67	I	Memory Data Parity Out 1 - An active high input that is the output of the stored memory parity data. It is checked for parity errors with the high byte of data read from memory.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MDPIN0	65	O	Memory Data Parity In 0 - An active high output that is the parity input to the system board memory. It is generated from the current low byte data on the memory data bus.
MDPIN1	8	O	Memory Data Parity In 1 - An active high output that is the parity input to the system board memory. It is generated from the current high byte data on the memory data bus.
PAREN	24	I	Parity Enable - This active high input is used to enable the parity data latch. It is used to prevent false parity errors when ROM memory access occurs.
–PARERROR	15	O	Parity Error - An active low output that is used to indicate that a memory parity error has occurred. This signal is latched by –XMEMR and is valid until the next memory access.
XD0-XD7	46-53	I/O	Peripheral Data Bus Bits 0-7 - I/O's used to control the coprocessor, keyboard, ROM memory, and the DMA controllers.
D0-D15	56-59, 61-64 68, 1-7	I/O	CPU Data Bus Bits 0-15 - This is a bidirectional bus controlled by the DT/–R input.
SD0-SD15	34-31, 29-26, 36-39, 41-44	I/O	System Data Bus Bits 0-15 - These are I/O signals.
VDD	18, 35, 60		System Power: 5 V
VSS	9, 25, 30, 40, 45, 54, 66		System Ground

FUNCTIONAL DESCRIPTION

The VL82C204 is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Data Buffer replaces several bus transceivers and a CPU lower byte data latch located within a PC/AT-type system.

The primary function of the Data Buffer is to multiplex the 80286 microprocessor data lines D0-D15 to the system data bus SD0-SD15 and the peripheral data bus XD0-XD7. This is accomplished through four sets of 8-bit wide data multiplexors. The lower data byte of the CPU data bus transceiver has a byte wide register which is clocked by the rising edge of CNTLOFF. The data can be latched to the lower byte of the CPU data bus only. XA0 is used to control data flow to the CPU data bus. When XA0 = 0, real time data is passed to the CPU data bus. When XA0 = 1, latched data is passed to the CPU data bus. The four groups of transceivers can be seen in the block diagram of the device. The data parity encoder/decoder logic is also located within this device. All data present upon the CPU data bus passes through the parity logic. The outputs of the parity encoder/decoders, MDPIN0 and MDPIN1, are enabled via PAREN to prevent decoding a ROM access and are gated with –XMEMR. The –PARERROR signal is fed back to the Memory Controller where it is gated with other logic to produce the NMI signal for the 80286.

The logic controlling the bus transceivers has been optimized for speed and as such there are no provisions to prevent internal bus collisions. In a standard PC/AT-type application using the full 16 or 20 MHz, the VL82CPCAT-16/-20, chip sets this is not a problem as the control signals which enable the transceivers are decoded in such a fashion as to prevent this from happening. In the case where only the VL82C204 is used, care must be taken as to ensure that the control signals will not cause an internal bus collision. From the block diagram it can be seen that every bus transceiver has an A and B I/O port. The DIR input to the transceiver controls the direction of data flow through the transceiver. A high (1) input into the DIR pin causes data to flow from A to B. A low (0) causes data to flow from B to A. All transceiver enables are low true causing the output of the particular transceiver to be active.

The VL82C204 should be used with either the VL82CPCAT-16 or VL82CPCAT-20 chip sets as it implements a changed architecture from the original system. In order to speed up the memory access, the MD bus (memory data) has been moved to the CPU Data Bus. The VL82C204 has been designed to accommodate this change.

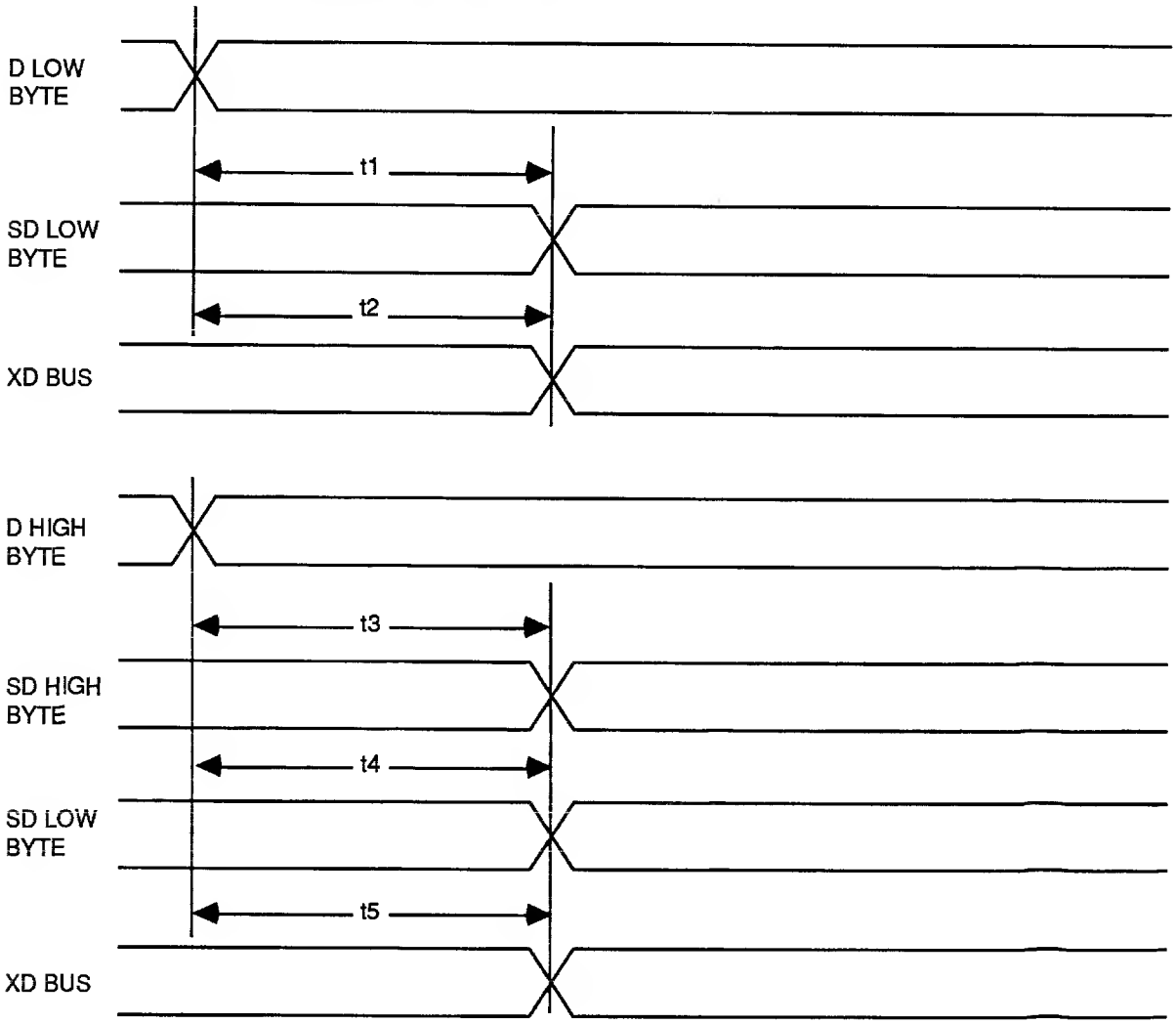
The –TEST pin has been added to enhance system level testing of the chip sets. When this pin is active (0), all outputs and bidirectional pins are placed in three-state. This allows a board level test system to overdrive outputs of the VL82C204 without damage to the device. In addition to three-stating the outputs, all bus control inputs are ignored to prevent internal bus collisions and the internal bus follows the state of the system data bus (SD0-SD15).

AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

CPU DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t1	D Low Byte In to SD Low Byte Out		35		35	ns	CL = 200 pF
t2	D Low Byte In to XD Bus Out		30		30	ns	CL = 100 pF
t3	D High Byte In to SD High Byte Out		35		35	ns	CL = 200 pF
t4	D High Byte In to SD Low Byte Out		35		35	ns	CL = 200 pF
t5	D High Byte In to XD Bus Out		30		30	ns	CL = 100 pF

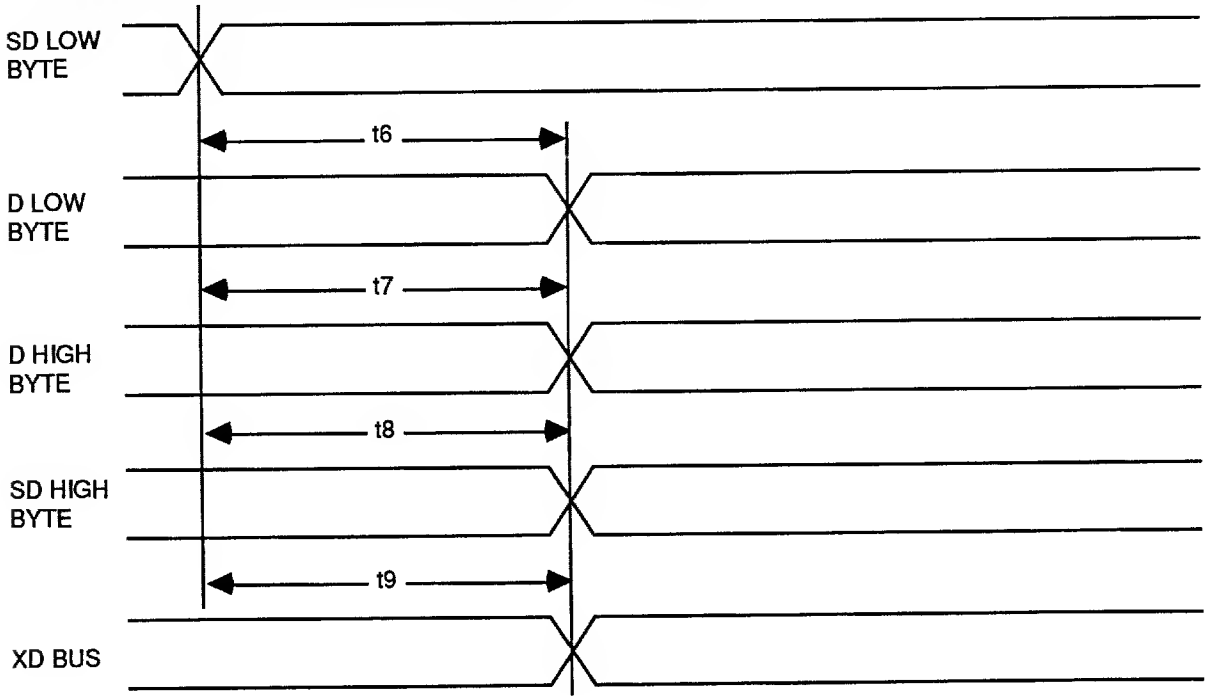
CPU DATA BUS I/O MODE TIMING WAVEFORMS



SYSTEM LOW BYTE DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t6	SD Low Byte In to D Low Byte Out		30		30	ns	CL = 120 pF
t7	SD Low Byte In to D High Byte Out		35		35	ns	CL = 120 pF
t8	SD Low Byte In to SD High Byte Out		35		35	ns	CL = 200 pF
t9	SD Low Byte In to XD Bus Out		30		30	ns	CL = 100 pF

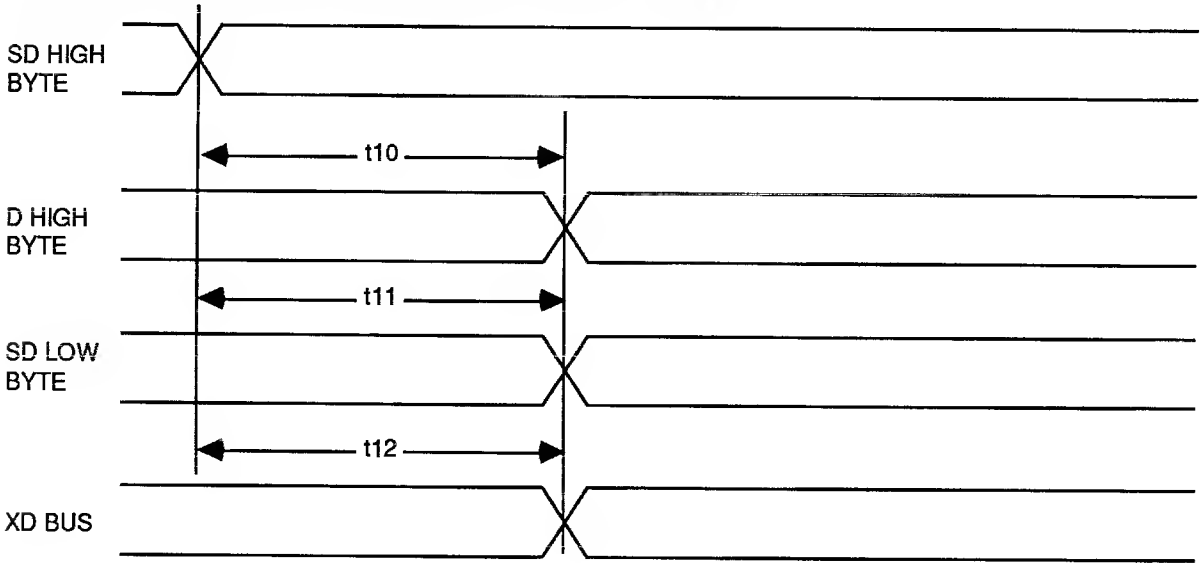
SYSTEM LOW BYTE DATA BUS I/O MODE TIMING WAVEFORMS



SYSTEM HIGH BYTE DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t10	SD High Byte In to D High Byte Out		30		30	ns	CL = 120 pF
t11	SD High Byte In to SD Low Byte Out		35		35	ns	CL = 200 pF
t12	SD High Byte In to XD Bus Out		30		30	ns	CL = 100 pF

SYSTEM HIGH BYTE DATA BUS I/O MODE TIMING WAVEFORMS

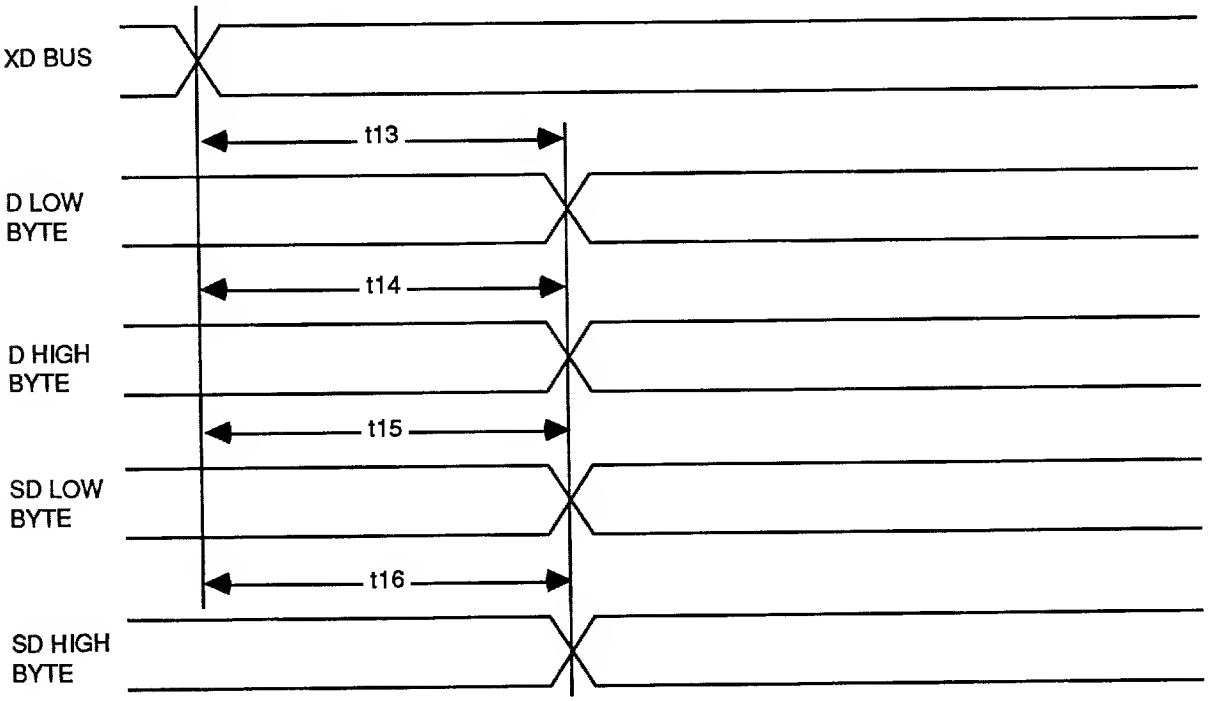


4

PERIPHERAL DATA BUS I/O MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t13	XD Bus In to D Low Byte Out		30		30	ns	CL = 120 pF
t14	XD Bus In to D High Byte Out		30		30	ns	CL = 120 pF
t15	XD Bus In to SD Low Byte Out		35		35	ns	CL = 200 pF
t16	XD Bus In to SD High Byte Out		35		35	ns	CL = 200 pF

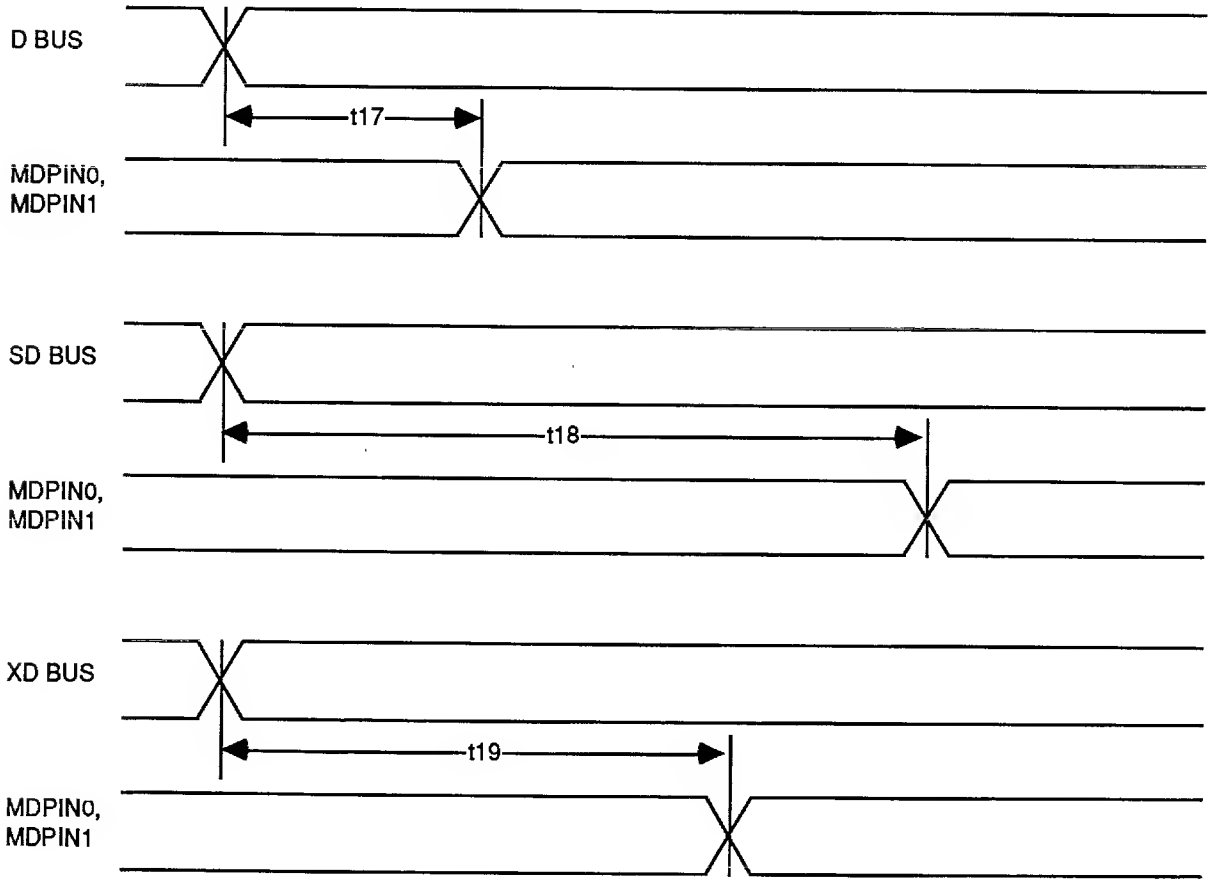
PERIPHERAL DATA BUS I/O MODE TIMING WAVEFORM



MEMORY WRITE MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t17	D Bus In to MDPIN0, MDPIN1 Out		16		16	ns	CL = 50 pF
t18	SD Bus In to MDPIN0, MDPIN1 Out		46		46	ns	CL = 50 pF
t19	XD Bus In to MDPIN0, MDPIN1 Out		46		46	ns	CL = 50 pF

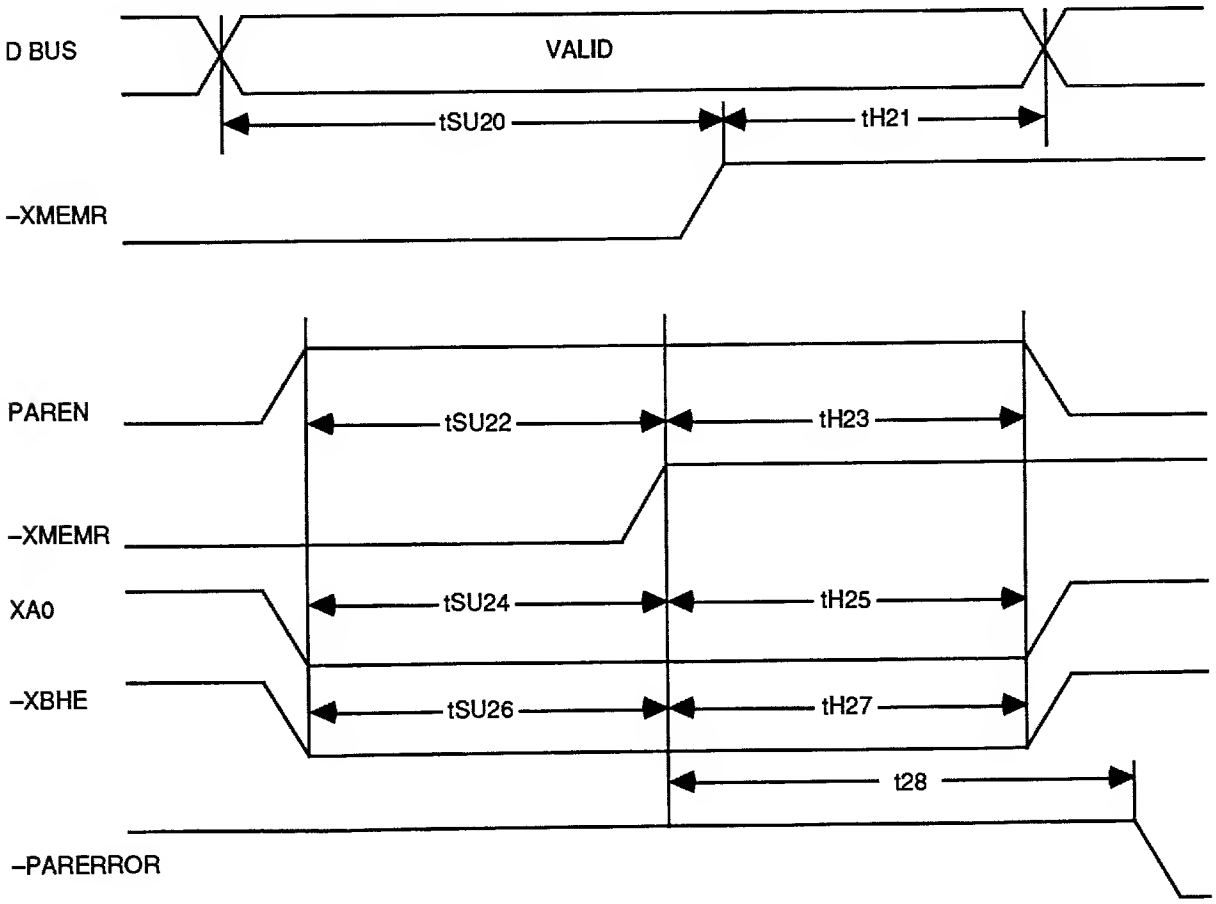
MEMORY WRITE MODE TIMING WAVEFORM



MEMORY READ MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU20	D Bus Setup to –XMEMR High	19		19		ns	
tH21	D Bus Hold to –XMEMR High	–4		–4		ns	
tSU22	PAREN Setup to –XMEMR High	10		10		ns	
tH23	PAREN Hold to –XMEMR High	3		3		ns	
tSU24	XA0 Setup to –XMEMR High	10		10		ns	
tH25	XA0 Hold to –XMEMR High	3		3		ns	
tSU26	–XBHE Setup to –XMEMR High	10		10		ns	
tH27	–XBHE Hold to –XMEMR High	3		3		ns	
t28	–XMEMR High to –PARERROR Out		25		25	ns	CL = 50 pF

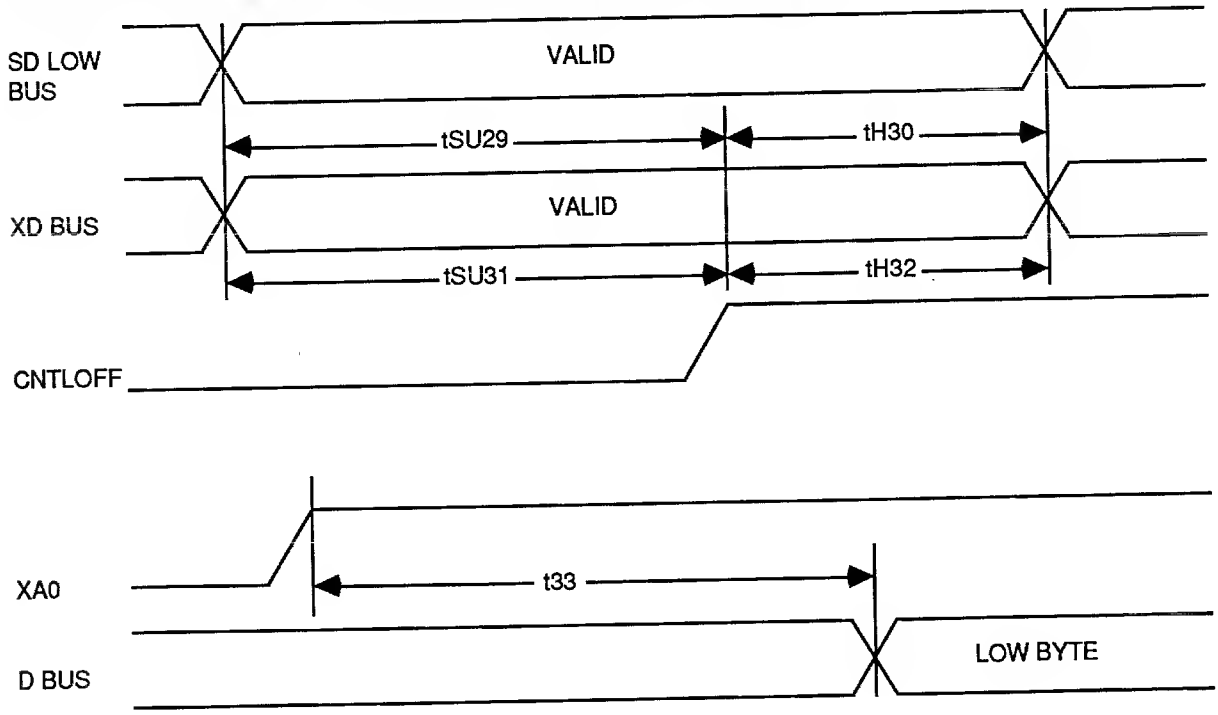
MEMORY READ MODE TIMING WAVEFORM



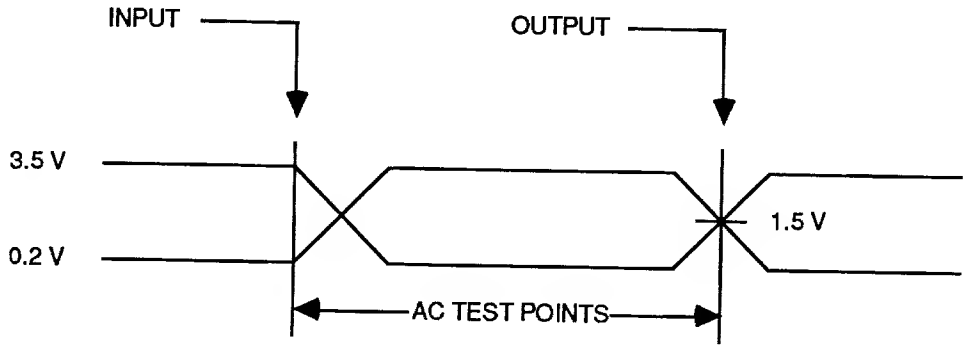
CPU LOW BYTE DATA BUS LATCH AND SELECT TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU29	SD Low Byte Setup to CNTLOFF High	20		20		ns	
tH30	SD Low Byte Hold to CNTLOFF High	10		10		ns	
tSU31	XD Bus Setup to CNTLOFF High	20		20		ns	
tH32	XD Bus Hold to CNTLOFF High	10		10		ns	
t33	XA0 to D Low Bus Out		30		30	ns	CL = 120 pF

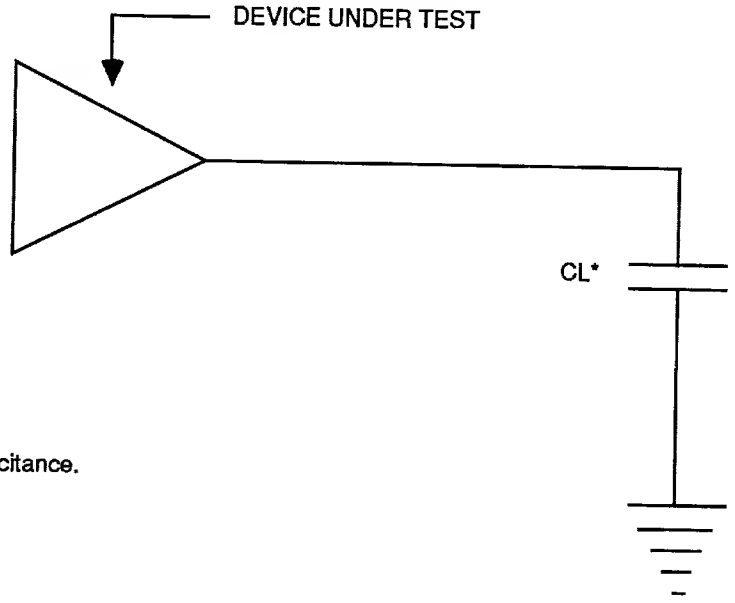
CPU LOW BYTE DATA BUS LATCH AND SELECT TIMING WAVEFORMS



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
26-29, 31-34, 36-39, 41-44	200
1-7, 56-59, 61-64, 68	120
46-53	100
8, 15, 65	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 24 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	CNTLOFF
VILC	Input Low Voltage	–0.5	0.6	V	CNTLOFF
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		20	mA	@ 1 MHz Test Rate

Notes: 1. Pins 1-7, 46-53, 56-59, 61-64, 68.
2. Pins 26-29, 31-34, 36-39, 41-44.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

APPLICATION NOTE

In order to ensure correct function of bus transfers when using the VL82C204 as a stand-alone part (not part of the chip set), the following conditions must be met:

For SD high byte in to SD low byte out, ensure that either –DENHI = 1 or DT/–R = 0.

For SD low byte in to SD high byte out, ensure that either –DENLO = 1 or DT/–R = 0 and AEN = 1 or XDATADIR = 1.

When using the VL82C204 along with the remaining chips in the chip set, these conditions are virtually excluded.

NOTES:

VL82C205

PAGE-MODE ACCESS CONTROLLER

FEATURES

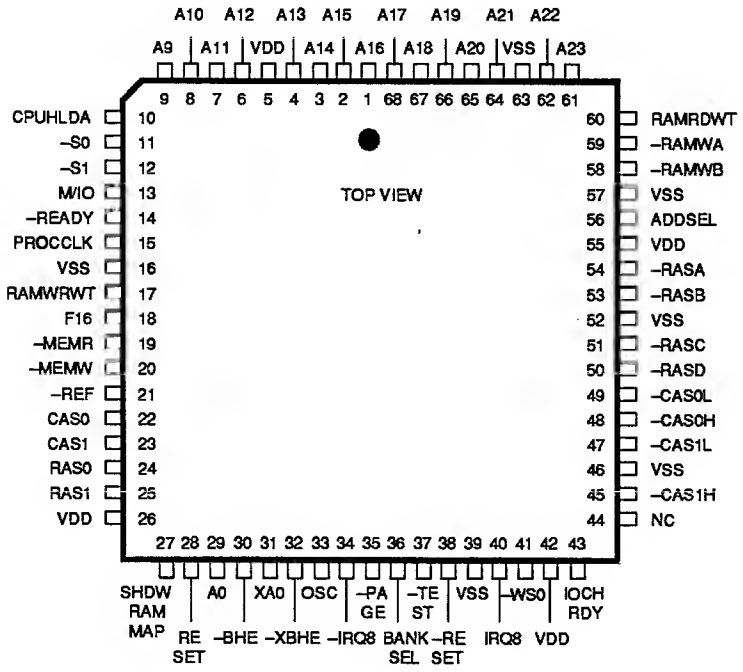
- Supports 16 MHz 80286 operation with 100 ns DRAMs
- Supports page-mode DRAM access for PC/AT-compatible systems
- Speed upgrades to 20 MHz
- Companion to VL82CPCAT-16 and VL82CPCAT-20, 16/20 MHz PC/AT-compatible chip sets
- 13 chip PC/AT implementation (non-memory chips)
- 0.6 wait state operation during DRAM read accesses
- Low power CMOS technology
- 68-pin PLCC package

DESCRIPTION

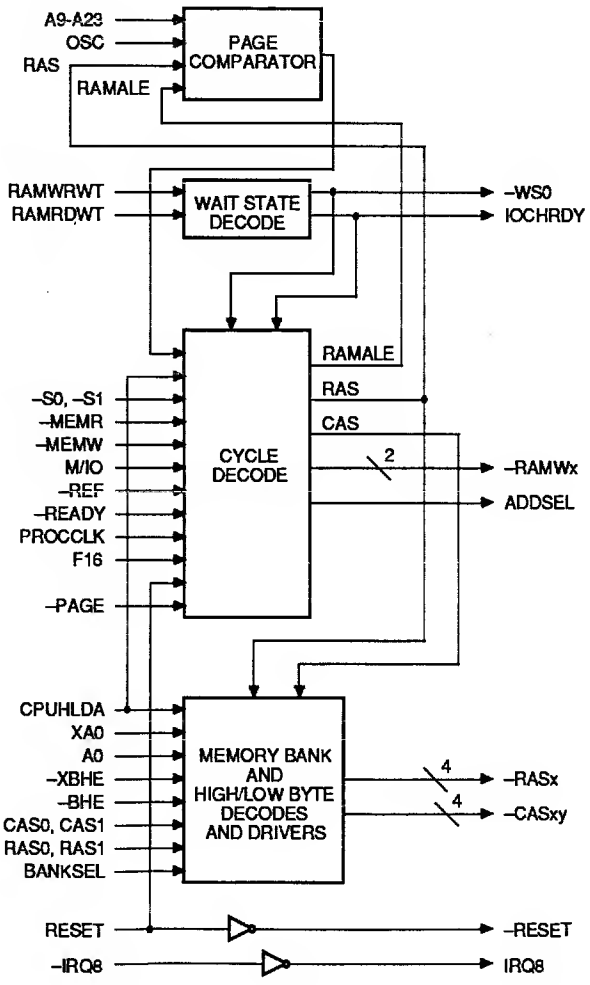
The VL82C205 is a page-mode memory controller for the VLSI, VL82CPCAT-16 and VL82CPCAT-20, 16/20 MHz PC/AT-compatible chip set. This chip in addition to the other five chips from the VLSI chip sets, allows page-mode memory cycles to be run, allowing a 16 MHz processor to use standard 100 ns DRAMs and still have only 0.6 wait states during DRAM read accesses.

When using page-mode, accesses that are within 512 words of the last access are performed with zero wait states, accesses that are outside that range are performed in two wait states.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Freq.	Package
VL82C205-16QC	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C205-20QC	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
A9-A23	9-6, 4-1, 68-64, 62, 61	I	Upper Address Bits from the CPU - These inputs are latched any time the –RASx signals go active. On any following memory reads the address bits are compared to the latched value to determine if a page hit has occurred.
CPUHLDA	10	I	CPU Hold Acknowledge - This input is used to determine which signals are used to initiate and terminate memory cycles. When CPUHLDA is low, the status signals –S0, –S1 and M/–IO along with –READY are used to control memory cycles. When CPUHLDA is high, the inputs –MEMR and –MEMW are used to generate the DRAM control signals.
–S0	11	I	Status 0 - This input is used along with –S1 and M/–IO to determine which type of bus cycle is being requested by the CPU.
–S1	12	I	Status 1 - This input is used along with –S0 and M/–IO to determine which type of bus cycle is being requested by the CPU.
M/–IO	13	I	Memory or I/O select - This input is used along with –S0 and –S1 to determine which type of bus cycle is being requested by the CPU.
–READY	14	I	An input used to determine when to terminate the current memory access to the DRAMs.
PROCCLK	15	I	This is the main clock input to the VL82C205 and should be connected to the same signal that drives the 80286 CLK pin.
RAMWRWT RAMRDWT	17 60	I I	The wait select inputs control the number of wait states to be used for memory accesses when the –PAGE input is high. If RAMRDWT is low, zero wait state read cycles are generated. If RAMWRWT is low, zero wait state write cycles are generated. If either signal is high, one wait state memory cycles are generated for the read or write.
F16	18	I	The F16 input comes from the memory controller chip and is used to indicate that the next address is in the on-board memory address space.
–MEMR	19	I	Memory Read - An input which is used to determine when memory read accesses to the DRAMs should occur if CPUHLDA is high.
–MEMW	20	I	Memory Write - An input which is used to determine when memory write accesses to the DRAMs should occur if CPUHLDA is high.
–REF	21	I	The –REFRESH input is used by the VL82C205 to force the ADDSEL output low.
CAS0	22	I	CAS Enable Input for Bank 0 - This input is used along with CAS1, RAS0, RAS1, and BANKSEL to determine which bank of DRAM should be accessed.
CAS1	23	I	CAS Enable Input for Bank 1 - This input is used along with CAS0, RAS0, RAS1, and BANKSEL to determine which bank of DRAM should be accessed.
RAS0	24	I	RAS Enable Input for Bank 0 - This input is used along with RAS1, CAS0, CAS1, and BANKSEL to determine which bank of DRAM should be accessed.
RAS1	25	I	RAS Enable Input for Bank 1 - This input is used along with RAS0, CAS0, CAS1, and BANKSEL to determine which bank of DRAM should be accessed.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SHDWRAMMAP	27	I	Shadow RAM Map - An active high input that indicates the system is using the shadow mode (see the VL82C202 description for complete discussion of shadow mode). This signal is decoded with the addresses to generate RAS and CAS outputs while doing memory writes to address blocks 0A XXXX to 0D XXXX during the copying of ROM into shadow RAM. This is needed because the F16 signal is inhibited during the writes to these blocks before the proper read enable register bits have been set on the VL82C202.
RESET	28	I	This input is the main reset signal for the page-mode controller chip.
–RESET	38	O	This output is the logical inversion of the RESET input.
A0	29	I	A0 is an input signal from the CPU. It is used when CPUHLDA is low to enable the appropriate low byte –CAS output during a memory cycle.
–BHE	30	I	Byte High Enable - An input signal from the CPU. It is used when CPUHLDA is low to enable the appropriate high byte –CAS output during a memory cycle.
XA0	31	I	XA0 is sampled when CPUHLDA is high to enable the appropriate low byte –CAS output during a memory cycle.
–XBHE	32	I	–XBHE is sampled when CPUHLDA is high to enable the appropriate high byte –CAS output during a memory cycle.
OSC	33	I	The OSC clock input is used as a fixed frequency to determine when a RAS precharge is required.
–IRQ8	34	I	This input is the active low interrupt request from the real time clock. It is inverted and sent out as IRQ8.
IRQ8	40	O	This output is the logical inversion of the –IRQ8 input.
–PAGE	35	I	The –PAGE input controls the type of memory accesses to be performed for CPU requests. When –PAGE is low, the VL82C205 will generate zero wait state page-mode accesses on page hits. When –PAGE is high, the VL82C205 will sample RAMWRWT or RAMRDWT to generate normal zero or one wait state memory accesses.
BANKSEL	36	I	Bank Select - Used to determine whether the combination of signals on the inputs RAS0, RAS1, CAS0, and CAS1 are addressing a DRAM bank controlled by this VL82C205.
–TEST	37	I	An active low input which should be pulled high through an external pull-up resistor. When pulled low, it will force the page-mode controller to put all output pins into a high impedance state to isolate it from other parts in the system.
–WS0	41	O	Wait State 0 - An active low output which is pulled low any time the page-mode controller wants the current bus cycle to be a zero wait state cycle. It requires an external 300 ohm pull-up resistor.
IOCHRDY	43	O	I/O Channel Ready - An output which is pulled low only during page hits. It requires an external 300 ohm pull-up resistor.
NC	44		No Connect.
–CAS1H	45	O	Column Address Strobe 1 High - This active low column address strobe should be connected directly to the DRAMs for the high byte of bank 1. It is enabled for memory accesses to bank 1 when –BHE is low in CPU mode or when –XBHE is low in non-CPU mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–CAS1L	47	O	Column Address Strobe 1 Low - This active low column address strobe should be connected directly to the DRAMs for the low byte of bank 1. It is enabled for memory accesses to bank 1 when A0 is low in CPU mode or when XA0 is low in non-CPU mode.
–CAS0H	48	O	Column Address Strobe 0 High - This active low column address strobe should be connected directly to the DRAMs for the high byte of bank 0. It is enabled for memory accesses to bank 0 when –BHE is low in CPU mode or when –XBHE is low in non-CPU mode.
–CAS0L	49	O	Column Address Strobe 0 Low - This active low column address strobe should be connected directly to the DRAMs for the low byte of bank 0. It is enabled for memory accesses to bank 0 when A0 is low in CPU mode or when XA0 is low in non-CPU mode.
–RASx	54, 53, 51, 50	O	Row Address Strobes A, B, C, and D - These are the active low row address strobes to be connected directly to the DRAMs. RAS timing will vary depending on the operating mode. Refer to the functional description and AC timing diagrams for timing. All the –RASx outputs are functionally identical. Each output provides sufficient drive for a single 8 bit bank.
ADDSEL	56	O	Address Select - An output used to switch from row to column addresses. It will always follow the –RASx outputs by half a PROCCLK cycle if in page-mode. In non page-mode, (–PAGE = 1, or CPUHLDA = 1) it follows the –RASx outputs by half a PROCCLK cycle unless zero wait state is selected. During zero wait state cycles ADDSEL follows –RASx on the same PROCCLK edge but is delayed 4 to 12 ns. ADDSEL is forced low during refresh cycles.
–RAMWB	58	O	RAM Write B - Used to get an early write enable signal to the DRAMs to support page-mode timing and zero wait state write cycles. It will go low during the second phase of any memory write cycle. –RAMWB will return high at the end of the bus cycle when –READY is sampled low. –RAMWB is functionally identical to –RAMWA. Each output provides sufficient drive for a single 16 bit bank.
–RAMWA	59	O	RAM Write A - Used to get an early write enable signal to the DRAMs to support page-mode timing and zero wait state write cycles. It will go low during the second phase of any memory write cycle. –RAMWA will return high at the end of the bus cycle when –READY is sampled low. –RAMWA is functionally identical to –RAMWB. Each output provides sufficient drive for a single 16 bit bank.
VSS	16, 39, 46, 52, 57, 63		System Ground
VDD	5, 26, 42, 55		System Power: 5 V

FUNCTIONAL DESCRIPTION

The VL82C205 consists of several major blocks, including the page hit detection logic, RAS and CAS generation, RAS time-out detection, non-page-mode timing support, time base generation and glue-collection. For a more detailed understanding of the VL82C205, refer to the block diagram.

PAGE-MODE CONTROLLER

In this discussion, the following terms are used:

- Page refers to a block of 512 bytes, for which only the lower nine address bits may change.
- Bank refers to the upper or lower half of a 16-bit word, selected by –XBHE if CPUHLDA = 1 and by –BHE if CPUHLDA = 0.
- High/Low Byte refers to the decoding of the address LSB, selected by XA0 if CPUHLDA = 1 and by A0 if CPUHLDA = 0.

The VL82C205 controller may be used in either page-mode or non page-mode, as chosen by input –PAGE. In page-mode, any read access within the same page of the previous memory access is performed with zero wait states. Internal latches track the successive address references, permitting the shorter cycles to be used automatically.

For references on page, the DRAM row addresses do not change. Therefore, the RAS lines remain asserted continuously between DRAM cycles. (The DRAM column lines are effectively mapped to the lower nine bits of the address space.)

An access outside of the 512-byte page or a write operation forces two wait states. Under that condition, the RAS lines are de-asserted for the required precharge time.

With the controller's page-mode operation enabled, an average of 0.6 wait states is used. This assumes 16 MHz operation, with standard 100 ns DRAMs.

RAS/CAS GENERATION

The controller attempts to generate RAS at the earliest time possible. A number of conditions are monitored by the chip, which could preclude early RAS. The RAS precharge timing logic then generates RAS and CAS based on them.

The four RAS outputs are identical. The same signal is brought out four times to supply suffcient drive for large memory arrays, without the need for off-chip buffering.

The four CAS outputs are decoded separately as follows:

–CAS1H = en_cas1 • en_cashigh

–CAS1L = en_cas1 • en_caslow

–CAS0H = en_cas0 • en_cashigh

–CAS0L = en_cas0 • en_caslow

Where:

en_cas1: = (BANKSEL • CAS1 • RAS1) + (/BANKSEL • CAS1 • RAS0)

en_cas0: = (BANKSEL • CAS0 • RAS0) + (/BANKSEL • CAS0 • RAS1)

en_cashigh: = (/CPUHLDA • /–BHE) + (CPUHLDA • /–XBHE)

en_caslow: = (/CPUHLDA • /A0) + (CPUHLDA • /XA0)

This decoding allows up to eight banks of memory when used with the RAS and CAS signals from the VL82C202 Memory Controller.

RAS-ACTIVE TIMEOUT WARNING

An internal counter monitors RAS to detect maximum RAS active time. After approximately 10 µs, a RAS precharge is performed.

Input OSC is used to monitor RAS. A maximum of 72 consecutive read operations at 16 MHz to the same page can take place before a false page miss is inserted to do the RAS precharge.

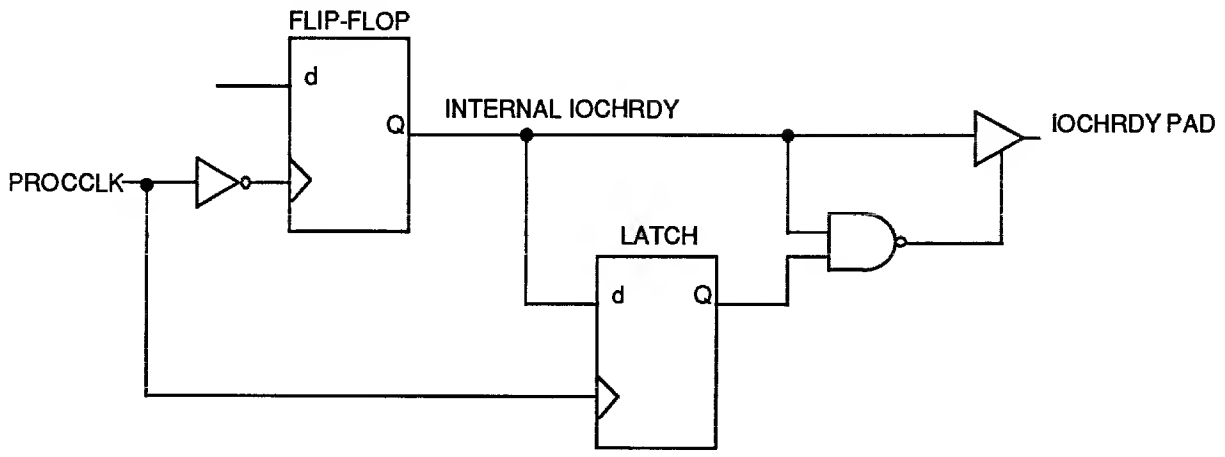
WAIT STATE GENERATION

IOCHRDY and –WS0 are the outputs that indicate how many wait states are in the current cycle. –WS0 is pulled low for all page hits. Other zero wait state cycles are handled by the VL82C201. This is an open drain output and a 300 ohm pull-up resistor is required for 16 MHz operation.

IOCHRDY is pulled low for all two wait state cycles. This is a three-state output. When IOCHRDY goes high (inactive), the VL82C205 drives the signal for half a PROCCLK cycle (15 ns), then goes into three-state (see the logic below). A 300 ohm pull-up resistor is required to hold the signal high and to pull-up the other system open drain outputs connected to IOCHRDY.

4

FIGURE 1. IOCHRDY GENERATION



NON-CPU MODE

When CPUHLDA = 1, the processor surrenders the bus for Master, DMA, or Refresh modes. In these three modes the –MEMW and –MEMR inputs signify whether memory reads or writes occur. Also, inputs XA0 and –XBHE replace A0 and –BHE in the decoding of the four –CASxy outputs.

–MEMW and –MEMR can be asynchronous to PROCCLK. They are sampled by the falling edge of PROCCLK to synchronize them with the internal state machine.

IOCHRDY is never driven active (low) in this mode since the read or write cycles can be extended by keeping –MEMR or –MEMW low (see the waveforms for non-CPU mode timing). Note that if inputs RAMRDWT or RAMWRWT are low, then ADDSEL and the –CASxy outputs go active off the falling edge of PROCCLK.

USING TWO VL82C205s IN A SYSTEM

The VL82C202 Memory Controller allows up to four system RAM banks. By using two VL82C205s a system can have up to 4M bytes of fast RAM running at zero wait states in non page-mode. The jumpered input should be set as follows:

- When the VL82C205 is controlling the page-mode banks, –PAGE = 0, RAMWRWT = 1, RAMRDWT = 1, BANKSEL = 1.
- When the VL82C205 is controlling the normal mode banks, –PAGE = 1, BANKSEL = 0, RAMRDWT = same as pin 18 on the VL82C201 System Controller, RAMWRWT = same as pin 80 on the VL82C201.

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU1	–S0, –S1 to PROCCLK Setup Time	13		9		ns	
tSU2	M/–IO, A9-A23, A0 to PROCCLK Setup Time	33		24		ns	
tSU3	F16 to PROCCLK Setup Time	8		6		ns	
tSU4	CAS0, CAS1 to PROCCLK Setup Time	14		10		ns	
tSU5	RAS0, RAS1 to PROCCLK Setup Time	26		20		ns	
tSU6	–MEMW to PROCCLK Setup Time	10		10		ns	Note 1
tSU7	–MEMR to PROCCLK Setup Time	10		10		ns	Note 1
tSU8	–READY to PROCCLK Setup Time	15		10		ns	
tD9	–RASx Delay from PROCCLK		19		17	ns	
tD10	ADDSEL Delay from PROCCLK Leading Edge		20		20	ns	Note 2
tD11	–CASxy Delay from PROCCLK		22		19	ns	Note 3
tD12	IOCHRDY Delay from PROCCLK		20		20	ns	
tD13	–WS0 Active Delay from PROCCLK		20		20	ns	
tD14	–RAMWx Delay from PROCCLK		20		20	ns	
tD15	ADDSEL Delay from –RASx	4	12	4	12	ns	0 WS Non Page-mode
tD16	–RESET, –IRQ Delay from RESET, IRQ		20		18	ns	
tD17	ADDSEL Delay from –REF		25		25	ns	
t18	PROCCLK Period	31		25		ns	
t19	PROCCLK High Pulse Width	11		9		ns	Measured at 3.6 V
t20	PROCCLK Low Pulse Width	7		6		ns	
t21	PROCCLK Fall Time		4		4	ns	3.6 V to 1.0 V
t22	PROCCLK Rise Time		5		4	ns	3.6 V to 1.0 V
tSU23	–BHE to PROCCLK Setup Time	12		10		ns	
tH24	–BHE Hold Time from PROCCLK	0		0		ns	

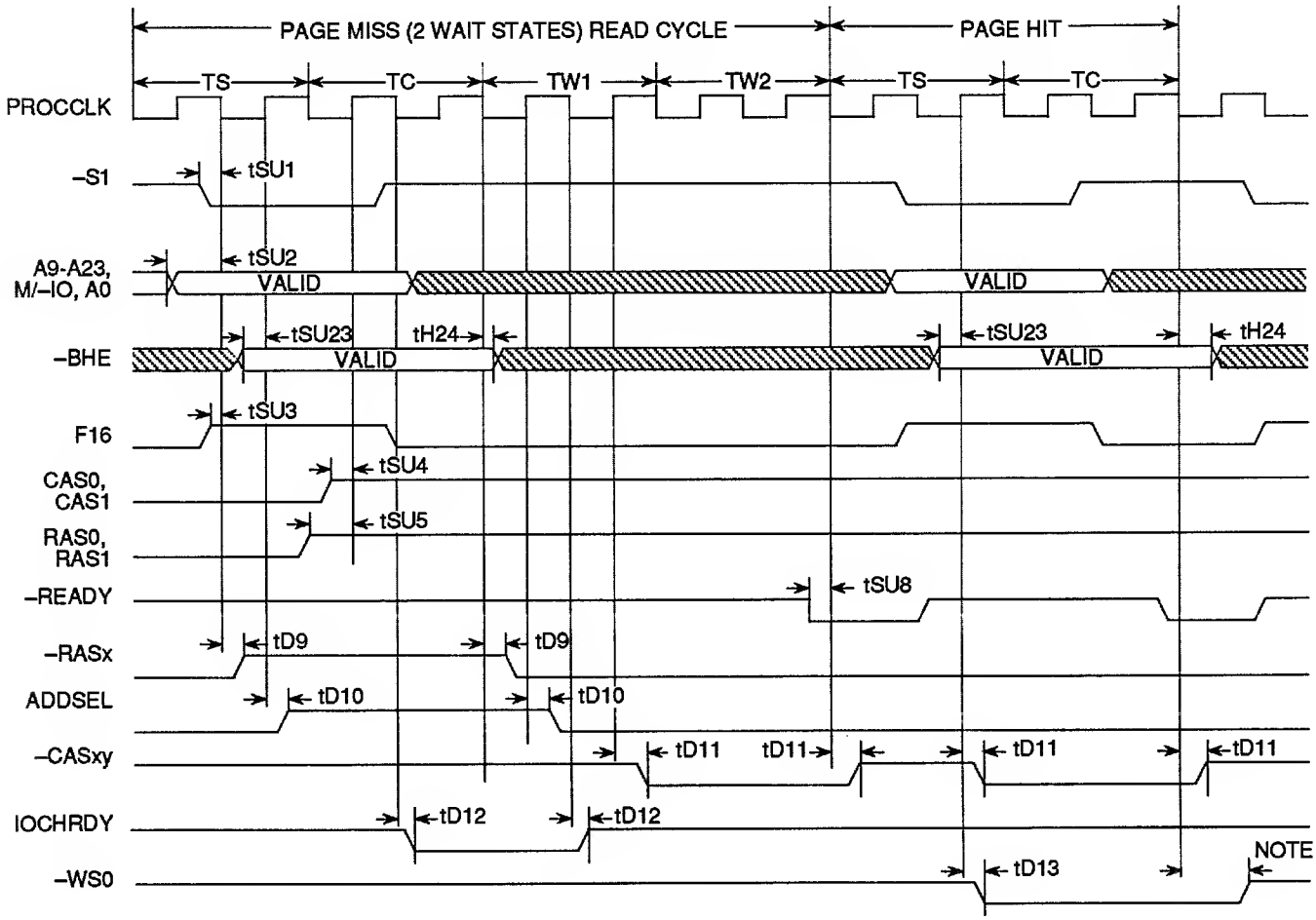
Notes: 1. –MEMR and –MEMW can be asynchronous to PROCCLK. They must meet the setup time to start the appropriate read or write cycle on the falling edge of PROCCLK. This spec is used in testing the parts.

2. ADDSEL is clocked off the rising edge of PROCCLK during all page-mode cycles and during one wait state normal cycles. During zero wait state normal cycles ADDSEL is clocked off the trailing edge of PROCCLK (see spec tD15).

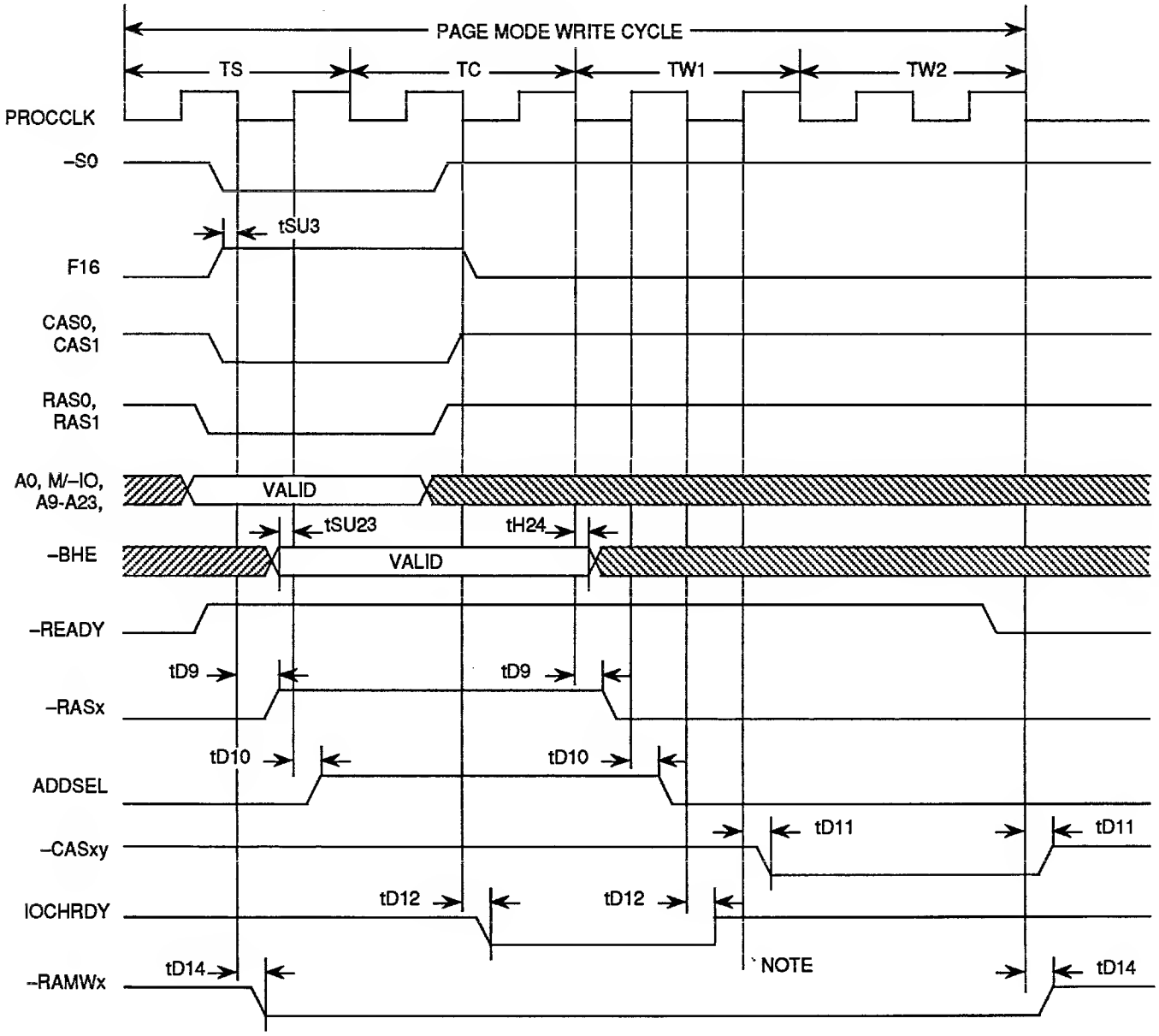
3. –CASxy signals are clocked off different edges of PROCCLK. All transition from active to inactive (0-1) are clocked off the falling edge of PROCCLK.

   During all page-mode cycles and all normal mode one wait state cycles the inactive to active transition is clocked off the rising edge of PROCCLK. During zero wait state normal mode cycles the inactive to active transition is clocked off the falling edge of PROCCLK.

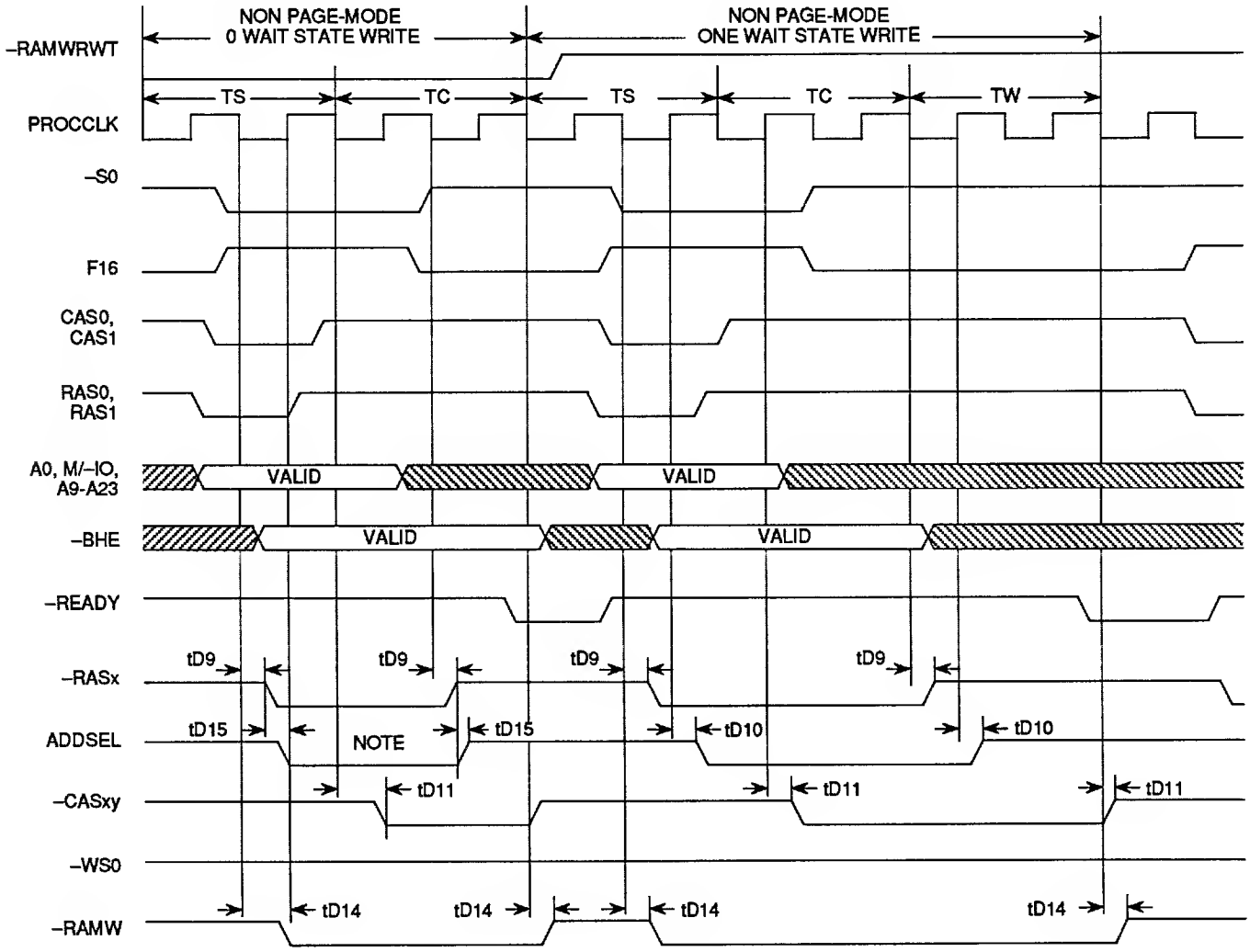
4. Inputs –PAGE, BANKSEL, RAMWRWT and RAMRDWT should be strapped to VDD or VSS to define the proper mode for a specific design.



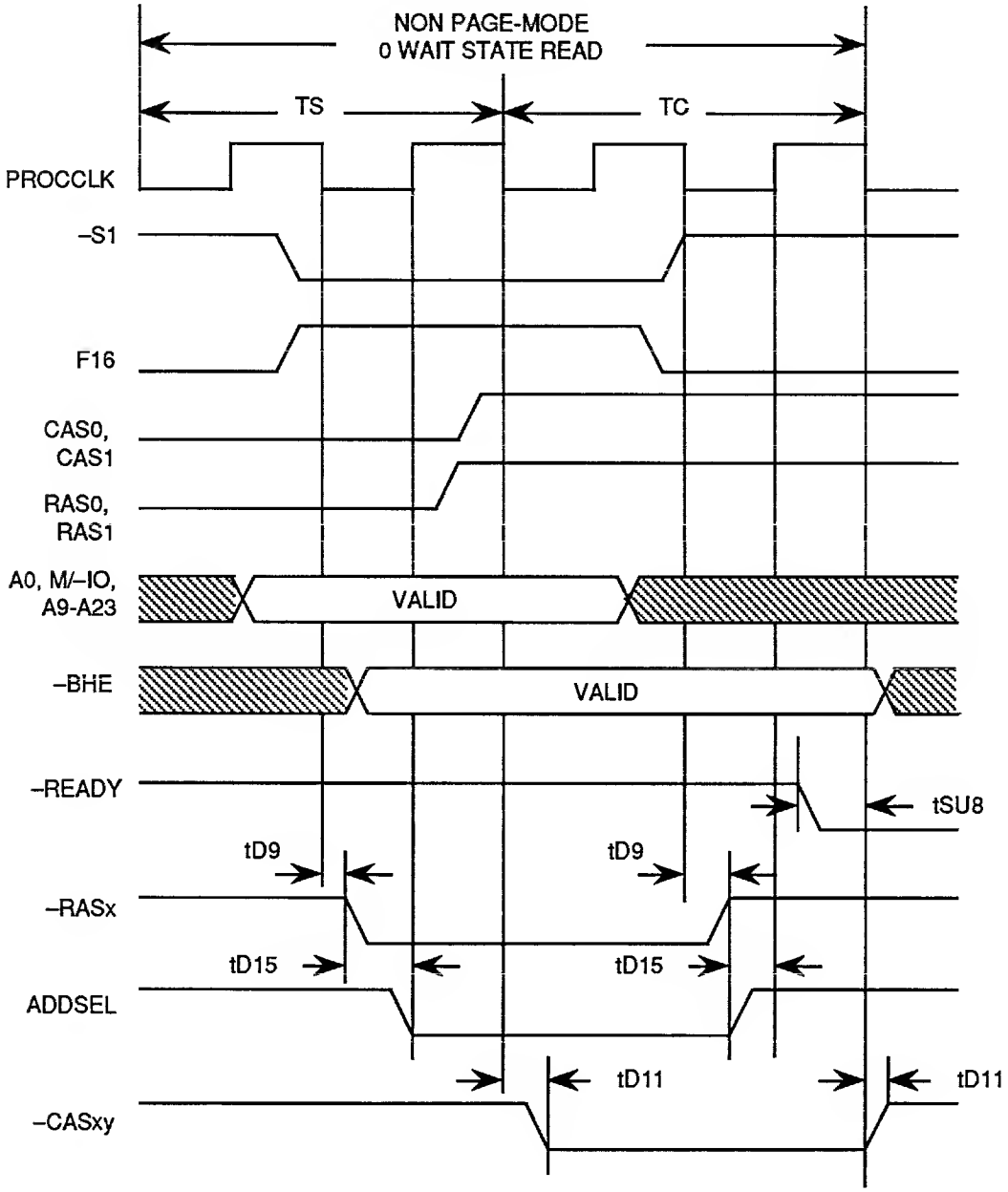
Note: -WS0 is an open drain output. The rise time depends on the size of the pull-up resistor used externally. -WS0 is released by the VL82C205 on the indicated rising edge of PROCCLK.



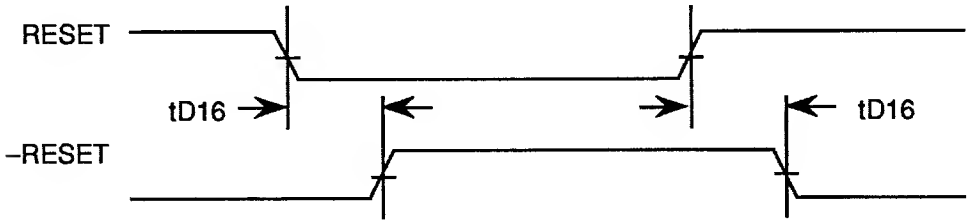
Note: IOCHRDY is three-stated after this PROCCLK rising edge.

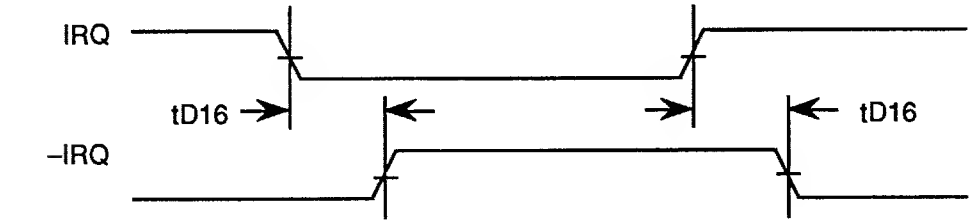


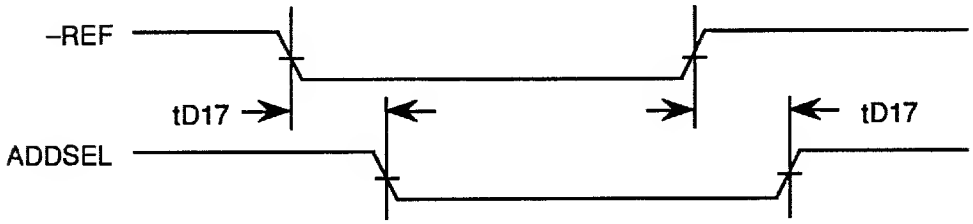
Note: In this mode ADDSEL follows -RASx off the trailing edge of PROCCLK. The delay between -RASx and ADDSEL is a minimum of 4 ns and a maximum of 12 ns.

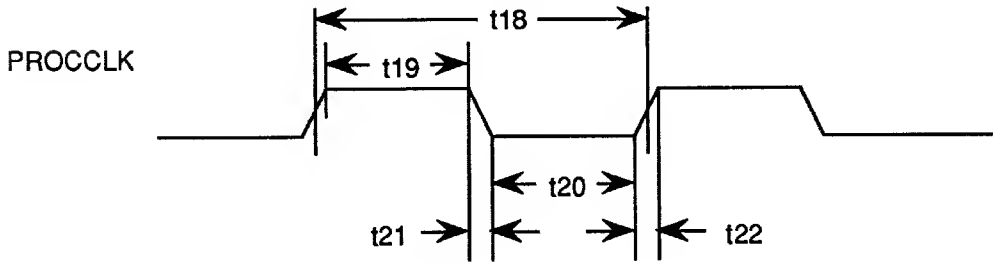

NON PAGE-MODE
0 WAIT STATE READ
TS
TC
PROCCLK
–S1
F16
CAS0,
CAS1
RAS0,
RAS1
A0, M/–IO,
A9-A23
VALID
–BHE
VALID
–READY
tSU8
tD9
tD9
–RASx
tD15
tD15
ADDSEL
tD11
tD11
–CASxy

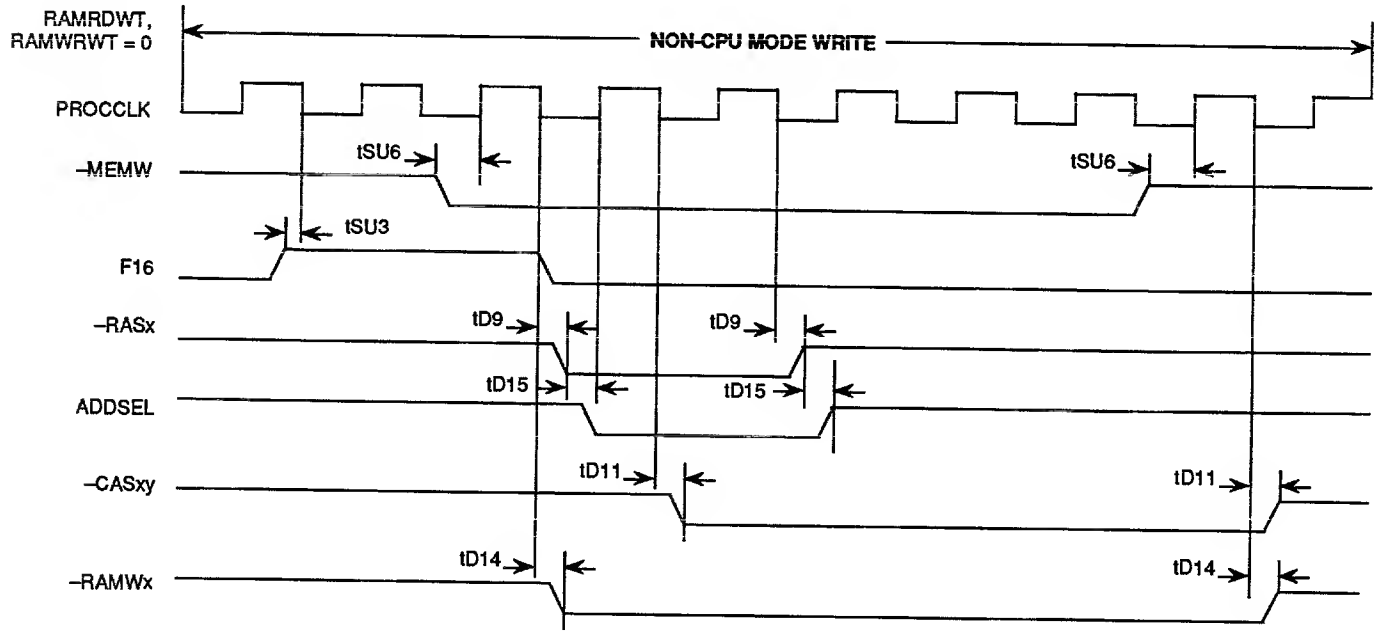
MISCELLANEOUS TIMINGS

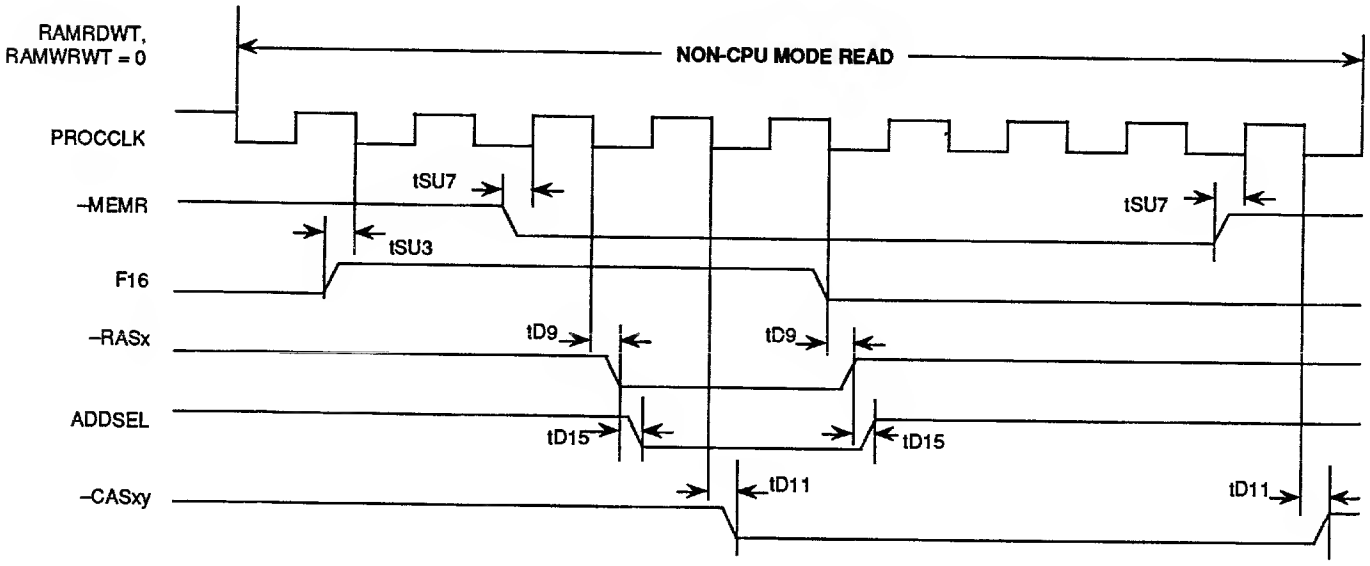


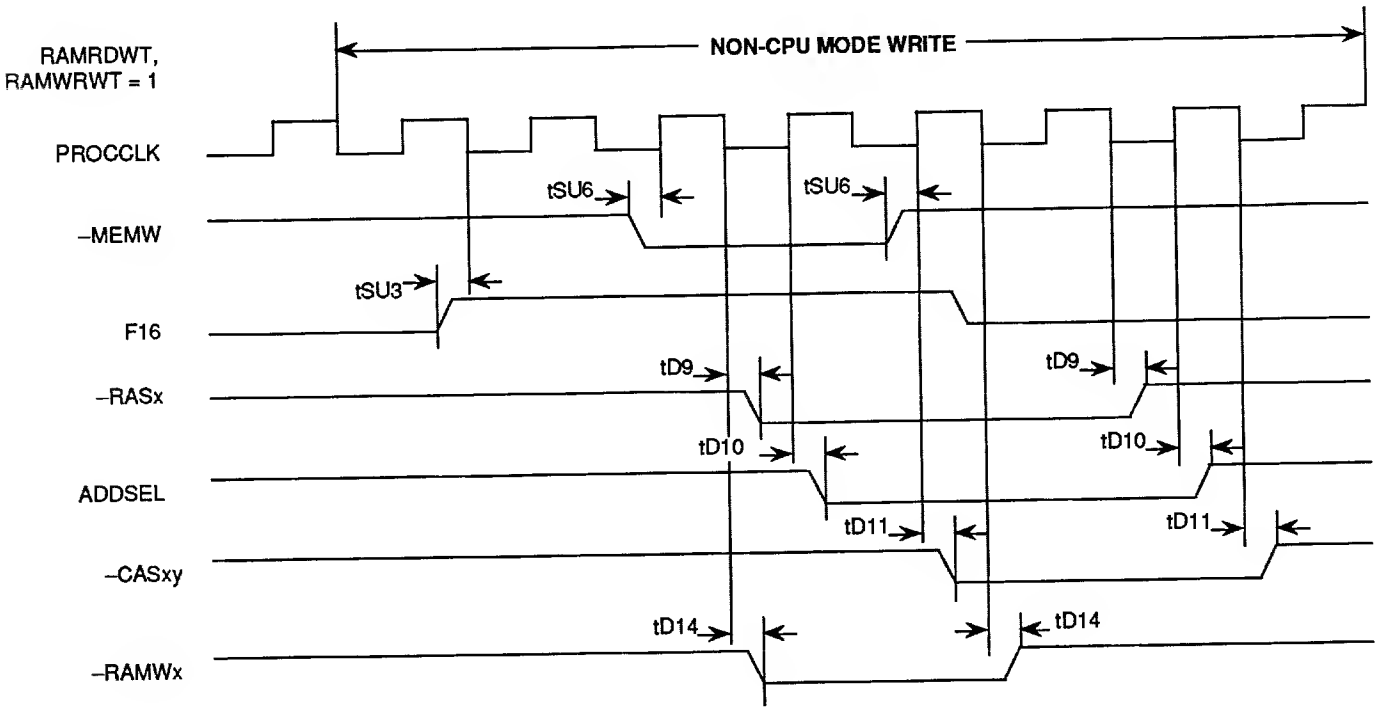


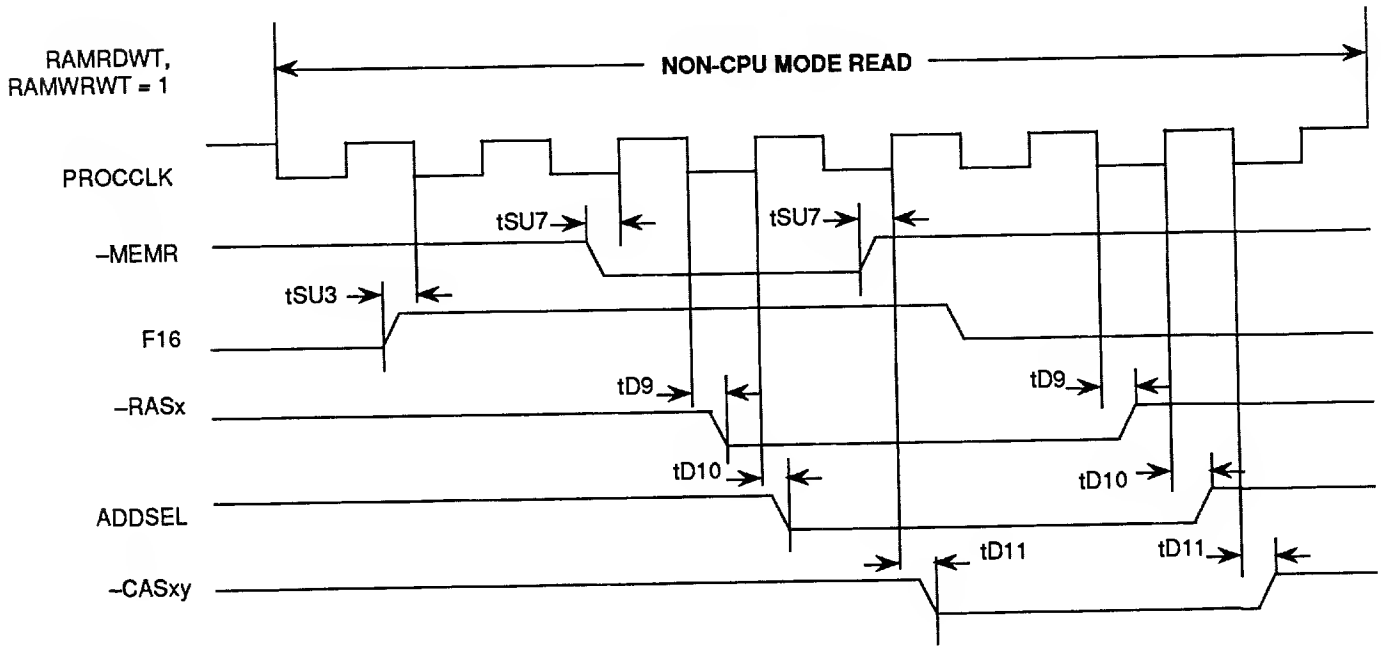




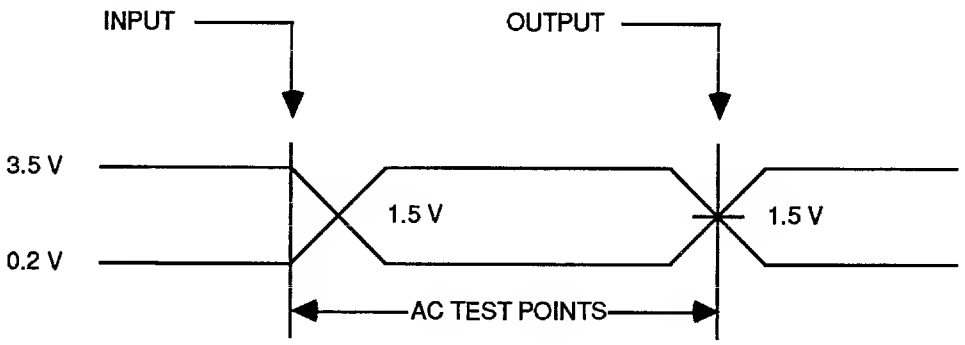

RAMRDWT,
RAMWRWT = 0
NON-CPU MODE WRITE
PROCCLK
–MEMW
tSU6
tSU6
tSU3
F16
–RASx
tD9
tD9
tD15
tD15
ADDSEL
–CASxy
tD11
tD11
–RAMWx
tD14
tD14


RAMRDWT,
RAMWRWT = 0
NON-CPU MODE READ
PROCCLK
–MEMR
tSU7
tSU7
tSU3
F16
–RASx
tD9
tD9
ADDSEL
tD15
tD15
–CASxy
tD11
tD11

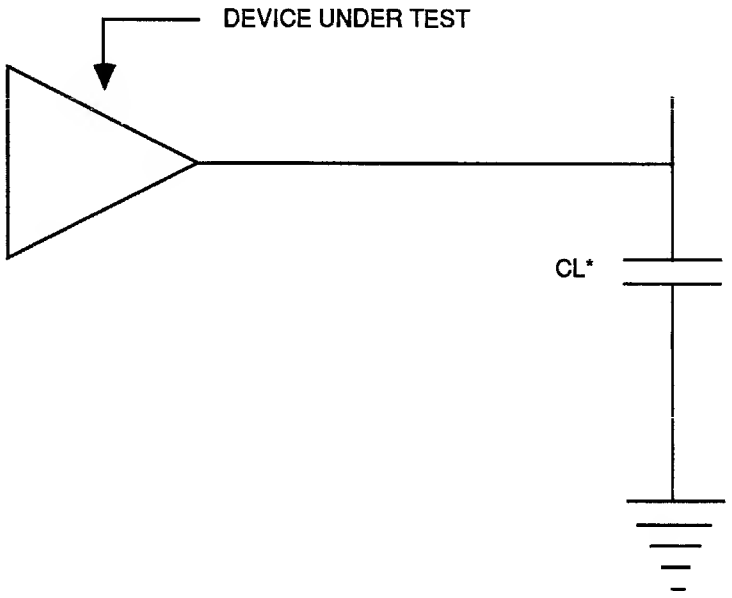

RAMRDWT,
RAMWRWT = 1
NON-CPU MODE WRITE
PROCCLK
tSU6
tSU6
–MEMW
tSU3
F16
tD9
tD9
–RASx
tD10
tD10
ADDSEL
tD11
tD11
–CASxy
tD14
tD14
–RAMWx


RAMRDWT,
RAMWRWT = 1
NON-CPU MODE READ
PROCCLK
tSU7
tSU7
–MEMR
tSU3
F16
tD9
tD9
–RASx
tD10
tD10
ADDSEL
tD11
tD11
–CASxy

AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
41, 43, 58, 59	200
45, 47-51, 53, 54	100
All Others	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +0.3 V
Applied Output Voltage	–0.5 V to +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	–WS0, IOCHRDY, CL = 200 pF, IOL = 24 mA
VOL2	Output Low Voltage		0.45	V	–RAMWA, –RAMWB, CL = 200 pF, IOL = 8 mA
VOL3	Output Low Voltage		0.45	V	–RASx, –CASxy, CL = 100 pF, IOL = 8 mA
VOL4	Output Low Voltage		0.45	V	All Other Pins, CL = 50 pF, IOL = 8 mA
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.6	VDD + 0.5	V	PROCCLK
CO	Output Capacitance		16	pF	
CI	Input Capacitance		8	pF	
CIN	Input Pin Capacitance		10	pF	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		25	mA	Note

Note: Inputs = VSS or VDD, outputs are not loaded.

VLSI TECHNOLOGY, INC.

SECTION 5

PS/2-COMPATIBLE DEVICES

Logic Products Division


VLSI TECHNOLOGY, INC.

VL82C031

IBM PS/2® MODEL 30-COMPATIBLE SYSTEM CONTROLLER

FEATURES

- Supports 8086 or V30 CPU at 8 MHz or 10 MHz zero wait state using 150 ns DRAMs
- Generates programmable fast and normal timing for PC memory
- Provides either DRAM or SRAM control
- Supports up to 8M bytes of expanded memory
- Supports 256K or 1M bit DRAMs on EMS memory
- Arbitrates the system bus among the CPU, DMA, math coprocessor, and DRAM memory refresh cycles
- Provides four channels of 8 MHz DMA as well as burst mode
- RAM pin available to select static or dynamic memory interface
- Power down mode for low power standby operation

DESCRIPTION

The VL82C031 provides the PS/2 Model 30-compatible system with dual speed control, 8 MHz or 10 MHz, to operate the system at peak performance. The device also controls memory, I/O, parity, address paths, and data paths as well as handling four channels of direct memory access. The VL82C031 is available from VLSI Technology, Inc. in an industry-standard plastic 100-pin flatpack.

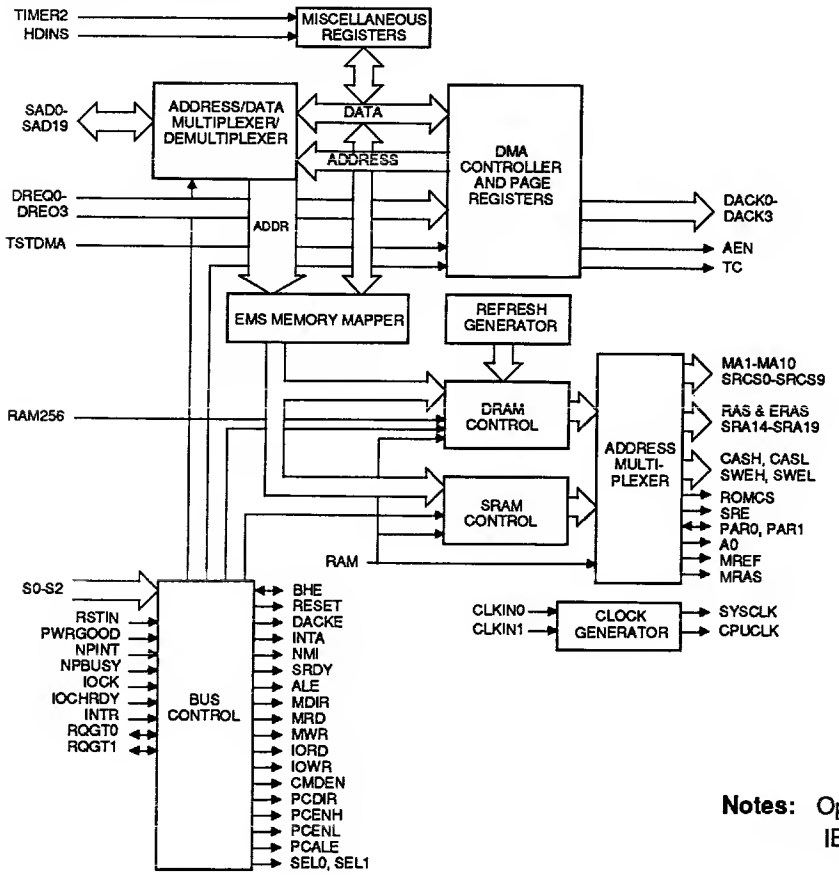
The CMOS VL82C031 is the System Controller device in the two-chip VLSI PS/2 Model 30-compatible chip set. The other device is the VL82C032 I/O Controller.

The chip set integrates logic on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30-compatible system, the VLSI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M bytes of memory using EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

The chip can be brought to a power-down mode to conserve power dissipation when static RAM is used. The chip can then be woke up from power-down mode by an external interrupt.

A third device, the VL82C037 VGA, Video Graphics Controller, is also used in the PS/2 Model 30-compatible system and provides high resolution graphics of up to 800 x 600 pixels with 16 colors. Graphic capabilities with this resolution are usually found only on more expensive systems.

BLOCK DIAGRAM

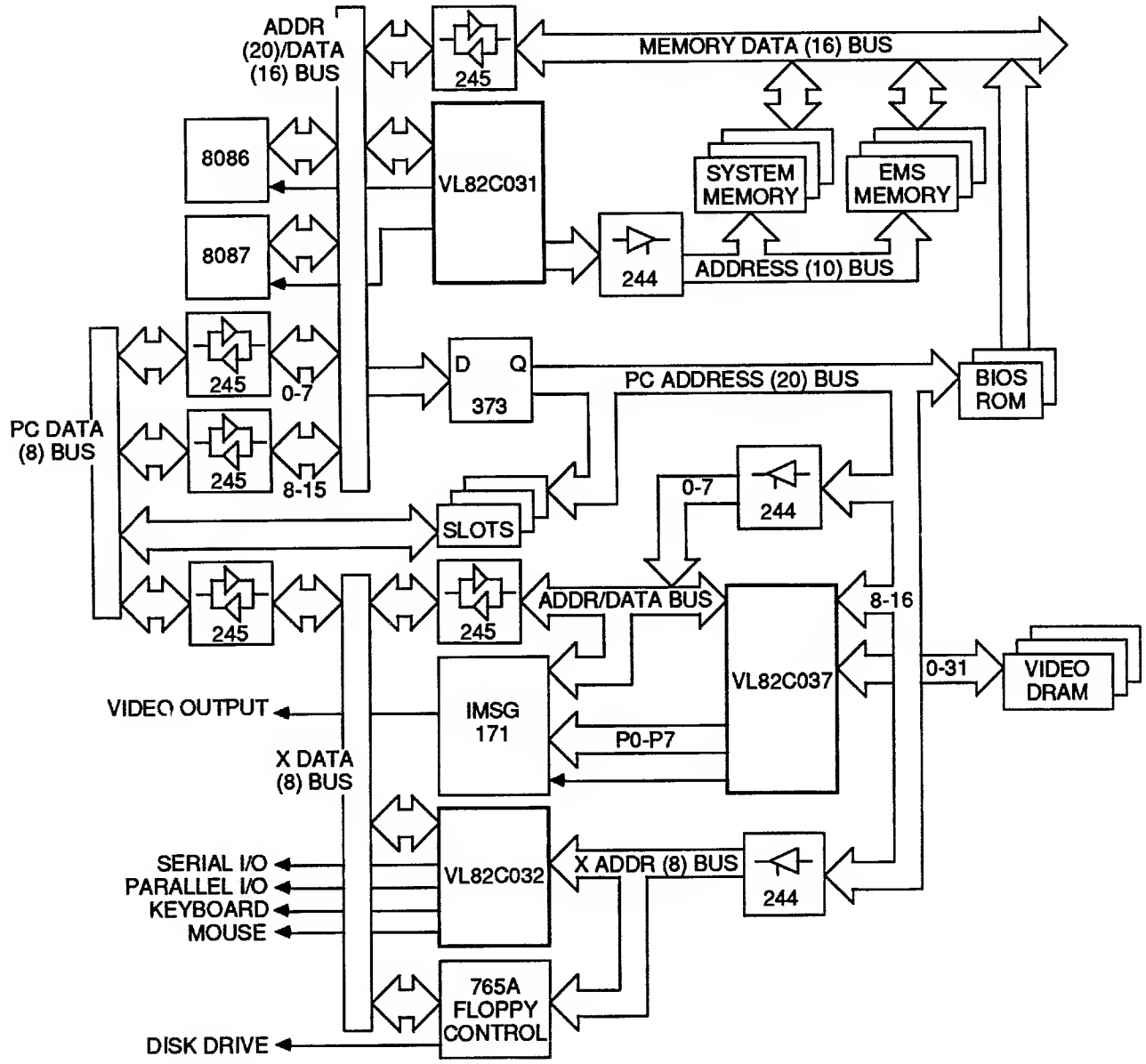


ORDER INFORMATION

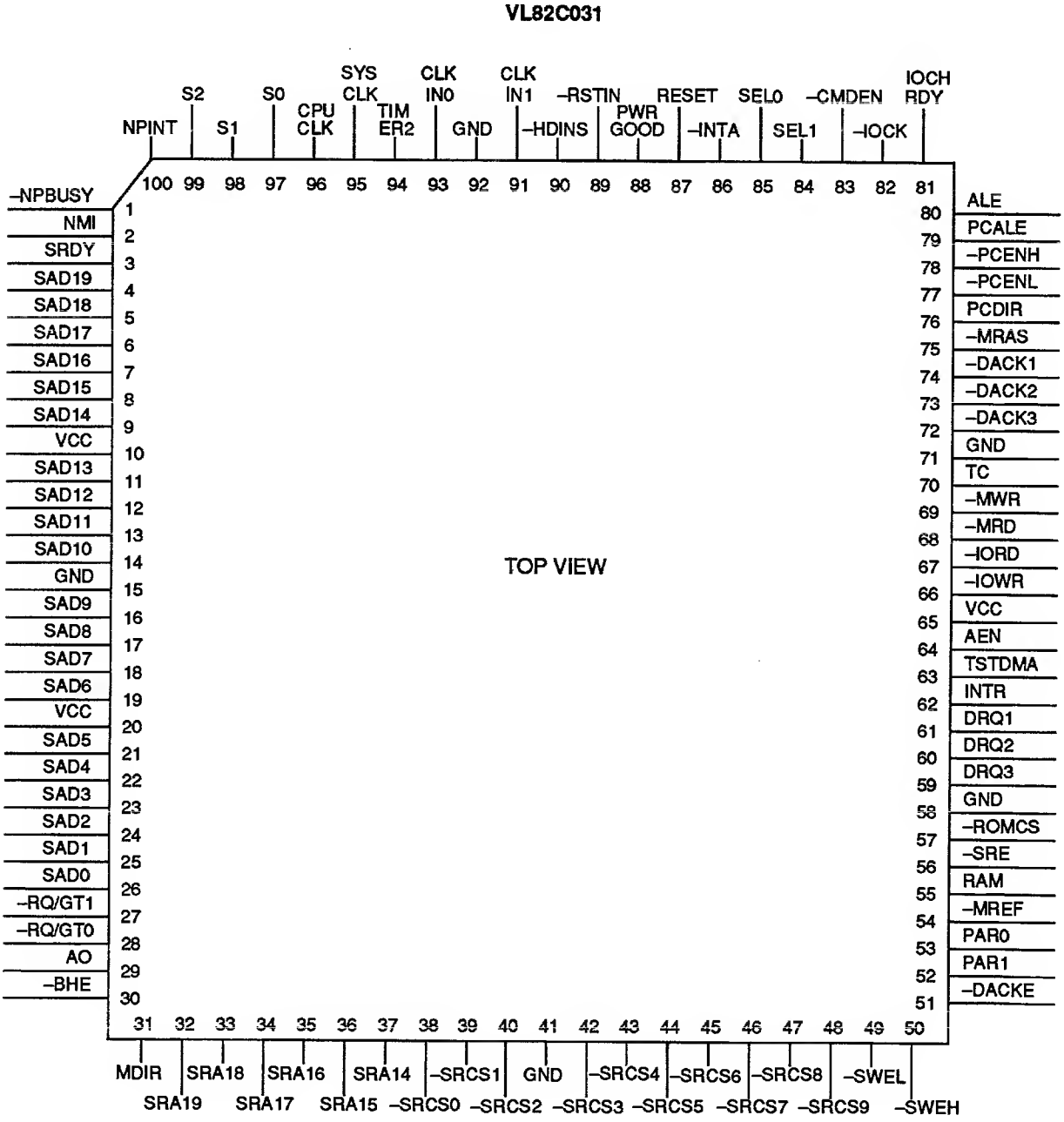
Part Number	Package
VL82C031-FC	Plastic Flatpack

Notes: Operating temperature range is 0°C to +70°C.
IBM PS/2® is a registered trademark of IBM Corp.

PS/2 MODEL 30-COMPATIBLE SYSTEM DIAGRAM

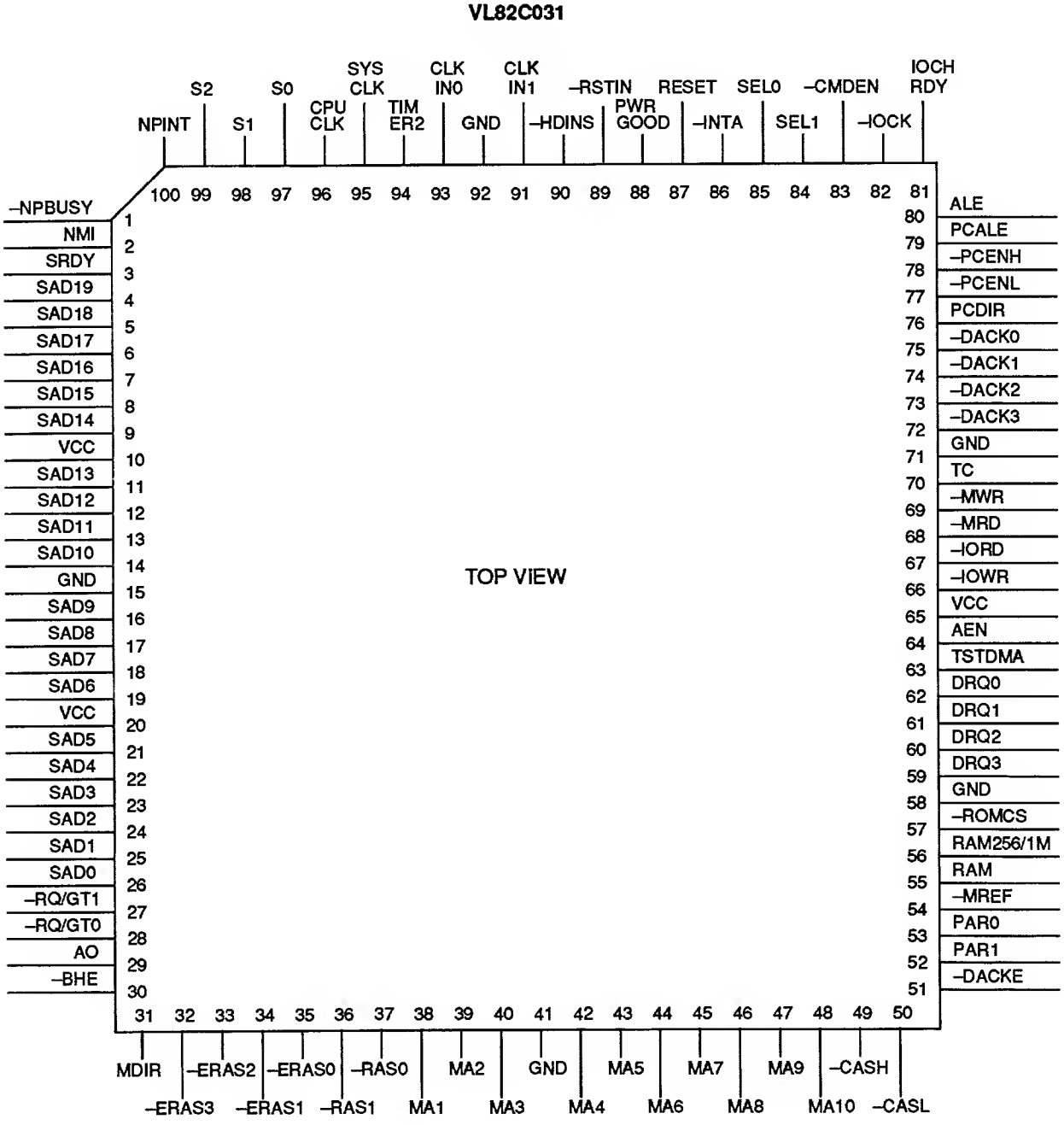


PIN DIAGRAM [When pin 55 (RAM) is tied low, SRAM configuration.]



5

PIN DIAGRAM [When pin 55 (RAM) is tied high, DRAM configuration.]



SIGNAL DESCRIPTIONS [With Pin 55 (RAM) tied to low, SRAM configuration]

Signal Name	Pin Number	Signal Type	Signal Description
–NPBUSY	1	I	Busy - Is an active low signal connected directly to the –BUSY signal of NP8087 which is normally connected to the –TEST signal of the 8086 CPU. It is examined by the bus arbitrator logic internally to the VL82C031.
NMI	2	O	Non Maskable Interrupt - Is an active high signal to the CPU that there is an exception caused by one of the following: - memory parity error, - I/O channel check signaled from the PC bus, - 8087 interrupts (an unmasked exception has occurred).
SRDY	3	O	System Ready - This is an active high signal that acknowledges to the CPU or 8087 at t3 or tW before t4 time that a data transfer for either memory or I/O is complete.
SAD19-SAD16	4-7	I/O	Address Bus - These lines are the four most significant address lines for memory operation. They are input lines when the CPU or 8087 is in control. The chip starts driving these lines during DMA address time.
SAD15-SAD0	8, 9, 11-14, 16-19, 21-26	I/O	Address and Data Bus - These lines are a time multiplexed address and data bus corresponding to the AD15-AD0 of 8086 and 8087 bus. The VL82C031 monitors these lines during the time the CPU or 8087 is in control of the bus. It will drive these lines during DMA address time.
–RQ/GT1	27	I/O	Request Grant Channel 1 - Is an active low pulse signal connected directly to –RQ/GT1 of the 8087. This signal is used by the chip to request the bus from the 8087. If the 8087 is not controlling the bus at that time, the request will relay through –RQ/GT0 of the 8087 which is connected to –RQ/GT1 of the CPU.
–RQ/GT0	28	I/O	Request Grant Channel 0 - Is an active low pulse signal connected directly to –RQ/GT0 of the CPU. This signal is used by the chip to request the bus from the CPU if there is no 8087, otherwise it is inactive.
A0	29	O	Address Line 0 - Is the latched version of address 0. It is used along with –BHE signal to distinguish 8/16 bit and odd/even byte operation.
–BHE	30	I/O	Byte High Enable - This is an active low signal used to enable data to the most significant half of the data bus (D15-D8). It is an input line when the CPU or 8087 is in control. The chip drives this signal during DMA time.
MDIR	31	O	Memory Direction - Controls memory write enable of memory devices and also the data direction of the transceiver between the CPU and system memory bus.
SRA16-SRA19	35-32	O	SRAM Address Bits 16-19 - If RAM is low, these bits drive an SRAM address decoder for the Expanded Memory option. The combination of SRA16-SRA19 is capable of selecting one of 15 32K X 8 SRAM banks organized as a word wide for a total of 960K bytes (15 banks of 64K each). Expanded memory is not selected if SRA16-SRA19 are 1111.
SRA14, SRA15	37, 36	O	SRAM Address Bits 14, 15 - If RAM is low, these are the two most significant address bits of the 32K X 8 SRAM.

–BHE	A0	Operation
0	0	Word (D15-D0)
0	1	Odd Byte (D15-D8)
1	0	Even Byte (D7-D0)
1	1	Not Used

5

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SRCS0- –SRCS9	38-40, 42-48	O	Static RAM Chip Select Bits 0-9 - If RAM is low, these are Static RAM Memory Chip Selects (active low). Each signal selects a bank of two 32K X 8 SRAM chips for a total of 640K bytes of system memory.
–SWEH, –SWEL	50, 49	O	SRAM Write Enable (High & Low) - If RAM is low, these are active low write enable signals for SRAM: - –SWEH for odd byte, - –SWEL for even byte.
–DACKE	51	O	DACK Enable - Is an active low control signal to enable either –DACK2 or –DACK3 to the on-board floppy and hard disk controllers respectively. This is a programmable signal based on the content of Chip Select Control Port 0065 (hex).
PAR0, PAR1	53, 52	I/O	Parity Bits 0-1 - Are the memory parity bits (odd type) for even and odd bytes of memory bank. Each parity bit is generated and written during a memory write operation. Each parity bit is checked and errors are reported by NMI to the system at the end of each memory cycle. PAR0 is the memory parity bit for even bytes. PAR1 is the memory parity bit for odd bytes.
–MREF	54	O	Memory Refresh - Is an active low signal indication of the refresh cycle. It is inhibited when RAM is low.
RAM	55	I	RAM Select - Is an input signal which indicates the memory type used in the system: - RAM = low = Static RAM, - RAM = high = Dynamic RAM.
–SRE	56	O	SRAM Read Enable - If RAM is low, it is an active low read enable signal for SRAM memory.
–ROMCS	57	O	ROM Chip Select - Is an active low signal used to enable the ROM BIOS to output data to the data bus.
DRQ1-DRQ3	61-59	I	DMA Request Bits 1-3 - Are asynchronous active high channel request inputs used by peripheral devices to obtain DMA service. –DACK will acknowledge the recognition of DRQ signals. These signals are compatible with the DRQ signals of the 8237 DMA controller.
INTR	62	I	Interrupt Signal - Is a positive edge signal to release the system from an idle state for power management.
TSTDMA	63	I	Test DMA Function - This signal is used for testing purposes of the internal DMA controller. It should be tied low.

Signal	Memory Space
–SRCS0	00000 - 0FFFF
–SRCS1	10000 - 1FFFF
–SRCS2	20000 - 2FFFF
–SRCS3	30000 - 3FFFF
–SRCS4	40000 - 4FFFF
–SRCS5	50000 - 5FFFF
–SRCS6	60000 - 6FFFF
–SRCS7	70000 - 7FFFF
–SRCS8	80000 - 8FFFF
–SRCS9	90000 - 9FFFF

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
AEN	64	O	Address Enable - Is an active high signal during the DMA cycle to disable any I/O devices from the I/O channel to allow DMA transfers to take place.
–IOWR	66	O	I/O Write Command - Is an active low signal to instruct an I/O device to read the data present on the data bus.
–IORD	67	O	I/O Read Command - Is an active low signal to instruct an I/O device to drive its data on the data bus.
–MRD	68	O	Memory Read Command - Is an active low signal to instruct the memory to drive its data on to the data bus.
–MWR	69	O	Memory Write Command - Is an active low signal to instruct the memory to store the data present on the data bus.
TC	70	I/O	Terminal Count - Is an active high pulse signal when any DMA transfer is completed. It can be driven from the I/O channel to terminate a current DMA cycle.
–DACK1- –DACK3	74-72	O	DMA Acknowledge Bits 1-3 - Are active low signals to notify the requesting peripherals when one has been granted a DMA cycle. These signals are compatible with the DACK signals of the 8237 DMA controller.
–MRAS	75	O	Memory Signal Timing - Is an active low control signal to indicate a system memory cycle.
PCDIR	76	O	PC Data Bus Direction - Is the direction signal to the data transceiver between the CPU and PC data bus: - high means the CPU drives the PC data bus (write cycle), - low means the PC drives the CPU data bus (read cycle).
–PCENL	77	O	PC Data Byte Low Bus Enable - Is the active low control signal to enable the data buffer (D7-D0) between the CPU and PC data bus.
–PCENH	78	O	PC Data Byte High Bus Enable - Is the active low control signal to enable the data buffer (D15-D8) between the CPU and PC data bus.
PCALE	79	O	PC Address Latch Enable - Is an active high pulse active during t1 of any bus cycle. It is similar to the ALE signal except that this signal is active high throughout the DMA cycle.
ALE	80	O	Address Latch Enable - Is an active high pulse active during t1 of any bus cycle including DMA and memory refresh cycles. The CPU address should be latched using the ALE falling edge.
IOCHRDY	81	I	I/O Channel Ready - Is an active high ready signal from an I/O channel. Memory or I/O devices can pull this signal low to lengthen memory or I/O cycles. For every system clock cycle this signal is low, one wait state is added.
–IOCK	82	I	I/O Channel Check - This signal should be pulled low for at least two system clock cycles to indicate an uncorrectable error on an I/O channel. This signal causes a Non Maskable Interrupt if NMI is enabled.
–CMDEN	83	O	Command Enable - Is the active low control signal to enable the command buffer going to the I/O channel bus (PC Bus). It is used to prevent bus contention between the I/O devices that share the same address space in the X bus and in the I/O channel bus.

5

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SEL0,SEL1	85, 84	O	Select Function (0-1) - These are special select decoders for address range according to the following table:
–INTA	86	O	Interrupt Acknowledge - This pin is an active low signal used to enable the interrupt controller's interrupt-vector data on to the data bus.
RESET	87	O	Reset - Is an active high signal synchronized to the system clock to reset the CPU and system.
PWRGOOD	88	I	Power Good - Is an active high signal (TTL level of 2.4 to 5.25 Vdc during normal operation, or an inactive level of 0.0 to 0.4 Vdc) coming from a power supply to indicate that power is stable.
–RSTIN	89	I	Reset Input - Is an active low signal which is used to generate the RESET signal. The VL82C031 provides a Schmitt Trigger input so that an RC connection can be used to establish the power on reset of proper duration.
–HDINS	90	I	Hard Disk Installed - Is the status signal that the hard disk is installed on the system. This can be read at I/O port 62 bit 2.
CLKIN1	91	I	Clock Input 1 - Is a 30 MHz TTL clock input with 40/60% duty cycle. It is used for a system clock with the CPU running at 10 MHz. It should be pulled high if there is no clock source to this pin.
CLKIN0	93	I	Clock Input 0 - A 24 MHz TTL clock input with 40/60% duty cycle. It is used for the system clock with the CPU running at 8 MHz, internal DMA control, and memory refresh timing.
TIMER2	94	I	Timer2 Status - Is the status signal on the 8253 Timer Channel 2 which comes from VL82C032. This is can be read at I/O port 62 bit 5.
SYSCLK	95	O	System Clock - Is the MOS driven clock signal to the 8087 and system. It has a 33% duty cycle (67-low, 33-high).
CPUCLK	96	O	CPU Clock - Is a MOS driven clock signal to 8086 or NEC V30 CPU. The clock speed can be selected through a special register. The duty cycle of CPU clock is 33% (67-low, 33-high).
S2-S0	99-97	I	System Status - These signals are used to decode different CPU or 8087 operations.

SEL1	SEL0	Range
0	0	Don't Care
0	1	A15-A10 = 0 (I/O)
1	0	ROM
1	1	Video RAM

S2-S0	Operation
000	Interrupt Acknowledge
001	I/O Read
010	I/O Write
011	Halt
100	Memory Read (fetch)
101	Memory Read (data)
110	Memory Write
111	Passive

SIGNAL DESCRIPTIONS (SRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
NPINT	100	I	8087 Numerical Processor Interrupt - An active high signal that indicates that an unmasked exception has occurred during numeric instruction execution when 8087 interrupt is enabled.
VCC	65, 20, 10		Power - +5 V
GND	92, 71, 41, 58, 15		Ground

SIGNAL DESCRIPTIONS [For pins which operate differently in DRAM configuration (Pin 55 tied high)]

Signal Name	Pin Number	Signal Type	Signal Description
–ERAS0- –ERAS3	35-32	O	EMS Row Address Strobe Bits 0-3 - If RAM is high, these are active low –RAS signals for Expanded Memory option to the system:
–RAS0, –RAS1	37, 36	O	Row Address Strobe Bits 0-1 - If RAM is high, these are active low control signals to the 640K byte DRAM system memory to inform the memory that a row address is present on the address bus. –RAS0 is for the first 128K and –RAS1 is for the next 512K of memory.
MA1-MA10	38-40, 42-48	O	Memory Address Bit 1-10 - If RAM is high, these are time multiplexed row and column memory address lines for 1M memory chips (for 256K memory chips MA10 is not used.)
–CASH- –CASL	49 ,50	O	Column Address Strobe (High & Low) - If RAM is high, these are active low control signals to the on-board DRAM system and EMS memory to signal that a column address is present on the address bus: - –CASH for odd byte [D(15-8)], - –CASL for even byte [D(7-0)].
–MREF	54	O	Memory Refresh - Is the active low signal indication of the refresh cycle. It is inhibited when RAM is low.
RAM	55	I	RAM Select - Is an input signal to tell the chip of the memory type used in the system: - RAM = low = Static RAM, - RAM = high = Dynamic RAM.
RAM256/1M	56	I	256K or 1M - If RAM is high, this is the signal which informs the chip of the memory type used in expanded memory: - low means 1M chips, - high means 256K chips.

	Pin	Odd	Even
–ERAS0	35	256K (1M)	256K (1M)
–ERAS1	34	256K (1M)	256K (1M)
–ERAS2	33	256K (1M)	256K (1M)
–ERAS3	32	256K (1M)	256K (1M)

5

SIGNAL DESCRIPTIONS (DRAM Configuration Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
DRQ0-DRQ3	62-59	I	DMA Request Bits 0-3 - Are asynchronous active high channel request inputs used by peripheral devices to obtain DMA service. –DACK will acknowledge the recognition of DRQ signals. These signals are compatible with the DRQ signals of the 8237 DMA controller.
–DACK0- –DACK3	75-72	O	DMA Acknowledge Bits 0-3 - Are active low signals to notify the requesting peripherals when one has been granted a DMA cycle. These signals are compatible with the DACK signals of the 8237 DMA controller.

FUNCTIONAL DESCRIPTION

SYSTEM MEMORY AND I/O MAP

The 8086/V30 supports 16 bit operations with 20 bit addressing to directly access up to 1M byte of memory space. The system memory and an On-board Expanded Memory (if it's enabled) are byte and/or word accessible. Memory is mapped in Table 1.

MEMORY CONTROL UNIT

VL82C031 offers either Dynamic or Static RAM memory control depending on the RAM input signal with zero wait states for 150 ns memory access.

If the "RAM" pin is strapped high (to VCC), the VL82C031 will generate on-board DRAM memory control signals. It supports 640K bytes of system memory using 64K X 4 DRAM for the first 128K bytes and 256K X 1 DRAM for the next 512K bytes of memory. In addition to 640K bytes, the VL82C031 also supports EMS 4.0 which makes multi-tasking possible. The EMS logic will support either 256K or 1M byte memory chips depending on how the RAM256/1M input signal is strapped. The EMS logic will control on-board memory up to 2M bytes if 256K memory is used and up to 8M bytes if 1M chips are used (see RAM256/1M input definition in the VL82C031 Signal Descriptions).

If the "RAM" pin is strapped low (to Ground), the VL82C031 will generate SRAM memory control. It supports 640K bytes of system memory using 32K X 8 SRAM chips. It also supports an EMS SRAM up to 960K (1M minus 64K) bytes of 32K X 8 type memory. It provides four address lines (SRA16-SRA19) that can select one out of 15 banks of memory (64K bytes each). When EMS SRAM is not accessed, SRA16-SRA19 will be all 1's so only 15 banks can be selected.

The Memory Control Unit has the following five functions:

1. System Memory Control
2. EMS Control
3. Memory Refresh Control
4. Memory Parity Check and Generator
5. Row and Column Address Generator

SYSTEM MEMORY CONTROL

FOR DRAM CONTROL: The system memory controller generates RAS signals for 640K of read/write memory:

- –RAS0 is for the first 128K of memory,
- –RAS1 is for the next 512K of memory.

FOR SRAM CONTROL: The system memory controller generates 10 SRAM chip selects (–SRCS0-SRCS9) as shown in Table 2 and read/write control signals (–SRE, –SWEH, –SWEL).

TABLE 1. FUNCTIONS

Hex Address	Description	
00000 - 1FFFF	128K byte: 1st bank #1	640K System Memory
20000 - 2FFFF	64K byte: 2nd bank #2	
30000 - 3FFFF	64K byte: 2nd bank #3	
40000 - 4FFFF	64K byte: 2nd bank #4	
50000 - 5FFFF	64K byte: 2nd bank #5	
60000 - 6FFFF	64K byte: 2nd bank #6	
70000 - 7FFFF	64K byte: 2nd bank #7	
80000 - 8FFFF	64K byte: 2nd bank #8	
90000 - 9FFFF	64K byte: 2nd bank #9	
A0000 - BFFFF	64K byte: Video Buffer	
C0000 - EFFFF	192K byte: Reserved for BIOS on I/O Channel.	
F0000 - FFFFF	64K byte: System ROM	

TABLE 2. MEMORY

Signal	Memory Space
–SRCS0	00000 - 0FFFF
–SRCS1	10000 - 1FFFF
–SRCS2	20000 - 2FFFF
–SRCS3	30000 - 3FFFF
–SRCS4	40000 - 4FFFF
–SRCS5	50000 - 5FFFF
–SRCS6	60000 - 6FFFF
–SRCS7	70000 - 7FFFF
–SRCS8	80000 - 8FFFF
–SRCS9	90000 - 9FFFF

The controller can allocate system memory through the Planar RAM Control Register at Port 006B. If the first 128K bytes of memory are not installed or bad, the system can remap the next 512K bytes over. Also, each 64K block of the second bank (except the first two blocks) can be enabled or disabled so the system can allocate memory between system memory and expanded memory.

If bit 0 of the Planar RAM register is 0, –RAS0 or –SRCS0-SRCS1 will be active at memory space 00000 - 1FFFF (128K bytes), and –RAS1 or –SRCS2-–SRCS9 will be active at memory space 20000 - 9FFFF (512K byte) for 640K bytes of system memory .

If bit 0 is 1, memory bank 0 is disabled (–RAS0 or –SRCS0- –SRCS1), and the physical memory at addresses 80000 - 9FFFF will be mapped to memory space 00000 - 1FFFF. Thus, –RAS1 or –SRCS2- –SRCS9 will be active in memory space 00000 - 7FFFF for 512K bytes of system memory.

The format of the Planar RAM Control/ Status Register is as follows:

Planar RAM Control Register: I/O Port 006B (hex) R/W:

Bit	Function
7	Parity Check Pointer 1 = Lower 128K failed 0 = Upper 512K failed
6	DIS/EN– RAM, 90000 - 9FFFF
5	DIS/EN– RAM, 80000 - 8FFFF
4	DIS/EN– RAM, 70000 - 7FFFF
3	DIS/EN– RAM, 60000 - 6FFFF
2	DIS/EN– RAM, 50000 - 5FFFF
1	DIS/EN– RAM, 40000 - 4FFFF
0	MAP/UNMAP– Low Memory

At power-on or reset, this port is 00.

If the EMS memory happens to be selected in the system memory space, –RAS0 and –RAS1 or –SRCS0-–SRCS9 will be blocked. Both –RAS0 and –RAS1 will be asserted during REFRESH. REFRESH is inhibited if "RAM" is low.

Bit 7 of Planar RAM Control Register will be set (1) or clear (0) according to the most recent parity bit error:

- If the current memory read cycle is in the first 128K memory and caused a parity error, bit 7 will be set.
- If the current memory read cycle is in the next 512K memory and caused a parity error, bit 7 will be cleared.
- If there is no parity error, bit 7 will remain unchanged.
- Writing a 1 to bit 7 of this port will reset this bit. Writing a 0 to this bit has no effect.

This feature is primarily intended for use in memory testing and is not particularly useful for post-mortem diagnostics.

EMS CONTROL

The EMS Control consists of EMS Current Map, EMS Alternate Map, and the EMS RAS generator.

The Current and Alternate Maps are 36 word by 10 bit register files each containing an enable bit and the physical address bits 22-14 of the EMS memory. The memory space is logically broken down to 64 blocks of 16K bytes each. However, the first 256K of system memory (00000 - 3FFFF), Video memory (40000 - BFFFF), and ROM BIOS (F0000 - FFFFF) are reserved. That leaves two areas of memory: 40000 - 9FFFF and C0000 - EFFFF mappable to EMS. Each block of 16K bytes can be mapped to any of n blocks of EMS memory. (If RAM256/1M is high, n = 128. If RAM256/1M is low, n = 512.) EMS can access up to 2M or 8M bytes of DRAM depending on the state of RAM256/1M.

If SRAM is used (i.e. Pin 55 is tied low) the maximum EMS memory will be 1M minus 64K (960K) bytes of SRAM, that is n = 60.

The EMS Current Map is a 36 word by 10 bit register file that translates A14-A19 during memory cycles to an EMS memory address. The EMS Current Memory Map can be accessed through three I/O ports:

CMPR - Current Map Pointer Register 8-bit I/O R/W

CMDR - Current Map Data Register 16-bit I/O R/W

The CPU performs an I/O write to CMPR with a pointer to the current map. After that, the CPU performs I/O reads or writes to CMDR.

The CMPR and CMDR formats are:

CMPR: I/O Port 0011 R/W:

Bit	Function
7, 6	Not Used
5-0	Current Map Ponter

CMDR: I/O Port 0012 R/W word access only:

Bit	Function
15-10	Not Used
9	Map Address 22 for EMS Memory
8	Map Address 21 for EMS Memory
7	EN/DIS-
6	Map Address 20 for EMS Memory
5	Map Address 19 for EMS Memory
4	Map Address 18 for EMS Memory
3	Map Address 17 for EMS Memory
2	Map Address 16 for EMS Memory
1	Map Address 15 for EMS Memory
0	Map Address 14 for EMS Memory

The type of memory and map address bits used in EMS are determined by the RAM and RAM256/1M input pins as shown in Table 3.

TABLE 3. MEMORY CONFIGURATION OPTIONS

RAM	256/1M	Type of Memory	Map Bits Used
0	X	32K X 8 SRAM	14-19
1	0	1M DRAM	14-22
1	1	256K DRAM	14-20

X = Don't Care

When RAM is low, and during EMS memory access, SRA14-SRA19 are identical to the map address. SRA14-SRA19 are all high if the access is not in EMS memory.

CMDR bit 7: EN/DIS- is used to enable or disable mapping of the logical memory address space to the EMS memory area. If this bit is set to 1, it will use the map address 21-14 during the memory access time to map to the EMS memory, otherwise it will be unmapped and either system memory or memory on the I/O channel will be accessed.

The EMS Alternate Map is a 36 word by 10 bit register file that translates A14-A19 during DMA memory cycles to the EMS memory. The EMS Alternate Memory Map can be accessed through three I/O ports:

AMPR - Alternate Map Pointer Register 8-bit I/O R/W
AMDR - Alternate Map Data Register 16-bit I/O R/W

The CPU performs an I/O write to AMPR with a pointer to the alternate map. After that, the CPU performs I/O reads or writes to AMDR.

The AMPR and AMDR formats are:

AMPR: I/O Port 0015 R/W:

Bit	Function
7, 6	Not Used
5-0	Alternate Map Pointer

AMDR: I/O Port 0016 R/W word access only:

Bit	Function
15-10	Not Used
9	Map Address 22 for EMS Memory
8	Map Address 21 for EMS Memory
7	EN/DIS-
6	Map Address 20 for EMS Memory
5	Map Address 19 for EMS Memory
4	Map Address 18 for EMS Memory
3	Map Address 17 for EMS Memory
2	Map Address 16 for EMS Memory
1	Map Address 15 for EMS Memory
0	Map Address 14 for EMS Memory

The type of memory and map address bits used in EMS are determined by the same system as with the current map. See Table 3.

The EMSEN I/O port enables or disables the EMS Current or Alternate Memory Map during CPU or NPU accesses:

EMSEN: I/O Port 0010 R/W:

Bit	Function
7-2	Not Used
1	EN/DIS- Alternate Map
0	EN/DIS- Current Map

Bit 0 and 1 of this port are Master EMS Enable bits used to enable or disable the EMS memory access function during the CPU or NPU memory access cycles. Writing a 1 to the EMSEN port bit 0 and/or bit 1 enables the EMS Current Map and/or Alternate Map to function. Otherwise, the EMS memory is not accessible. However, the EMS Current and Alternate Memory Maps are always accessible. If both bit 0 and 1 are set to 1's, the Current Memory Map will be used. See Table 4.

If one of the maps is selected but the EN/DIS- bit for the current page is 0, the memory access will go to CPU system memory, or the I/O channel if that address space is disabled through the Planar RAM Control Register.

The EMS RAS signals are always generated during memory refresh. At power-on or reset, bits 0 and 1 are 0's.

EMDMA is an I/O port used to tag any DMA channel to the Current or Alternate Map access during the DMA cycle:

EMDMA I/O Port 0014 R/W:

Bit	Function
7	EMCDMA3 : EN/DIS- Current Map during DMA Channel 3.
6	EMCDMA2 : EN/DIS- Current Map during DMA Channel 2.
5	EMCDMA1 : EN/DIS- Current Map during DMA Channel 1.
4	EMCDMA0 : EN/DIS- Current Map during DMA Channel 0.
3	EMADMA3 : EN/DIS- Alternate Map during DMA Channel 3.
2	EMADMA2 : EN/DIS- Alternate Map during DMA Channel 2.
1	EMADMA1 : EN/DIS- Alternate Map during DMA Channel 1.
0	EMADMA0 : EN/DIS- Alternate Map during DMA Channel 0.

There are four pairs of bits: 0,4; 1,5; 2,6; 3,7 that are related directly to each channel of the DMA in map selection

TABLE 4. GLOBAL EMS MAPPING

EMSEN Bit 1	EMSEN Bit 0	Map of EMS Memory Access During CPU or NPU Access cycles
0	0	None
0	1	Current Map
1	0	Alternate Map
1	1	Current Map

TABLE 5. EMS DMA ASSIGNMENT

EMDMA Bits 0,4; 1,5; 2,6; 3,7	Map of Memory Access During DMA Cycles
0, 0	None (map to system memory or I/O channel)
1, 0	Alternate Map
0, 1	Current Map
1, 1	Alternate Map

At power-on or reset, EMDMA = 00.

during each DMA cycle. The function of those bits are defined in Table 5.

If one of the maps is selected but the EN/DIS- bit for the current page is 0, the memory access will go to CPU system memory, or the I/O channel if that address space is disabled through the Planar RAM Control Register.

The EMS RAS Generator takes the content of CMDR or AMDR during memory access and generates the EMS RAS signals:

- ERAS0 : For EMS Bank 0.
- ERAS1 : For EMS Bank 1.
- ERAS2 : For EMS Bank 2.
- ERAS3 : For EMS Bank 3.

EMST: The EMS Parity Status Port Register is an eight bit I/O read only port used to identify the source of EMS parity errors if the EMS function is enabled:

EMST: I/O Port 0018 Read:

Bit	Function
7	EMSERR : EMS memory parity error.
6	Not Used
5	ODDBYTE : Odd byte is bad, if EMSERR is set.
4	EVENBYTE : Even byte is bad, if EMSERR is set.
3	EMSBNK3 : EMS memory bank 3 is bad, if EMSERR is set.
2	EMSBNK2 : EMS memory bank 2 is bad, if EMSERR is set.
1	EMSBNK1 : EMS memory bank 1 is bad, if EMSERR is set.
0	EMSBNK0 : EMS memory bank 0 is bad, if EMSERR is set.

EMST: I/O Port 0018 Write:

Bit	Function
7	EN/DIS- : EMS memory parity error.
6	Not Used
5	EN/DIS- : Odd parity byte, if EMSERR is set.
4	EN/DIS- : Even parity byte, if EMSERR is set.
3	EN/DIS- : EMS memory parity bank 3, if EMSERR is set.
2	EN/DIS- : EMS memory parity bank 1, if EMSERR is set.
1	EN/DIS- : EMS memory parity bank 1, if EMSERR is set.
0	EN/DIS- : EMS memory parity bank 0, if EMSERR is set.

Writing 0 to these bits will reset the corresponding parity bits to 0.

At power-on or reset, EMST = 00.

The mapping registers are implemented internally as static RAM register files, and can be disabled to reduce power consumption for applications such as laptop computers. This is done by writing a 1 to I/O Port IEh to enable the funtion, and then writing a 1 or 0 to I/O Port 1Ch to enable or disable the register banks, respectively. Reading I/O Port 1Ch at this point will disable the register banks and stop the CPUCLK output. An active signal on the INTR input (pin 62) will then restart the CPU clock. During the shutdown period the SYSCLK output continues to run.

CLOCK CONTROL

The speed and duty cycle of the clock outputs can be controlled through the Clock Control Register which resides at I/O Port 19h.

Clock Control: I/O Port 0019 R/W:

Bit	Function
7-3	Not Used
2	CPUCLK Duty Cycle - 0 = 33%, 1 = 50%
1	Divider Select - 0 = +6, 1 = +3
0	Clock Select - 0 = CLKIN0, 1 = CLKIN1

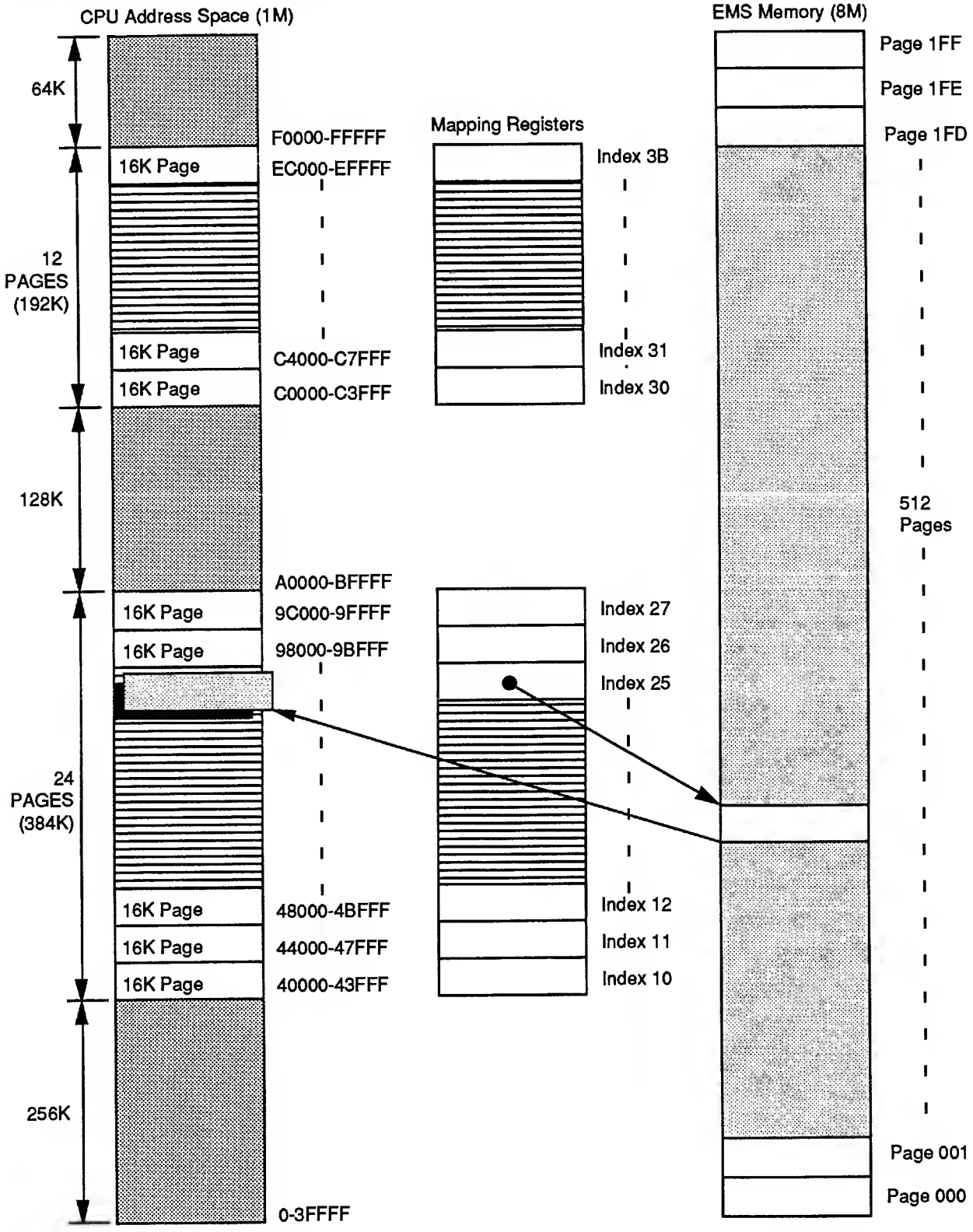
Both of the clock outputs (CPUCLK and SYSCLK) are affected by clock input and clock divider selection. Only the CPUCLK is affected by duty cycle selection.

5

VL82C031 I/O MAP

I/O Address	Function	Response
0000 - 000F	DMA Controller	R/W
0010 - 001F	System Control and Status Group 1	R/W
006B	Planar RAM Control	R/W
0081 - 0087	DMA Page Registers	R/W
03B0 - 03DF	Video System	On-Board Decoder

FIGURE 1. EMS MAPPING REGISTERS



MEMORY REFRESH CONTROL

The Memory Refresh Timer generates a request every 15.6 µs to the Refresh Controller. Once the Refresh Controller grants the cycle (–MREF is asserted), it outputs the ALE, PCALE, and –MRD signals. The minimum refresh cycle is five system clocks for a system running at 8 MHz or six system clocks for a system running at 10 MHz.

The Memory Refresh Address Generator drives all 20 address lines through the CPU bus during memory refresh cycle time (–MREF is low). Address 0-8 comes from a 9-bit binary counter (which will increment at the end of the cycle), and A9-A19 is driven low during the memory refresh cycle.

DMA CONTROL

DMA Control consists of two blocks:

- 8237-Compatible DMA Controller
- DMA Page Registers

The DMA Controller is a four channel DMA operating at 8 MHz which supports byte (8-bits) transfer operations between memory and peripherals. Its function is equivalent to the 8237 DMA chip. The DMA channels are assigned as shown in Table 6.

Each channel can transfer data throughout the 1M byte system address space up to 64K bytes at a time. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller
Address	A19 ◄——► A16	A15 ◄—► A0

Note: The addressing signal, 'byte high enable' (–BHE), is generated by inverting address line A0.

Three DMA channels (1, 2, 3) are available on the I/O channel. The 8237 DMA controller command code addresses are shown in Table 8.

DMA PAGE REGISTER

DMA Page Registers can be accessed through four 8-bit I/O ports. These ports are read/write and only data bits 0-3 are significant. Table 7 shows the addresses for the page registers.

Addresses for all DMA channels cannot increase or decrease through page boundaries (64K bytes).

5

TABLE 6. DMA CHANNELS

Channel	Assignment
Channel0: DRQ0	Reserved
Channel1: DRQ1	Not Used
Channel2: DRQ2	Diskette
Channel3: DRQ3	Fixed Disk

TABLE 7. PAGE REGISTERS

Page Register	I/O Address (In Hex)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082

TABLE 8. DMA CONTROLLER REGISTER FUNCTIONS

I/O Address (In Hex)	Register Function
0000	Channel 0 Base and Current Address Register
0001	Channel 0 Base and Current Word Count
0002	Channel 1 Base and Current Address Register
0003	Channel 1 Base and Current Word Count
0004	Channel 2 Base and Current Address Register
0005	Channel 2 Base and Current Word Count
0006	Channel 3 Base and Current Address Register
0007	Channel 3 Base and Current Word Count
0008	Read Status Register/Write Command Register
0009	Write Request Register
000A	Write Single Mask Register Bit
000B	Write Mode Register
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Register/Write Master Clear
000E	Clear Mask Register
000F	Write All Mask Register Bits

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
tCYC	SYSCLK, CPUCLK Cycle Time	100		ns	
tC1	CLKIN0 Cycle Time	42		ns	24 MHz
tC2	CLKIN1 Cycle Time	33		ns	30 MHz
tC3	SYSCLK High Time	33		ns	33% Duty Cycle
tC4	SYSCLK Low Time	60		ns	33% Duty Cycle
tC5	CPUCLK High Time	33		ns	33% Duty Cycle
		47		ns	50% Duty Cycle
tC6	CPUCLK Low Time	60		ns	33% Duty Cycle
		47		ns	50% Duty Cycle
t7	SYSCLK to Command		25	ns	
tD8	SYSCLK Low to ALE, PCALE High		42	ns	
tD9	SYSCLK High to ALE, PCALE Low		30	ns	
tD10	SYSCLK to SRDY		35	ns	
tD11	SYSCLK Low to Address on I/O Channel		75	ns	
tSU12	Data Valid before t4 during Read	25		ns	
tH13	Data Invalid after End of t3 during Read		5	ns	
tD14	Data from End of t1 during Write		75	ns	
tD15	Memory Row Address Valid from SYSCLK Low		100	ns	
tD16	Memory Column Address Valid from SYSCLK Low		43	ns	
tD17	SYSCLK to –RAS		20	ns	
tD18	SYSCLK to –CAS		20	ns	
tD19	Memory Data Valid from –RAS		155	ns	
tD20	Memory Data Valid from –CAS		75	ns	
tSU21	Memory Data Valid before t4	20		ns	
tH22	Memory Data Invalid after –CAS		20	ns	
tD23	Memory Data Valid after SYSCLK Low during Write		75	ns	
tH24	Memory Data Hold Time after –CAS	20		ns	
tD25	Request/Grant from SYSCLK Low		25	ns	
tD26	Refresh after SYSCLK Low		40	ns	
tD27	PCALE after SYSCLK High during Refresh		30	ns	
tD28	Memory Refresh Address after PCALE		25	ns	
tD29	–RQ/GT Request from DRQ		2 tCYC	ns	
t30	DRQ Hold Time after –DACK		0	ns	
tH31	PCALE High from –RQ/GT Grant		30	ns	

AC CHARACTERISTICS: (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
tH32	Data Hold Time from t4 SYSCLK High during Write	35		ns	
tD33	PCALE Low from End of DMA Command		2 1/2 tDCY +35	ns	tDCY=DMA Cycle Time Min 125 ns
tD34	AEN High from –RQ/GT Grant		1/2 tDCY +35	ns	
tD35	AEN Low from End of DMA Command		2 1/2 tDCY +35	ns	
tD36	–DACK Low from AEN		3 tDCY +70	ns	
tD37	–DACK High from End of DMA Command		1/2 tDCY +40	ns	
tD38	DMA Address Valid from AEN		3 tDCY +30	ns	
tD39	–MRD, –IORD Active from AEN		3 1/2 tDCY +35	ns	
tD40	–MWR, –IOWR Active from –MRD, –IORD		2 tDCY	ns	
t41	–MWR, –IOWR Command Width	4 tDCY		ns	
t42	–MRD, –IORD Command Width	6 tDCY		ns	
tD43	End of DMA Command to –RQ/GT Release		2 tDCY	ns	

5

MAXIMUM OUTPUT CAPACITANCE LOADING

Pinout	Capacitance Loading (pF)
CPUCLK	20
SYSCLK	20
RESET	200
–INTA	15
SEL0	30
SEL1	30
–CMDEN	15
ALE	20
PCALE	15
–PCENH	15
–PCENL	15
PCDIR	20
–DACK3- –DACK0	200
TC	15
–MWR	25

Pinout	Capacitance Loading (pF)
–MRD	25
–IORD	25
–IOWR	25
AEN	200
–ROMCS	20
–MREF	200
PAR0	100
PAR1	100
–DACKE	15
–CASL	45
–CASH	45
MA1-MA10	20
–RAS0	20
–RAS1	20
–ERAS0	20

Pinout	Capacitance Loading (pF)
–ERAS1	20
–ERAS2	20
–ERAS3	20
MDIR	15
–BHE	15
A0	15
–RQ/GT0	20
–RQ/GT1	20
SAD19-SAD0	40
SRDY	35
NMI	20

TIMING CHARACTERISTICS

FIGURE 2. CLOCK TIMING

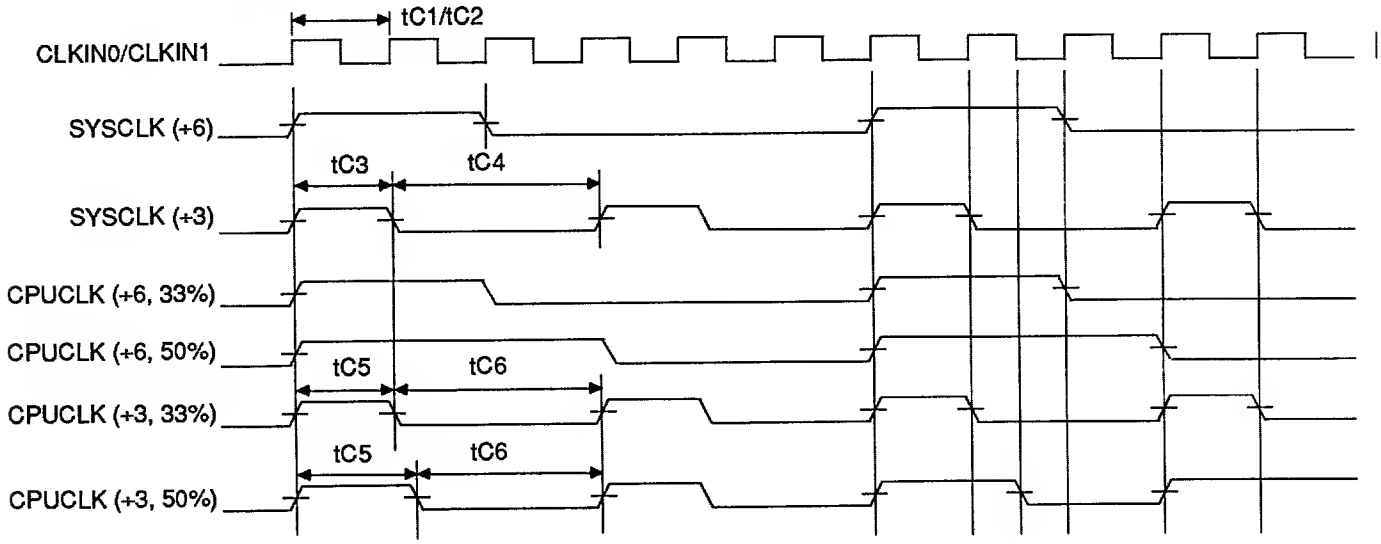
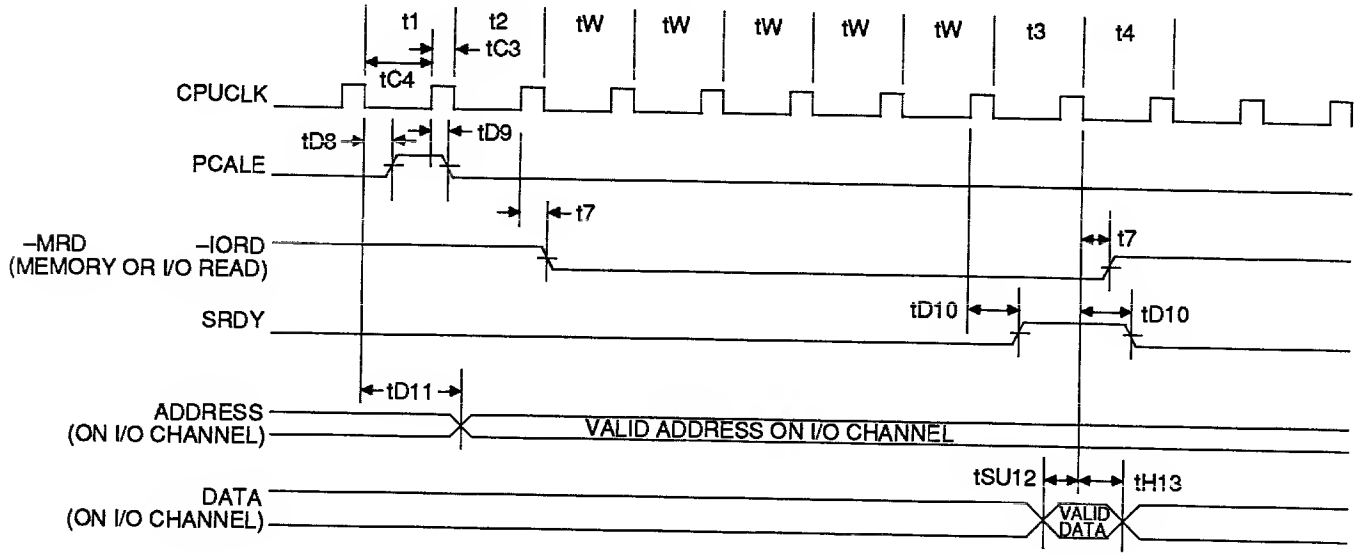


FIGURE 3. READ CYCLE TIMING DIAGRAM FOR I/O CHANNEL



5

FIGURE 3. WRITE CYCLE TIMING DIAGRAM FOR I/O CHANNEL

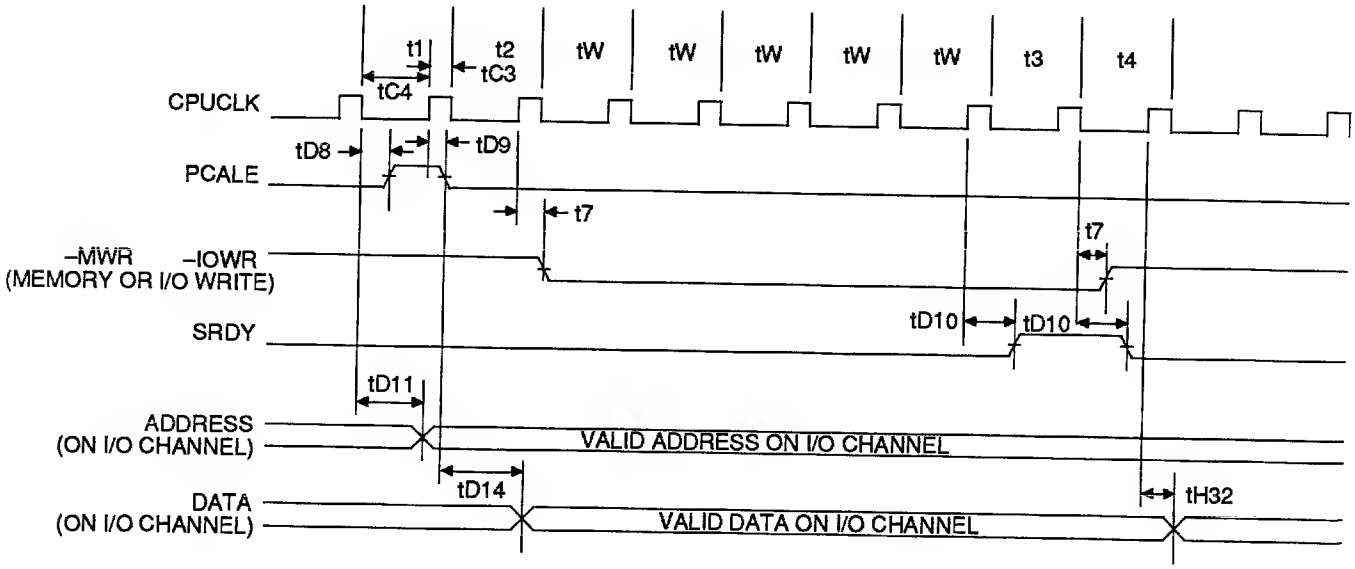


FIGURE 5. READ CYCLE TIMING DIAGRAM FOR ON-BOARD MEMORY (0 WAIT, 150 NS DRAM)

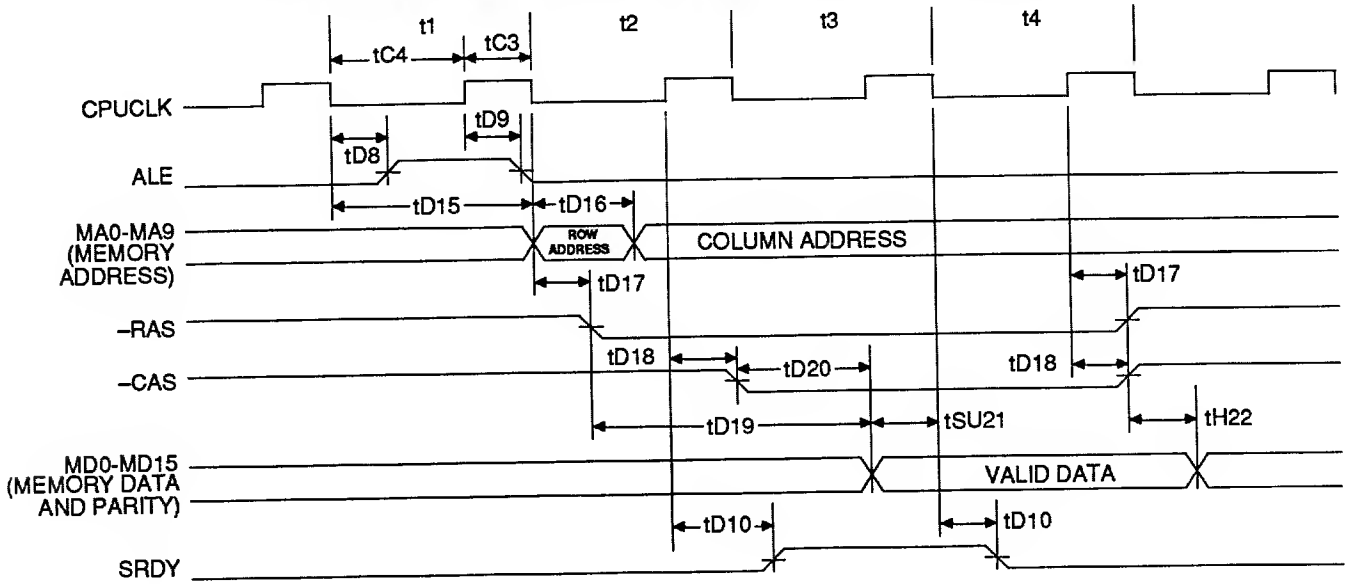


FIGURE 6. WRITE CYCLE TIMING DIAGRAM FOR ON-BOARD MEMORY (0 WAIT, 150 NS DRAM)

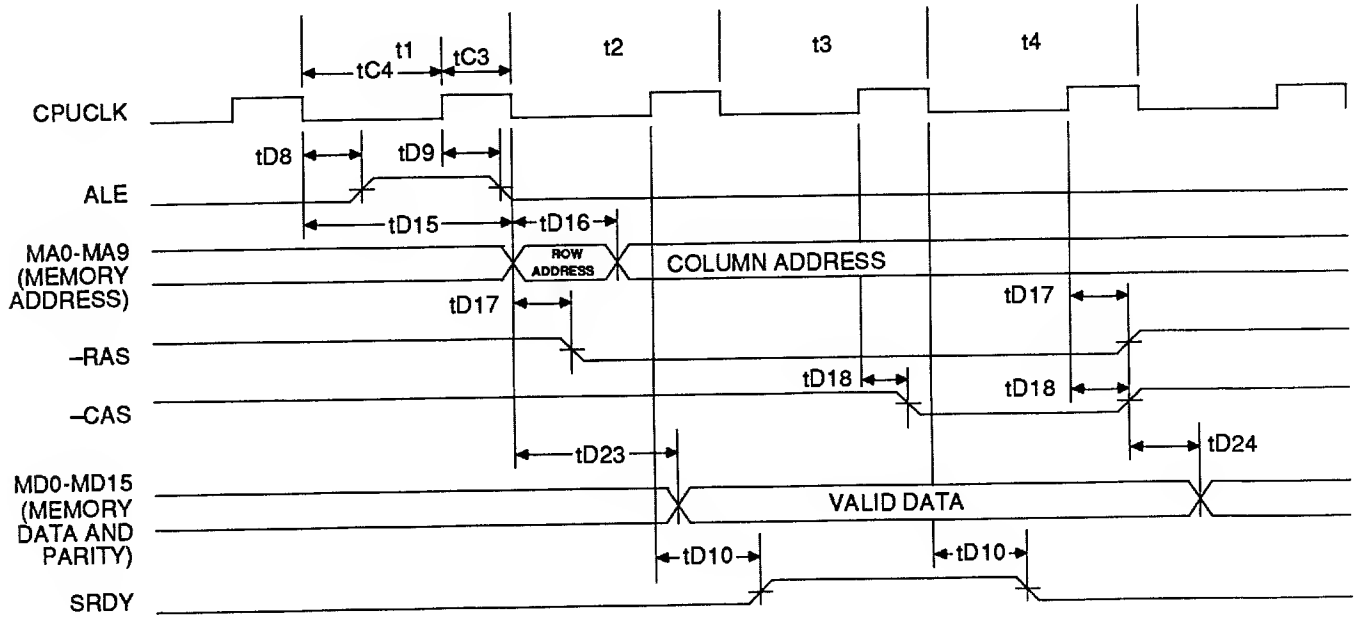
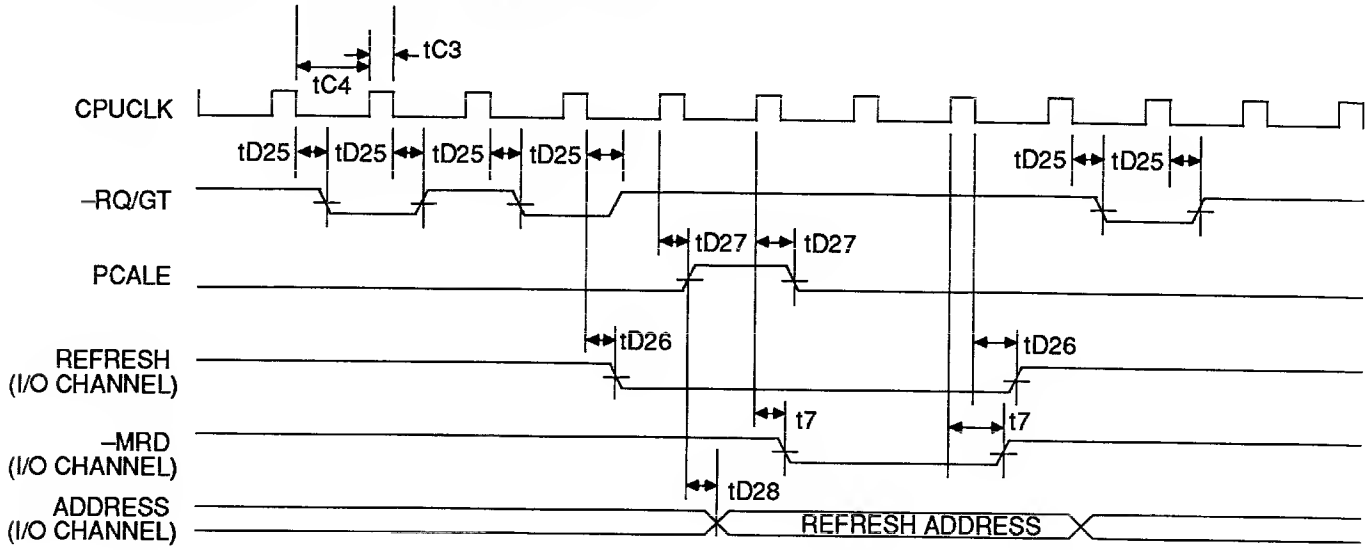
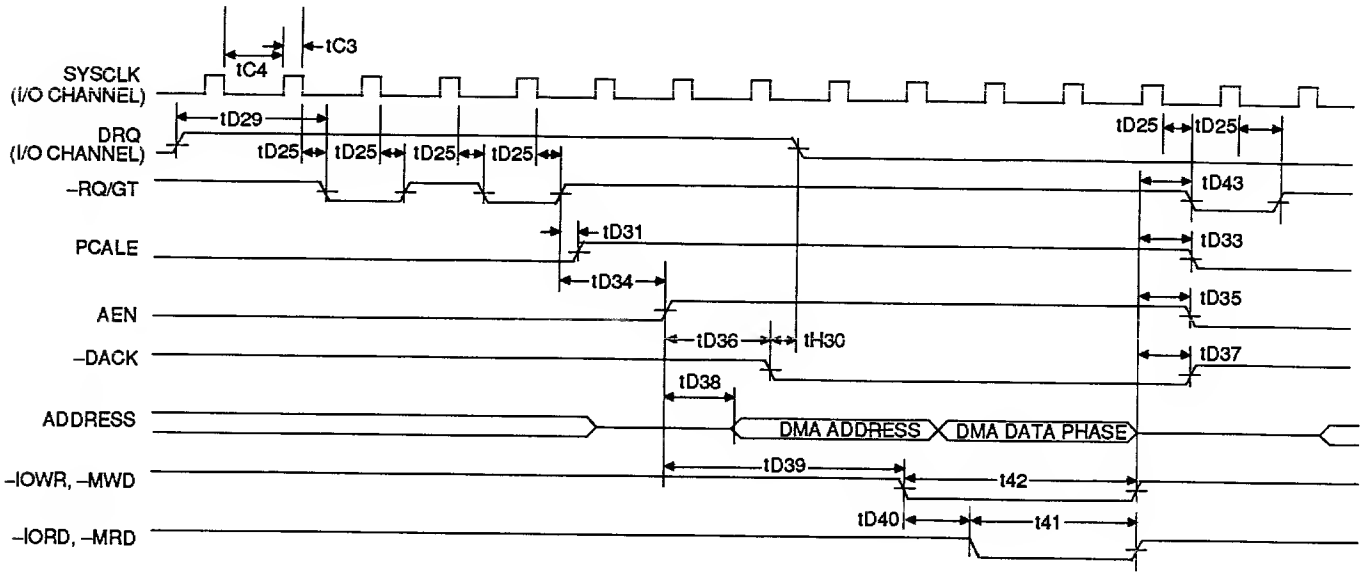


FIGURE 7. MEMORY REFRESH CYCLE TIMING DIAGRAM



5

FIGURE 8. DMA TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VCC +0.3 V
Applied Output Voltage	–0.5 V to VCC +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = 400 µA
VOL	Output Low Voltage		0.45	V	IOL = 20 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 12 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 8 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 4 mA, Note 1
VOL	Output Low Voltage		0.45	V	IOL = 2 mA, Note 1
VIH	Input High Voltage	2.0	VCC + 0.5	V	TTL
VIL	Input Low Voltage	–0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	–10	10	µA	
OLI	Output Leakage Current	–10	10	µA	
ICC	Operating Supply Current		250	mA	

Note 1: Output Current Driving Capabilities.

IOH	IOL	VL82C031 Pins
–3.3 mA	20 mA	RESET,–DACK1, –DACK3, AEN, –MREF
–1 mA	8 mA	PAR0, PAR1
–200 µA	4 mA	CPUCLK, SYSCLK, MDIR, –ERAS3 - –ERAS0, –RAS1, –RAS0, –CASH, –CASL, MA1-MA10, SAD0-SAD19, A0, ALE, –DACK0/–MRAS, –MWR, –MRD, –IOWR, –IORD, RAM256/1M, –ROMCS
–200 µA	2 mA	–INTA, SEL0, SEL1, –CMDEN, NMI, SRDY, –RQ/GT0, –RQ/GT1, –BHE, PCALE, –PCENH, –PCENL, PCDIR, TC, –DACKE

VLSI TECHNOLOGY, INC.

VL82C032

IBM PS/2® MODEL 30-COMPATIBLE I/O CONTROLLER

FEATURES

- Controls Model 30-compatible system keyboard and mouse
- Integrates the following functions on a single device:
  - –8253-compatible timer/counter
  - –Dual 8250-compatible serial communications controller
  - –Bidirectional parallel port controller
  - –8259-compatible interrupt controller
  - –58167-compatible real-time clock
- Decodes subsystems for floppy disk, hard disk, and video
- Provides chip select logic for serial/parallel ports, disk controllers, and real time clock.

DESCRIPTION

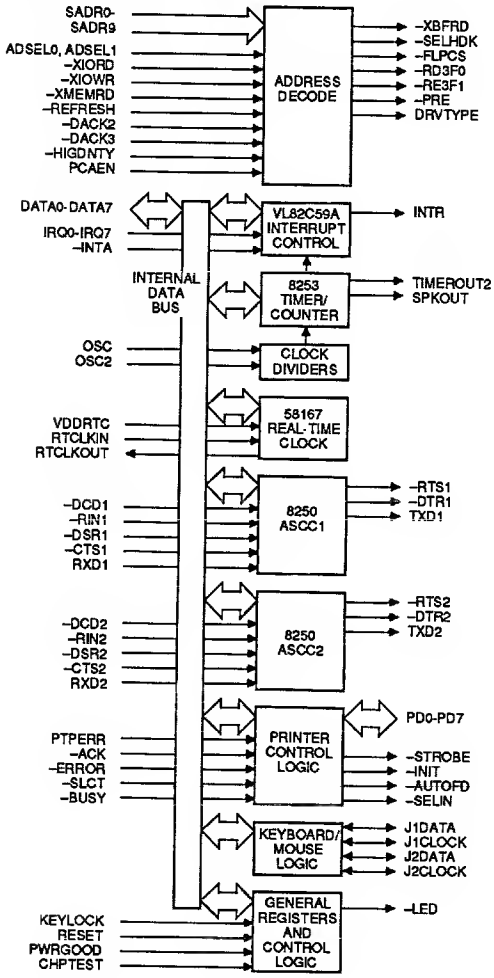
The VL82C032 provides the PS/2 Model 30-compatible system with control of both the keyboard and the pointing device ("mouse"), control of two serial communication channels, a real-time clock, as well as controlling both the disk storage and display functions. it also provides the chip select logic for the functions it controls. The VL82C032 is available from VLSI Technology, Inc. in an industry-standard plastic 100-pin flatpack.

The CMOS VL82C032 is the input/Output Controller device in the two-chip VLSI PS/2 Model 30-compatible chip set. The other device is the VL82C031 System Controller.

The chip set integrates logic and functions on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half, when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30 system, the VLSI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M-bytes of memory using EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

A third device, the VL82C037 VGA, Video Graphics Controller, is also used in the PS/2 Model 30-compatible system and provides high resolution graphics of up to 800 x 600 elements with 16 colors. Graphic capabilities of this resoiution are usually found only on more expensive systems.

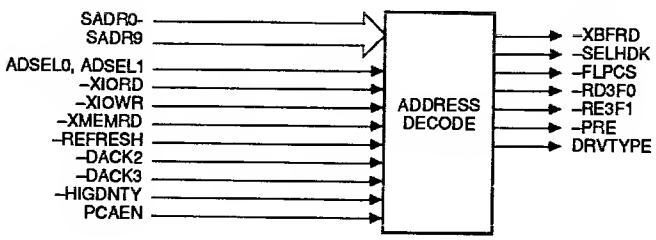
BLOCK DIAGRAM



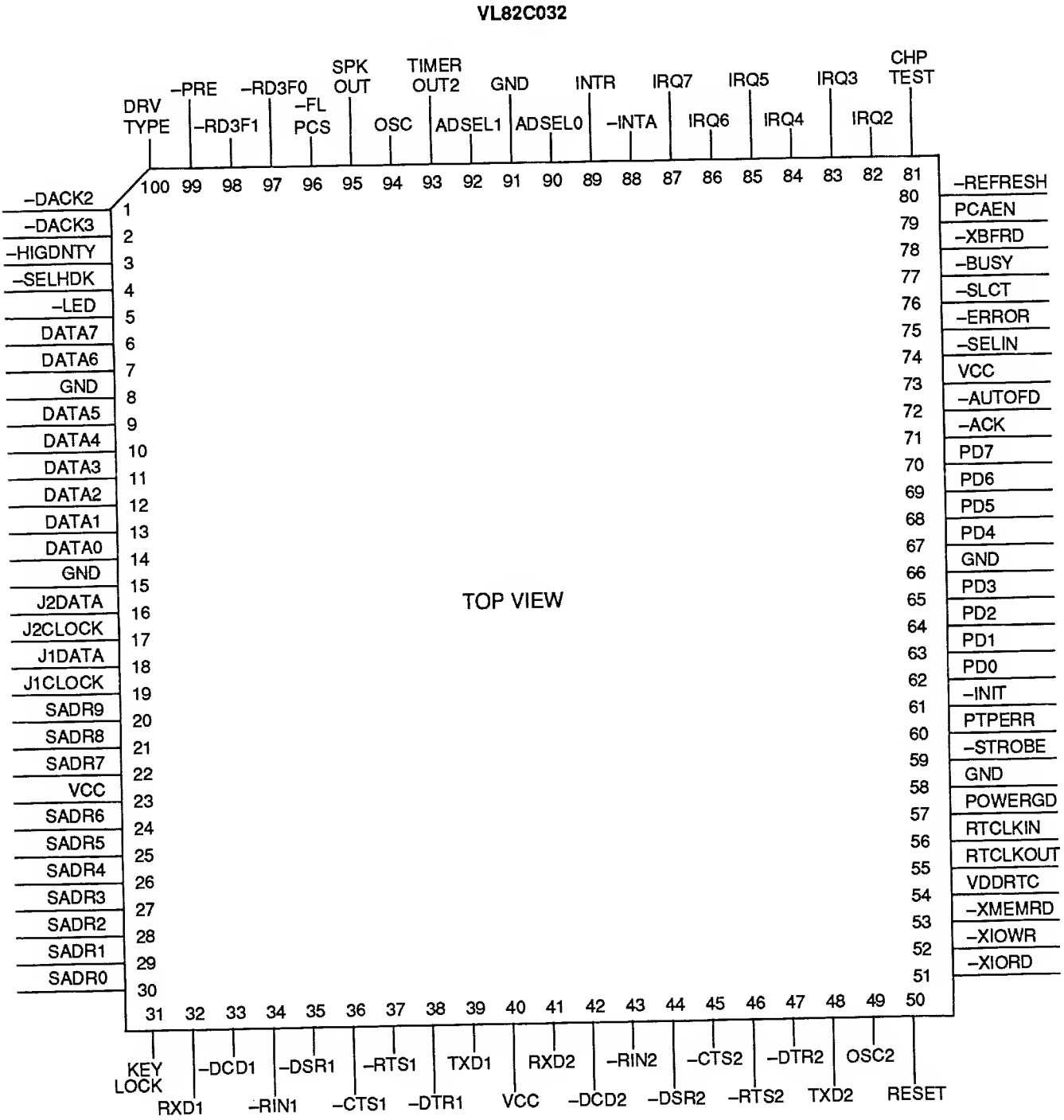
ORDER INFORMATION

Part Number	Package
VL82C032-FC	Plastic Flatpack

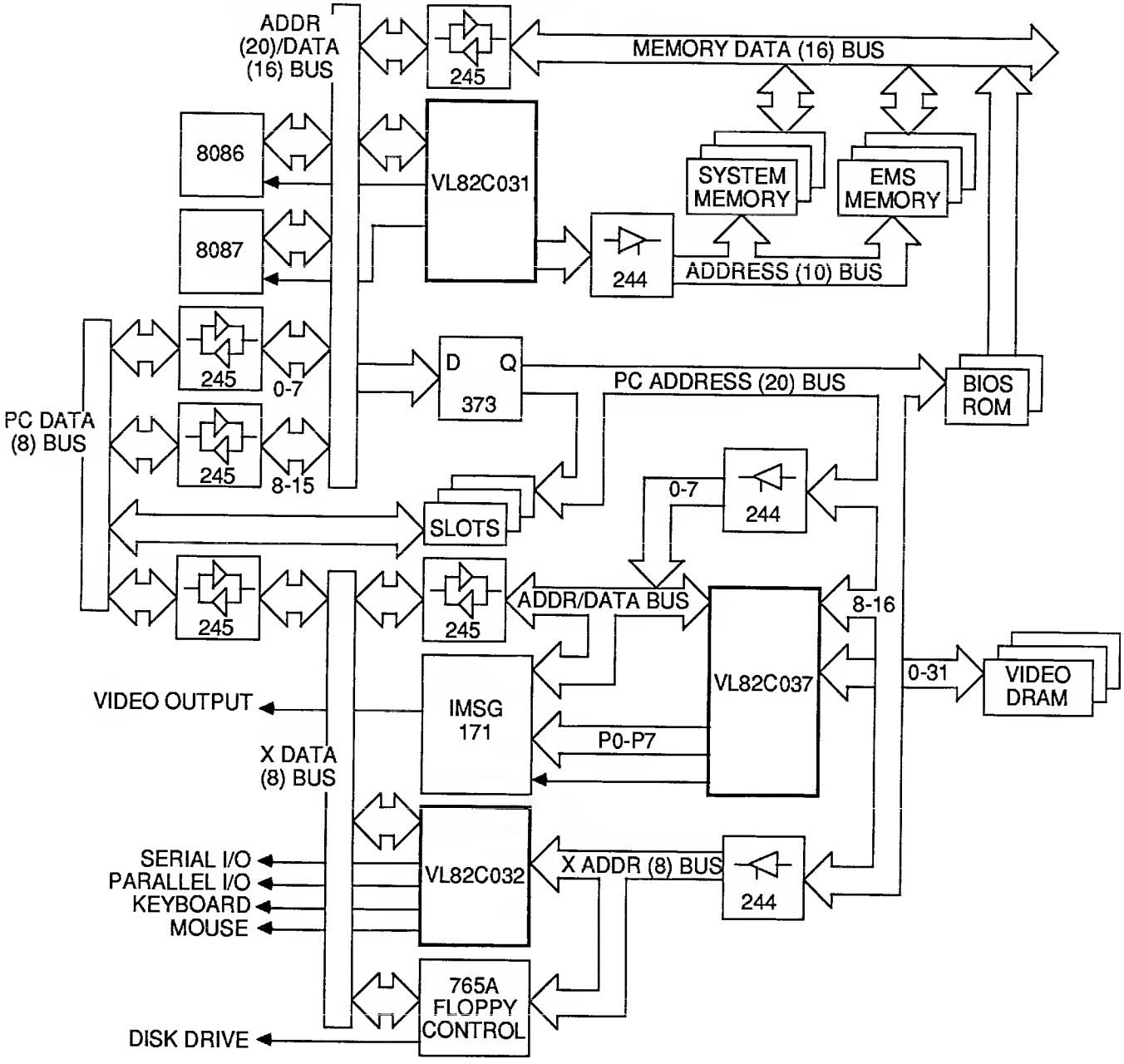
Notes: Operating temperature range is 0°C to +70°C.
IBM PS/2® is a registered trademark of IBM Corp.



PIN DIAGRAM


VL82C032
TOP VIEW
100 DRV TYPE
99 –PRE
98 –RD3F1
97 –RD3F0
96 –FL PCS
95 SPK OUT
94 OSC
93 TIMER OUT2
92 ADSEL1
91 GND
90 ADSEL0
89 INTR
88 –INTA
87 IRQ7
86 IRQ6
85 IRQ5
84 IRQ4
83 IRQ3
82 IRQ2
81 CHP TEST
1 –DACK2
2 –DACK3
3 –HIGDNTY
4 –SELHDK
5 –LED
6 DATA7
7 DATA6
8 GND
9 DATA5
10 DATA4
11 DATA3
12 DATA2
13 DATA1
14 DATA0
15 GND
16 J2DATA
17 J2CLOCK
18 J1DATA
19 J1CLOCK
20 SADR9
21 SADR8
22 SADR7
23 VCC
24 SADR6
25 SADR5
26 SADR4
27 SADR3
28 SADR2
29 SADR1
30 SADR0
31 KEY LOCK
32 RXD1
33 –DCD1
34 –RIN1
35 –DSR1
36 –CTS1
37 –RTS1
38 –DTR1
39 TXD1
40 VCC
41 RXD2
42 –DCD2
43 –RIN2
44 –DSR2
45 –CTS2
46 –RTS2
47 –DTR2
48 TXD2
49 OSC2
50 RESET
51 –XIORD
52 –XIOWR
53 –XMEMRD
54 VDDRTC
55 RTCLKOUT
56 RTCLKIN
57 POWERGD
58 GND
59 –STROBE
60 PTPERR
61 –INIT
62 PD0
63 PD1
64 PD2
65 PD3
66 GND
67 PD4
68 PD5
69 PD6
70 PD7
71 –ACK
72 –AUTOFD
73 VCC
74 –SELIN
75 –ERROR
76 –SLCT
77 –BUSY
78 –XBFRD
79 PCAEN
80 –REFRESH

PS/2 MODEL 30-COMPATIBLE SYSTEM DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–DACK2	1	I	DMA Acknowledge 2 - Used to notify the floppy controller that it has been granted a DMA cycle.
–DACK3	2	I	DMA Acknowledge 3 - Used to notify the on-board hard disk controller that it has been granted a DMA cycle.
–HIGDNTY	3	I	High Density - An active low signal that a high density floppy is being used.
–SELHDK	4	O	Hard Disk Select - Used to select on-board hard disk drive.
–LED	5	O	LED Output - Turns on an LED and is programmable through I/O Port D7h Bit 0.
DATA7-DATA0	6, 7 9-14	I/O	Data Bus - Bidirectional data lines to/from the CPU or I/O channel.
J2DATA	16	I/O	J2 Connector Data - A bidirectional data line for either a keyboard interface or pointing device.
J2CLOCK	17	I/O	J2 Connector Clock - A bidirectional clock for either a keyboard interface or pointing device.
J1DATA	18	I/O	J1 Connector Data - A bidirectional data line for either a keyboard interface or pointing device.
J1CLOCK	19	I/O	J1 Connector Clock - A bidirectional clock for either a keyboard interface or pointing device.
SADR9-SADR0	20-22 24-30	I	Address Bus - From I/O channel. This determines which I/O device the CPU is accessing.
KEYLOCK	31	I	Key Lock - Indicates whether the keyswitch has been locked or not. The state of this input can be read at Port 66h Bit 3.
RXD1	32	I	Receive Data 1 - Input pin for serial data to UART1.
–DCD1, –DCD2	33, 42	I	Carrier Detect - Notifies UART1 or UART2 that a carrier signal has been detected.
–RIN1, –RIN2	34, 43	I	Ring Indicator - Notifies UART1 or UART2 that a telephone ringing signal has been detected by a modem or data set.
–DSR1, –DSR2	35, 44	I	Data Set Ready - Handshake signal for UART1 and UART2, that the modem or data set is ready to transfer data.
–CTS1, –CTS2	36, 45	I	Clear To send - Handshake signal which notifies a modem or data set that UART1 or UART2 is ready to receive data.
–RTS1, –RTS2	37, 46	O	Request To Send - Handshake signal which notifies a modem or data set that UART1 or UART2 is ready to transmit data.
–DTR1, –DTR2	38, 47	O	Data Terminal Ready - Notifies a modem or data set that UART1 or UART2 is ready to transfer characters.
TXD1	39	O	Transmit Data 1 - Output pin for serial data from UART1.
RXD2	41	I	Receive Data 2 - Input pin for serial data to UART2.
TXD2	48	O	Transmit Data 2 - Output pin for serial data from UART2.
OSC2	49	I	Oscillator 2 - Is a 14.318 MHz TTL level clock input signal used to generate the clock for the 8253 internally.
RESET	50	I	Reset - An active high signal which is used to reset the internal logic of the VL82C032.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
-XIORD	51	I	I/O Read Command - Instructs the internal I/O device to drive its data on to the data bus.
-XIOWR	52	I	I/O Write Command - Instructs the internal I/O device to read the data present on the data bus.
-XMEMRD	53	I	Memory Read Command - Instructs the internal memory to drive its data on to the data bus.
VDDRTC	54	I	Real Time Clock Supply - Isolated power supply input for real time clock.
RTCLKOUT	55	O	Oscillator Output - 32.768 KHz real time clock output to crystal.
RTCLKIN	56	I	Oscillator Input - 32.768 KHz real time clock crystal or oscillator input.
PWRGOOD	57	I	Power Good - Indicates that power to the board is stable.
-STROBE	59	O	Printer Strobe - This pin is the "strobe" signal to a printer. Programmable through I/O Port 37Ah Bit 0.
PTPERR	60	I	Printer Paper End - Indicates that an end of paper has been detected. Readable at I/O Port 379h Bit 5.
-INIT	61	O	Printer Initialize - Initializes the printer. Programmable through I/O Port 37Ah Bit 2.
PD0-PD7	62-65 67-70	I/O	Parallel Port Data Bus - Bidirectional data lines to the parallel port device. When printer mode is selected, these lines are used as output lines. When input mode is selected, these lines are used as input lines.
-ACK	71	I	Printer Acknowledge - Indicates that data has been received by a printer. Readable at I/O Port 379h Bit 6.
-AUTOFD	72	O	Printer Auto Feed - Causes a printer to generate a line feed automatically after each line is printed. Programmable through I/O Port 37Ah Bit 1.
-SELIN	74	O	Printer Select In - Used to select the printer. Programmable through I/O Port 37Ah Bit 3.
-ERROR	75	I	Printer Error - Indicates that a printer error has occurred. Readable at I/O Port 379h Bit 3.
-SLCT	76	I	Printer Select - Indicates that the printer has been selected. Readable at I/O Port 379h Bit 4.
-BUSY	77	I	Printer Busy - This pin indicates whether the printer is able to receive data. Readable at I/O Port 379h Bit 7.
-XBFRD	78	O	Buffer Read - Controls the direction of an external data buffer. When this signal is low, data is read from the internal bus to the I/O channel. When this signal is high, data is written from the I/O channel to the internal bus.
PCAEN	79	I	Address Enable - Disables I/O devices from the I/O channel to allow DMA transfers to take place.
-REFRESH	80	I	Memory Refresh Request - Indicates that the system is in a memory refresh cycle.
CHPTEST	81	I	Chip Test Mode - When this signal is high, the VL82C032 is in a test mode. During normal operation, this pin should be tied to ground.
IRQ2-IRQ7	82-87	I	Interrupt Request Inputs - Asynchronous inputs which are the interrupt request signals to the internal 8259 interrupt controller.
-INTA	88	I	Interrupt Acknowledge - Enables the internal 8259 controller to vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
INTR	89	O	Interrupt Request - Interrupts the CPU. Generated whenever a valid IRQ is received.
ADSEL0, ADSEL1	90, 92	I	Address Select - Address range signals from the VL82C031, according to the following table:
TIMEROUT2	93	O	Timer Channel 2 Output - Provides a precision timer tick to the VL82C031.
OSC	94	I	OSC Input - A 24 MHz clock input.
SPKOUT	95	O	Speaker Data Output - Should be connected to a speaker driver to drive the speaker or beeper.
–FLPCS	96	O	Floppy Select - Chip select for a 765A floppy controller.
–RD3F0	97	O	Read Port A - A gate signal activated by a read from I/O Port 3F0h.
–RD3F1	98	O	Read Port B - A gate signal activated by a read from I/O Port 3F1h.
–PRE	99	O	Precomp - Used to select whether write precompensation is enabled in the 765A floppy controller. Programmable through I/O Port 3F7h Bit 2.
DRVTYPE	100	O	Drive Type - Used to control the data rate for the floppy controller (765A).
GND	8, 15, 58, 66, 91	I	System Ground
VCC	23, 40, 73	I	System Power: +5 V

ADSEL1	ADSEL0	Range
0	0	Don't Care
0	1	A15-A10 = 0 (I/O)
1	0	ROM
1	1	Video RAM

FUNCTIONAL DESCRIPTION

SYSTEM MEMORY AND I/O MAP

The 8086/V30 supports 16-bit operations with 20-bit addressing to directly access up to 1M byte of memory space. The system memory and an on-board expanded memory (if it's enabled) are byte and/or word accessible. Memory is mapped as follows:

Hex Address	Description	
00000 - 1FFFF	128K byte: 1st bank #1	640K System Memory
20000 - 2FFFF	64K byte: 2nd bank #2	
30000 - 3FFFF	64K byte: 2nd bank #3	
40000 - 4FFFF	64K byte: 2nd bank #4	
50000 - 5FFFF	64K byte: 2nd bank #5	
60000 - 6FFFF	64K byte: 2nd bank #6	
70000 - 7FFFF	64K byte: 2nd bank #7	
80000 - 8FFFF	64K byte: 2nd bank #8	
90000 - 9FFFF	64K byte: 2nd bank #9	
A0000 - BFFFF	64K byte: Video Buffer	
C0000 - EFFFF	192K byte: Reserved for BIOS on I/O Channel.	
F0000 - FFFFF	64K byte: System ROM	

VL82C032 I/O MAP

I/O Address	Function	Response	PC Bus Response
0020 - 0021	Interrupt Control	R/W	None
0040 -0043	System Timer	R/W	None
0060	System Data Port	R/W	None
0061	System Control	R/W	None
0062	System Status Register	R/W	None
0063	Interrupt Control	R/W	None
0065	Chip Select Control	R/W	None
0066 - 006A	Interrupt Diagnostic	R/W	None
00A0 - 00AF	Interrupt Extended Status	R/W	None
00B0 - 00BF	Real Time Clock	R/W	None
00D0 - 00DF	System Control and Status Group 2	R/W	None
00E0 - 00EF	Real Time Clock	R/W	None
02F8-02FF	Serial Comm. Control 2	R/W	None
0320 - 032F	Fixed Disk Control	R/W*	R/W
0378 - 037A	Parallel Port	R/W	None
03F0 - 03F7	Floppy Disk Control	R/W*	R/W
03F8 - 03FF	Serial Comm. Control 1	R/W	None

*Note: The peripheral is external to the VL82C032. It can be enabled or disabled through the Chip Select Control Register Port.

5

TABLE 1. INTERRUPT REQUEST LEVEL REGISTER

Level	VL82C032 Chip	System Board	I/O Channel
IRQ0	Timer Channel 0	Not Available	Not Available
IRQ1	Keyboard Interface Pointing Device and Real Time Clock	Not Available	Not Available
IRQ2	Not Used	Video (VL82C037)	Available
IRQ3	Serial Port 2	Not Used	Available
IRQ4	Serial Port 1	Not Used	Available
IRQ5	Not Used	Fixed Disk	Available
IRQ6	Not Used	765A Floppy Controller	Available
IRQ7	Parallel Port	Not Used	Available

TABLE 2. MODE FUNCTIONS

Address	W/R	Functions
		*** Initialization Mode***
0020	W	Initialization Command Word ICW1
0021	W	Initialization Command Word ICW2, ICW2, ICW3, ICW4
		*** Operation Mode ***
0021	W	Operation Control Word OCW1
0020	W	Operation Control Word OCW2, OCW3
		*** Read Status Register (Operation Mode) ***
0021	R	Interrupt Mask Register (IMR)
0020	R	Interrupt Request Register (IRR) and Interrupt Service Register (ISR), IRR and ISR is selected through b0 and b1 in OCW3

INTERRUPT CONTROL LOGIC

The interrupt control logic includes one Intel 8259A-compatible interrupt controller, one interrupt vector register and two interrupt extension registers.

The interrupt controller has eight levels of interrupt that are handled according to priority in the VL82C032 chip. Table 1 shows the hardware interrupts and their availability to the I/O channel (PC bus).

The I/O address for each register in the interrupt controller is defined in Table 2.

During initialization mode, when the vector address is written into ICW2 register, the same vector address will be written into the interrupt vector register. The content of interrupt vector register can be read through an I/O read from address 063h. In order to read this register, I/O Port 69h Bit 6 must be set to 1. By writing to I/O Port 63h any of the IRQ lines can be activated or the NMI line as shown in the following table:

I/O Port 63h (Write)

Bit	Function
7	IRQ7
6	IRQ6
5	IRQ5
4	IRQ4
3	IRQ3
2	IRQ2
1	Not Used
0	NMI

To write this port I/O Port 69h Bit 7 must first be set to 1. You must set Port 69h Bit 2 to 1 to allow NMI activation. To start the initialization mode of the interrupt controller, a command is issued with Bit 4 =1 to I/O address 020h which it is interpreted as ICW1. The content of the interrupt vector register is reset to 0 after power-up reset.

Regardless of the vector address initialized in ICW2, the vector address generated by interrupt IRQ1 is always hex 71. The interrupt acknowledge cycle only requires one wait state for 8 MHz or 10 MHz CPU 8086.

For detailed instructions on how to program the 8259A-compatible interrupt controller, see the VL82C59A data sheet.

TIMER CONTROLLER

This timer controller is compatible with the Intel 8253. It is a programmable interval timer/counter. The functions of the timer controller are to generate a constant system time and control the tone of the speaker. This controller contains three timer channels. Each channel is described as follows:

Channel 0:
This channel is a general purpose timer providing a constant time base for operating system. The input clock runs at 1.19 MHz. The enable clock input is always enabled after power-up. The output of this channel is connected to interrupt channel 0 (IRQ0) of the interrupt controller (8259A).

Channel 1:
This channel is for diagnostic purposes. During power-up test, the system BIOS will use this channel to check the functions of the timer controller. The system BIOS also uses this channel to check the frequency of memory refresh. The input clock runs at 15.6 µs per cycle. The enable clock input is always enabled after power-up. The output of this channel is not connected anywhere, so CLKOUT1 is not an available pin on the VL82C032.

Channel 2:
This channel is used to control the tone of the speaker. The input clock runs at 1.19 MHz frequency. The enable clock input is turned on or off by bit 0 of system control register 061h. When bit 0 of I/O PORT 061h is set to 1, the frequency of the tone is controlled by the number in counter register 2. The output of this channel is connected to the speaker driver. After power-up reset, bit 0 of I/O port 061h is reset to 0. More detailed information is available in the system control register section (061h).

The I/O address for each register in the timer controller is defined in Table 3.

The control mode register is to select the operation mode for each channel in the timer controller. There are six

TABLE 3. REGISTERS

Address	W/R	Functions
0040	W/R	Counter Register 0
0041	W/R	Counter Register 1
0042	W/R	Counter Register 2
0043	W	Control Mode Register

different modes that can be selected. They are listed as follows:

- mode 0: interrupt on terminal count
- mode 1: programmable one-shot
- mode 2: rate generator
- mode 3: square wave rate generator
- mode 4: software triggered strobe
- mode 5: hardware triggered strobe

REAL TIME CLOCK

A real time clock is integrated in the VL82C032 chip. Its functions are fully compatible with the National 58167A real time clock. However, the VL82C032 is much faster than the 58167A. It can complete a read or write cycle at normal I/O speed (four wait states) in a System 30, so it is not necessary to generate the IOCHRDY to the I/O Channel. The functional block has an independent power (VDDRTC) pin which is isolated from the normal power (VCC) pin of the VL82C032 chip.

This real time clock includes an addressable counter, eight bytes of RAM, and two interrupt outputs. A power-down input allows the real time clock to be powered from battery power and continue its operation independently during power-down mode. The time base is derived from a 32,768 Hz crystal oscillator.

The PWRGOOD input will block the chip select signal and I/O read or write signals during power-up or hardware reset. It prevents any non-valid I/O access to the real time clock.

The I/O address for each register and RAM in the real time clock is defined in Table 4.

The interrupt from the real time clock is connected to IRQ1 of the interrupt controller. IRQ1 is also shared with the keyboard and pointing device interface. The interrupt from the real time clock can be reset by reading the interrupt status register (I/O Port B0 hex).

An auto reset will be generated in the internal logic of the real time clock when VCC switches from 0.0 V to operating voltage. This reset signal will reset the content of RAM and the content of the interrupt registers to 0.

CMOS SRAM

There are 16 bytes of CMOS static RAM in the VL82C032, powered by the standby battery. This can be used for storing system configuration information.

The RAM can be accessed by writing an index value (0-F) to I/O Port D4h and then writing or reading I/O Port D5h.

The PWRGOOD input will block the chip select signal and I/O read or write signals during power-up or hardware reset. It prevents any non valid I/O access to the RAM.

An auto reset will be generated when VCC switches from 0.0 V to 2.0 V, which will reset the content of the SRAM to 0.

SERIAL CONTROLLER

The VL82C032 chip incorporates two serial communication controllers which are fully compatible with the NS8250A. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. These controllers support 5-, 6-, 7- and 8-bit characters with 1, 1.5 or 2 stop bits. A prioritized interrupt system controls transmit, receive, error, and line status as well as data-set interrupt. The clock applied to the serial controller is 1.84 MHz which is derived from the system clock.

Each serial port will provide the following RS232 signals:

- RXD: Receive Data
- CTS: Clear To Send
- DSR: Data Set Ready
- DCD: Data Carry Detect
- RI: Ring Indicator
- TXD: Transmit Data
- DTR: Data Terminal Ready
- RTS: Request To Send

The interrupt from serial controller 1 is connected to IRQ4 of the interrupt controller in the VL82C032. The I/O address for each register in serial controller 1 is defined in Table 5.

The interrupt from serial controller 2 is connected to IRQ3 of the interrupt controller in the VL82C032. The I/O address for each register in serial controller 2 is defined in Table 6.

5

TABLE 4. W/R FUNCTIONS

Address	W/R	Functions
00B0	R	Interrupt Status Register
00B1	W	Interrupt Control Register
00B2	W	Counters Reset (Data = FFH)
00B3	W	RAM Reset (Data = FFH)
00B4	R	Status Bit, d0 = 1, Counter Is Rippling The content of counters are invalid; reread.
00B5	W	Go Command (Data = XXH)
00B6	W	Standby Interrupt (1 = Enable, 0 = Disable)
00BF	W	Enable Test Mode
00E0	W/R	Counter - Ten Thousandths of Seconds
00E1	W/R	Counter - Hundredths and Tenths of Seconds
00E2	W/R	Counter - Seconds
00E3	W/R	Counter - Minutes
00E4	W/R	Counter - Hours
00E5	W/R	Counter - Day of Week
00E6	W/R	Counter - Day of Month
00E7	W/R	Counter - Month
00E8	W/R	RAM - Ten Thousandths of Seconds
00E9	W/R	RAM - Hundredths and Tenths of Seconds
00EA	W/R	RAM - Seconds
00EB	W/R	RAM - Minutes
00EC	W/R	RAM - Hours
00ED	W/R	RAM - Day of Week
00EE	W/R	RAM - Day of Month
00EF	W/R	RAM - Month

PARALLEL PORT CONTROLLER

The parallel port controller can be configured to be one of two modes. The first is "printer mode". The second is "input mode," which allows the parallel port to receive data from external devices. The input mode of the parallel port controller is selected by writing a 0 to bit 7 of the peripheral select control register 065h.

There are two output ports and three input ports in the parallel port controller. The following is a detailed description of each port.

Data Port: 378h

The data port is an 8-bit port for both the printer mode and input mode. For the printer mode, a write operation to this port immediately presents data to the connector pins. A read operation from this port in the printer port produces the data that was last written to it.

In the input mode, a write operation to this port will not affect the output of the data port. A read operation in the input mode produces the current data on the connector pins from external devices.

Status Port: 379h

The status port is a read-only port for either mode. When an interrupt is pending the interrupt status bit is set to 0. The following is the bit definition of the status port:

Bit Function

7 –BUSY: When this bit is 0, the printer is busy and cannot accept data.

6 –ACK: When this bit is 0, the printer is ready to accept data.

5 PE: When this bit is 1, the printer has detected the end of the paper.

4 SLCT: When this bit is 1, the printer has been selected.

3 –ERROR: When this bit is 0, the printer has detected an error condition.

2 –IRQ: When this bit is 0, the printer has acknowledged the previous transfer using the "–ACK" signal.

Output Control Port: 37Ah

The Output Control Port is a read or write port. The following shows the bit definition of the Output Control Port:

Bit Function

4 IRQEN: When this bit is set to 1, the interrupt logic is enabled.

3 SLCTIN: This bit controls the –SELIN signal on the VL82C032 pin 74. When this bit is set to 1, the printer is selected.

2 –INIT: This bit controls the "–INIT" signal on the VL82C032 pin 61. When this bit is set to 1, the printer starts.

1 AUTOFD: This bit controls the "–AUTOFD" signal on the VL82C032 pin 72. When this bit is set to 1, the printer will automatically line feed after each line is printed.

0 STROBE: This bit controls the "–STROBE" signal on the VL82C032 pin 59. When this bit is set to 1, data is pulse-clocked into the printer.

The interrupt from the parallel port controller is connected to IRQ7 of the interrupt controller in the VL82C032. The I/O address for each register in the parallel port controller is defined in Table 7.

KEYBOARD INTERFACE AND POINTING DEVICE INTERFACE

There are two interfaces (J1 and J2) which can be used for either keyboard or pointing device. The keyboard interface is fully compatible with the enhanced AT keyboard, and is implemented as hardware logic instead of the 8042 microcontroller. The pointing device interface is also fully compatible with IBM PS/2 mouse devices. The system BIOS will handle the following tasks:

- initialization of the interface after power-up
- define which device (keyboard or pointing device) has been connected to each interface (J1 and J2)
- receive interrupt and parity errors
- translation between keyboard scan code and ASCII code
- transmission sequences

The hardware will handle the following tasks:

- initialize both interface registers to default value after power-up reset
- generate protocol sequences (data line and clock line) between system and keyboard or mouse
- detect incoming data (start bit) from keyboard or mouse
- generate the receive interrupt and check parity error
- generate the parity bit during transmission
- handle asynchronous conditions between transmit and receive

There are two signal lines used for each interface. They are the data line and the clock line. During a receive or transmit cycle, the clock will be generated by the keyboard or pointing device. The system only drives the clock line for

TABLE 5. SERIAL CONTROLLER 1 I/O ADDRESSES

Address	W/R	Functions
03F8	W	Transmitter Holding Register
03F8	R	Receive Buffer Register
03F9	W/R	Interrupt Enable Register
03FA	R	Interrupt Identification Register
03FB	W/R	Line Control Register
03FC	W/R	Modem Control Register
03FD	R	Line Status Register
03FE	R	Modem Status Register
03FF	W/R	Scratch Register

TABLE 6. SERIAL CONTROLLER 2 I/O ADDRESSES

Address	W/R	Functions
02F8	W	Transmitter Holding Register
02F8	R	Receive Buffer Register
02F9	W/R	Interrupt Enable Register
02FA	R	Interrupt Identification Register
02FB	W/R	Line Control Register
02FC	W/R	Modem Control Register
02FD	R	Line Status Register
02FE	R	Modem Status Register
02FF	W/R	Scratch Register

handshake purposes. The protocols of handshake between the system and keyboard or pointing devices are described in Table 8.

The definitions of each register for interface are described as follows.

KEYBOARD/POINTING DEVICE DATA REGISTER (060h) R/W

This register is for user interface (application) at the system BIOS level. It is a dummy register, and does not relate to the hardware logic on any particular interface. When information is to be transmited to the keyboard or pointing device, writing the data to this register and the system BIOS will take the content of this register and transmit it to the keyboard or pointing device. When either interface receives data from an external device (keyboard or pointing device), the system BIOS will check any parity error and copy the data from the receive register to this data register.

This register will be reset to 0 at power-up reset.

KEYBOARD/POINTING DEVICE TRANSMIT/RECEIVE REGISTERS (067h AND 068h)

Register 067h is the transmit/receive register for interface J1. Register 068h is the transmit/receive register for interface J2. These are eight-bit registers. Reading these registers will not affect any logic state on the interfaces. These registers can be read at any time, and will return the data from the receive buffers for their respective interfaces.

When writing to these registers, the data will be stored in the transmit buffers and generate a parity bit. Writing the data to these registers will not start the transmit sequence. To start the transmit sequence on interface J1, bit 3 of the transmit control register (069h) must be toggled (0->1->0) before writing the data to the transmit register (067h). To start the transmit sequence on interface J2, bit 4 of the transmit control register (069h) must be toggled (0->1->0) before writing the data to the transmit register (068h). The purpose of toggling bit 3 or bit 4 of the transmit control register is to ensure the clock line on the interface (J1 or J2) is in a quiescent state.

The receive buffers and transmit buffers will be reset to 0 after power-up reset.

Bit 3 of this register is for initializing the transmission logic for interface J1. Bit 4 of this register is for initializing the transmission logic for interface J2. These two bits ensure the clock lines are in the quiescent state. If the external device (keyboard or pointing device) is sending data to the system before transmission starts, the transmit sequence will not be started until bit 4 or bit 6 of the receive control register (066h) is toggled (0->1->0). When either interface receives data from an external device the hardware logic will pull the clock line low to prevent contiguous data transmission by the external device. Toggling bit 4 of the receive control register (066h) will cause the clock line on interface J1 to become quiescent. Toggling bit 6 of the receive control register (066h) will cause the clock line on interface J2 to become quiescent. If the clock line is kept low for any reason, the transmit cycle should not be started until the clock line becomes quiescent.

The bit definitions of the transmit control register are shown in Table 9.

Toggling bit 3 or bit 4 of the transmit control register will reset any parity error indication (bit 0 or bit 1 of the receive control register - 066h).

Bit 7, bit 6 and bit 2 of the transmit control register are for interrupt/NMI diagnostics. These bits are described in the section covering the interrupt controller.

Reading this register will not affect the hardware logic. These bits will be reset to 0 after power-up reset.

KEYBOARD/POINTING DEVICE RECEIVE CONTROL REGISTER (066h)

This register controls the receive logic for both interfaces. This register also indicates which interface (J2 or J2) has been connected to the keyboard, and if any parity error has occurred during a receive cycle. The bits are defined in Table 10.

When bit 5 is set to 0, the clock line on interface J1 will be forced to 0. When bit 7 is set to 0, the clock line on

5

TABLE 7. OUTPUT AND PRINTER REGISTER

Address	W/R	Functions
0378	W/R	Data Output Register
0379	R	Printer Status Register b7 = Printer Busy (1 = Not Busy, 0 = Busy) b6 = Printer Acknowledge (1 = No –ACK, 0 = –ACK) b5 = End of Paper (1 = No Paper, 0 = Paper ok) b4 = Printer Selected (1 = Selected, 0 = Not Selected) b3 = Printer Error (1 = No –ERROR, 0 = –ERROR) b2 - b0 = Not Used
037A	W/R	Printer Control Register b7 - b5 = Not Used b4 = Enable/Disable Interrupt (1 = Enable, 0 = Disable) b3 = Select Printer Device (1 = Select, 0 = Not Select) b2 = Start Printer Device (1 = Stop, 0 = Start) b1 = Enable Line Feed (1 = Enable, 0 = Disable) b0 = Data Strobe (1 = Data Valid, 0 = Data Invalid)

TABLE 8. TRANSMIT DECODE

Clock Line	Data Line	Functions
0	X	No Transmit or Receive
1	0	System Transmit Data to Keyboard or Mouse
1	1	Keyboard or Mouse Transmit Data to System

interface J2 will be forced to 0. At power-up reset, these two bits are reset to 0. External devices cannot send any data to the system until these two bits are set to 1.

When bit 4 is set to 1, it clears the indication of parity errors and interrupts on interface J1. When bit 6 is set to 1, it clears the indication of parity errors and interrupts on interface J2. When these two bits are 1, the clock line will not be forced low after receiving data from an external device. Normally, these two bits should be set to 0. After receiving data from an external device, bit 4 or bit 6 should be toggled to clear any parity error or interrupt. These bits will be reset to 0 on power-up reset.

Bit 3 indicates whether the keyboard has been connected to interface J1. The keyboard connection is not detected by the hardware logic on the the interface J1. It is done by the system BIOS, so the system BIOS should set or reset this bit. When this bit is set to 1, the keyboard is connected to interface J1. When this bit is 0, the keyboard is connected to interface J2. This bit will be reset to 0 at power-up reset.

Bit 0 and bit 1 indicate parity errors. When bit 0 is set to 1, it indicates a parity error occurred on interface J1 during a receive cycle. Bit 0 can be cleared by writing one to bit 4 of this register or bit 3 of the transmit control register (069h). Bit 1 can be cleared by writing 1 to bit 6 of this register or bit 4 of the transmit control register (069h). These two bits are reset to 0 at power-up reset.

Bit 2 indicates whether the system keyswitch has been locked or not. When this bit is 0, the system keyswitch is locked.

KEYBOARD/POINTING DEVICE RECEIVE STATUS REGISTER (06Ah)

Bit 5 and bit 2 of this register indicate whether data has been received from an external device or not for interface J1 and J2, respectively. When bit 5 is 1, data has been received from interface J1. Bit 5 can be cleared by setting bit 4 of the receive control register (066h) or bit 3 of the transmit control register (069h). When bit 2 is 1, data has been received from interface J2. Bit 2 can be cleared by setting bit 6 of the receive control register (066h) or bit 4 of the transmit control register (069h). After power-up reset, these bits are reset to 0.

The bits in this register are defined in Table 11.

Bit 0 indicates what type of floppy disk drive has been connected to the system. When this bit is set to 0, a high density drive (1.44M bytes) has been selected. When this bit is set to 1, a low density drive (720K bytes) has been selected. This bit reflects the state of the –HIGDNTY input (pin 3) of the VL82C032.

INTERRUPT EXTENDED CONTROL REGISTER (0A1h)

The purposes of this register is to mask out incoming interrupts from the keyboard, pointing device or real time clock. The bit definitions for this register are described in Table 12.

When bit 3 is set to 1, interrupts from interface J2 will be masked out. When bit 2 is set to 1, interrupts from interface J1 will be masked out. When bit 0 is set to 1, interrupts from the real time clock wil be masked out.

Setting the bits in register 0A1 will not affect the indications on bit 2 and bit 3 of the interrupt extended status register (0A0h) and bit 2 and bit 5 of the keyboard/pointing device receive status register (06Ah). These bits are reset to 0 at power-up reset.

INTERRUPT EXTENDED STATUS REGISTER (0A0h)

IRQ1 (hardware interrupt) of the interrupt controller is shared by three devices; real time clock, J1 interface and J2 interface. This register determines which device generated the IRQ1.

The bit functions of this register are described in Table 13.

When bit 3 is 1, it indicates a pending interrupt from interface J2 (keyboard or pointing device). Bit 3 can be reset by toggling bit 6 of register 066h or bit 4 of register 069h. When bit 2 is 1, it indicates a pending interrupt from interface J1 (keyboard or pointing device). Bit 2 can be reset by toggling bit 4 of register 066h or bit 3 of register 069h. When bit 0 is 1, it indicates a pending interrupt from the real time clock. Bit 0 can be reset by reading the interrupt status register (0B0h) on the

TABLE 9. TRANSMIT CONTROL REGISTER

Address	W/R	Functions
0069	W/R	b7 = Enable Diagnostic Through Reg. 63h b6 = Blocks Reg. 63h Read b5 = Disable J1 and J2 Clock (1 = Disable) b4 = Toggle for System to Transmit Data Through J2 b3 = Toggle for System to Transmit Data Through J1 b2 = Enable NMI Diagnostic Through Reg. 63h b2 = Enable NMI Diagnostic Through Reg. 63h b1 = Not Used b0 = Not Used

TABLE 10. RECEIVE CONTROL REGISTER

Address	W/R	Functions
0066	W/R	b7 = System Drives the Clock on J2
	W/R	b6 = Toggle for System to Receive Data Through J2
	W/R	b5 = System Drives the Clock on J1
	W/R	b4 = Toggle for System to Receive Data Through J1
	W/R	b3 = J1 Has Keyboard Connection
	R	b2 = Key lock (0 = Key Is Locked)
	R	b1 = J2 Parity Error Indication
	R	b0 = J1 Parity Error Indication

interface J2 will be forced to 0. At power-up reset, these two bits are reset to 0. External devices cannot send any data to the system until these two bits are set to 1.

When bit 4 is set to 1, it clears the indication of parity errors and interrupts on interface J1. When bit 6 is set to 1, it clears the indication of parity errors and interrupts on interface J2. When these two bits are 1, the clock line will not be forced low after receiving data from an external device. Normally, these two bits should be set to 0. After receiving data from an external device, bit 4 or bit 6 should be toggled to clear any parity error or interrupt. These bits will be reset to 0 on power-up reset.

Bit 3 indicates whether the keyboard has been connected to interface J1. The keyboard connection is not detected by the hardware logic on the the interface J1. It is done by the system BIOS, so the system BIOS should set or reset this bit. When this bit is set to 1, the keyboard is connected to interface J1. When this bit is 0, the keyboard is connected to interface J2. This bit will be reset to 0 at power-up reset.

Bit 0 and bit 1 indicate parity errors. When bit 0 is set to 1, it indicates a parity error occurred on interface J1 during a receive cycle. Bit 0 can be cleared by writing one to bit 4 of this register or bit 3 of the transmit control register (069h). Bit 1 can be cleared by writing 1 to bit 6 of this register or bit 4 of the transmit control register (069h). These two bits are reset to 0 at power-up reset.

Bit 2 indicates whether the system keyswitch has been locked or not. When this bit is 0, the system keyswitch is locked.

KEYBOARD/POINTING DEVICE RECEIVE STATUS REGISTER (06Ah)

Bit 5 and bit 2 of this register indicate whether data has been received from an external device or not for interface J1 and J2, respectively. When bit 5 is 1, data has been received from interface J1. Bit 5 can be cleared by setting bit 4 of the receive control register (066h) or bit 3 of the transmit control register (069h). When bit 2 is 1, data has been received from interface J2. Bit 2 can be cleared by setting bit 6 of the receive control register (066h) or bit 4 of the transmit control register (069h). After power-up reset, these bits are reset to 0.

The bits in this register are defined in Table 11.

Bit 0 indicates what type of floppy disk drive has been connected to the system. When this bit is set to 0, a high density drive (1.44M bytes) has been selected. When this bit is set to 1, a low density drive (720K bytes) has been selected. This bit reflects the state of the –HIGDNTY input (pin 3) of the VL82C032.

INTERRUPT EXTENDED CONTROL REGISTER (0A1h)

The purposes of this register is to mask out incoming interrupts from the keyboard, pointing device or real time clock. The bit definitions for this register are described in Table 12.

When bit 3 is set to 1, interrupts from interface J2 will be masked out. When bit 2 is set to 1, interrupts from interface J1 will be masked out. When bit 0 is set to 1, interrupts from the real time clock wil be masked out.

Setting the bits in register 0A1 will not affect the indications on bit 2 and bit 3 of the interrupt extended status register (0A0h) and bit 2 and bit 5 of the keyboard/pointing device receive status register (06Ah). These bits are reset to 0 at power-up reset.

INTERRUPT EXTENDED STATUS REGISTER (0A0h)

IRQ1 (hardware interrupt) of the interrupt controller is shared by three devices; real time clock, J1 interface and J2 interface. This register determines which device generated the IRQ1.

The bit functions of this register are described in Table 13.

When bit 3 is 1, it indicates a pending interrupt from interface J2 (keyboard or pointing device). Bit 3 can be reset by toggling bit 6 of register 066h or bit 4 of register 069h. When bit 2 is 1, it indicates a pending interrupt from interface J1 (keyboard or pointing device). Bit 2 can be reset by toggling bit 4 of register 066h or bit 3 of register 069h. When bit 0 is 1, it indicates a pending interrupt from the real time clock. Bit 0 can be reset by reading the interrupt status register (0B0h) on the

TABLE 9. TRANSMIT CONTROL REGISTER

Address	W/R	Functions
0069	W/R	b7 = Enable Diagnostic Through Reg. 63h b6 = Blocks Reg. 63h Read b5 = Disable J1 and J2 Clock (1 = Disable) b4 = Toggle for System to Transmit Data Through J2 b3 = Toggle for System to Transmit Data Through J1 b2 = Enable NMI Diagnostic Through Reg. 63h b2 = Enable NMI Diagnostic Through Reg. 63h b1 = Not Used b0 = Not Used

TABLE 10. RECEIVE CONTROL REGISTER

Address	W/R	Functions
0066	W/R	b7 = System Drives the Clock on J2
	W/R	b6 = Toggle for System to Receive Data Through J2
	W/R	b5 = System Drives the Clock on J1
	W/R	b4 = Toggle for System to Receive Data Through J1
	W/R	b3 = J1 Has Keyboard Connection
	R	b2 = Key lock (0 = Key Is Locked)
	R	b1 = J2 Parity Error Indication
	R	b0 = J1 Parity Error Indication

real time clock. These bits are reset to 0 at power-up reset.

SYSTEM CONTROL REGISTER

The system control register (061h) is used as speaker control, enables the parity check on the I/O Channel and memory parity check on the system board. This register is read/write. The bits in this register are defined in Table 14.

When bit 5 is set to 1, it stops IOCHCK from generating an NMI. When cleared, an NMI is generated when IOCHCK goes active.

When bit 4 is set to 1, it stops a memory parity from generating an NMI. When cleared, an NMI is generated whenever a memory parity error is sensed.

Bit 1 is used as speaker data. This bit gates the output of timer 2. It is used to disable the timer's sound source or modify its output. When set to 1, it enables the output. When cleared, it forces the output to 0.

Bit 0 is routed to the timer input at GATE 2. When this bit is cleared, the timer operation is halted. This bit and bit 1 (speaker data) control the operation of the sound source.

At power-up reset, the contents of this register are reset to 0.

SYSTEM STATUS REGISTER (062h)

This port returns status and configuration information about the planar card. The bits are defined in Table 15.

Bit 7 - Parity Error status bit, is used to indicate that a memory error has been detected. This bit is read only and is cleared by a reset.

Bit 6 - I/O Channel Error status bit, is used to indicate the state of the IOCHCK pin. This bit is read only and is cleared by a reset.

Bit 5 - Timer 2 Output status bit, is used to reflect the current state of the output of timer channel 2. This bit is read only.

Bit 4 - Reserved, read as 0, and should be written as 0.

Bit 3 - Reserved, read as 0, and should be written as 0.

Bit 2 - Hard Disk Installed status bit, when set (1) indicates the hard disk drive is missing, and when reset (0) the hard disk is installed. This bit is set by the BIOS and defaults to 1 on reset.

Bit 1 - Coprocessor Installed status bit, when set (1) indicates that the coprocessor is installed, and when reset (0) indicates the coprocessor is missing. This bit is set by the BIOS. This bit defaults to 0 on reset.

Bit 0 - Reserved, read as 0, and should be written as 0.

PERIPHERAL SELECT CONTROL REGISTER (065h)

This register controls the following peripherals on the system board:

- Serial Controllers
- Floppy Controller
- Video Controller
- Parallel Controller
- Fixed Disk Controller

The bits in this register are defined in Table 16.

When a bit is set to 1, that peripheral is enabled. When the peripheral is enabled, the chip select signal is generated to start a read or write operation, and the read or write signal to the I/O channel is blocked. When the peripheral is disabled, the chip select signal is not generated and all read and write operations are directed to the I/O channel. See Table 16.

After power-up reset, all the bits of this register are reset to 0.

TABLE 11. RECEIVE STATUS REGISTER

Address	W/R	Functions
006A	R	b7 = Not Used b6 = J2 Status (0 = Receive in Progress) b5 = J1 Receive Buffer Full (Interrupt Status) b4 = Not Used b3 = J1 Status (0 = Receive in Progress) b2 = J2 Receive Buffer Full (Interrupt Status) b1 = Not Used b0 = High Density Floppy Media (0 = High Density)

TABLE 12. INTERRUPT EXTENDED CONTROL REGISTER

Address	W/R	Functions
00A1	W/R	b7 = Not Used b6 = Not Used b5 = Not Used b4 = Not Used b3 = Mask Out Interrupt from J2 b2 = Mask Out Interrupt from J1 b1 = Not Used b0 = Mask Out Interrupt from Real Time Clock

TABLE 13. INTERRUPT EXTENDED STATUS REGISTER

Address	W/R	Functions
00A0	R	b7 = Not Used b6 = Not Used b5 = Not Used b4 = Not Used b3 = IRQ1 from J2 b2 = IRQ1 from J1 b1 = Not Used b0 = IRQ1 from Real Time Clock

ADDRESS DECODE FOR FLOPPY CONTROLLER

VL82C032 has the capability to decode the I/O address for an on-board floppy controller and generates the select signal for the floppy controller. From the system point of view, the floppy controller and its associated registers inside the VL82C032 are on the same bus (I/O extended bus). The VL82C032 can control the data buffers between the I/O extended bus and the I/O channel during I/O cycles or DMA cycles for the floppy controller.

Two latch enable signals (–RD3F0 and –RD3F1) are decoded for this purpose. The bits in these latches should be connected as shown in Table 17.

ADDRESS DECODE FOR HARD DISK CONTROLLER

VL82C032 has the capability to decode the I/O address for the on-board hard disk controller and generates the select signal for the controller. From the system point of view, the hard disk controller and its associated registers reside on the same bus (I/O extended bus) as the VL82C032. VL82C032 can control the data buffers between the I/O extended bus and the I/O channel during I/O cycles or DMA cycles for the hard disk controller. The I/O address range for the hard disk controller is between 320h and 32Fh. Accessing these addresses will activate the –SELHDK output (pin 4). It uses DMA channel 3 for DMA access.

TABLE 14. SYSTEM CONTROL REGISTER

Address	W/R	Functions
0061	W/R	b7 = Not Used (0). b6 = Not Used (0). b5 = IOCHCK, PC-Bus Memory Parity Check (1 = Disable, 0 = Enable) b4 = On-Board Memory Parity Check (1 = Disable, 0 = Enable) b3 = Not Used (0). b2 = Not Used (0). b1 = Speaker Data, Enable/Disable Output of 8253-Timer 2 (1 = Enable, 0 = Disable) b0 = Enable/Disable 8253-Timer 2 (1 = Enable, 0 = Disable)

TABLE 15. SYSTEM STATUS REGISTER

Bit	Usage	Default
7	Parity Error	(R/O)
6	I/O Channel Error	(R/O)
5	Timer 2 Output	(R/O)
4	Reserved	0
3	Reserved	0
2	No Hard Disk	1
1	Coprocessor Installed	0
0	Reserved	0

TABLE 16. PERIPHERAL SELECT CONTROL REGISTER

Address	W/R	Functions
065	W/R	b7 = Parallel Port Output Enable b6 = Reserve (0) b5 = Reserve (0) b4 = Serial Port 1 Select b3 = Floppy Controller Select b2 = Video Select b1 = Parallel Port Select b0 = Hard Disk Select

TABLE 17. FLOPPY CONTROL LOGIC I/O ADDRESSES

Address	W/R	Functions
03F0	R	RAS A Port b7 = IRQ6 b6 = DRQ2 b5 = Step (Latched) b4 = Track 0 b3 = Head 1 Select b2 = Index b1 = Write Protect b0 = Direction
03F1	R	RAS B Port b7 = Not Used b6 = Drive Select 1 b5 = Drive Select 0 b4 = Write Data (Latched) b3 = Read Data (Latched b2 = Write Enable (Latched) b1 = Drive Select 3 b0 = Drive Select 2

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
tSU1	Address Setup Time before Command	50		ns	
tH2	Address Hold Time after Command	50		ns	
tSU3	ADSEL Setup Time before Command	30		ns	
tH4	ADSEL Hold Time after Command	50		ns	
tH5	Read Data Invalid from End of Read	5		ns	
tH6	Write Data Hold Time	20		ns	
tD7	Real Time Controller Data Valid from Read		160	ns	
tSU8	Real Time Controller Write Data Setup Time	100		ns	
tD9	Asynchronous Controller Data Valid from Read		140	ns	
tSU10	Asynchronous Controller Write Data Setup Time	160		ns	
tD11	Timer Controller Data Valid from Read		160	ns	
tD12	Timer Controller Data Valid from ADDR		260	ns	
tSU13	Timer Controller Write Data Setup Time	160		ns	
tD14	Internal Registers Data Valid from Read		110	ns	
tSU15	Internal Registers Write Data Setup Time	100		ns	
tD16	Interrupt Controller Data Valid from Read		150	ns	
tSU17	Interrupt Controller Write Data Setup Time	100		ns	
tD18	Interrupt Vector from Interrupt Acknowledge		150	ns	
tD19	Interrupt Vector Invalid after Acknowledge	5		ns	

FIGURE 1. *READ TIMING DIAGRAM FOR TIMER CONTROLLER (8253)

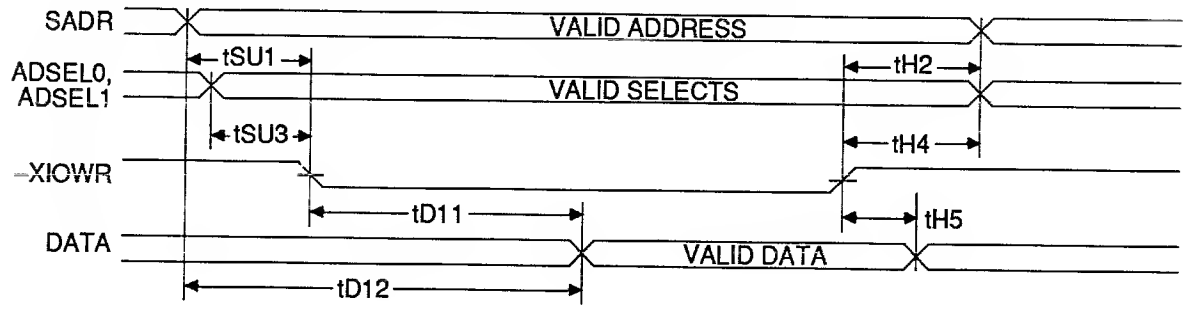


FIGURE 2. *WRITE TIMING DIAGRAM FOR TIMER CONTROLLER (8253)

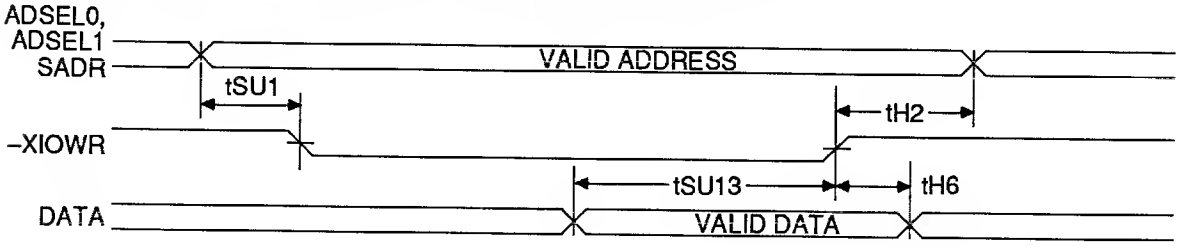


FIGURE 3. *READ TIMING DIAGRAM FOR ASYNCHRONOUS SERIAL COMMUNICATIONS CONTROLLER (8250A)

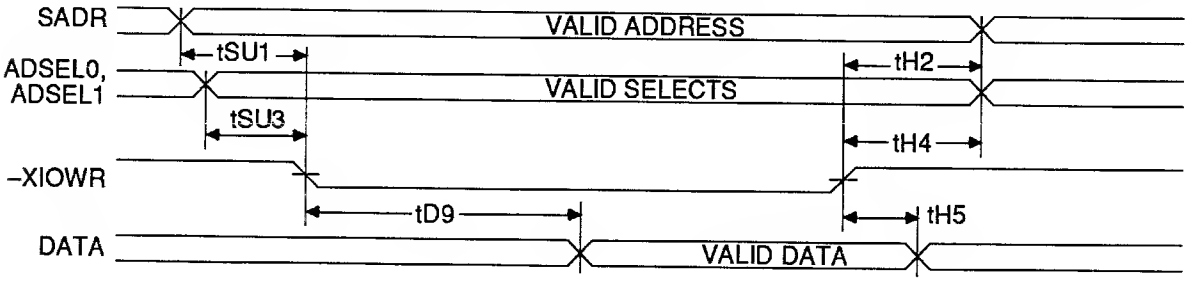
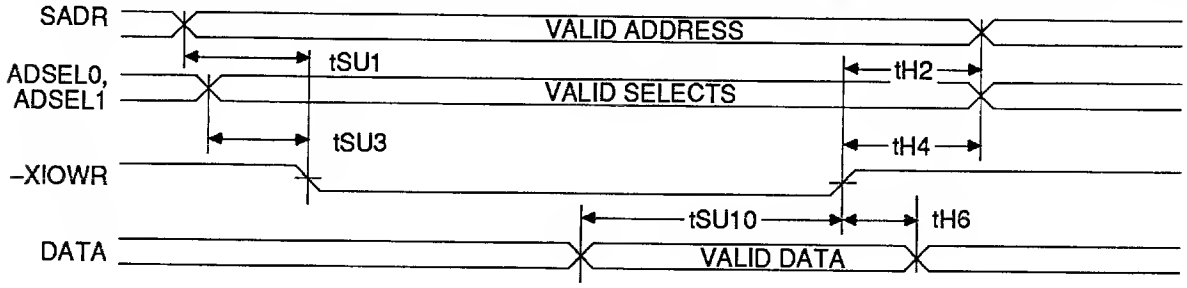


FIGURE 4. *WRITE TIMING DIAGRAM FOR ASYNCHRONOUS SERIAL COMMUNICATIONS CONTROLLER (8250A)



***Note:** Data Lines - Output Loading = 40 pF.

FIGURE 5. *READ TIMING DIAGRAM FOR INTERRUPT CONTROLLER (8259)

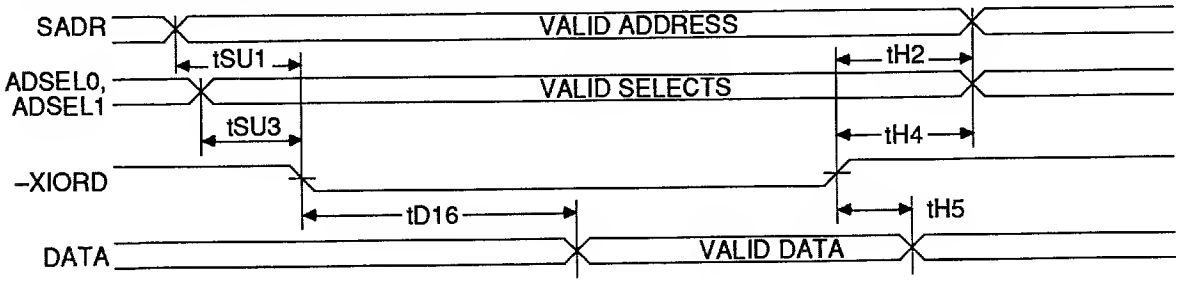


FIGURE 6. *WRITE TIMING DIAGRAM FOR INTERRUPT CONTROLLER (8259)

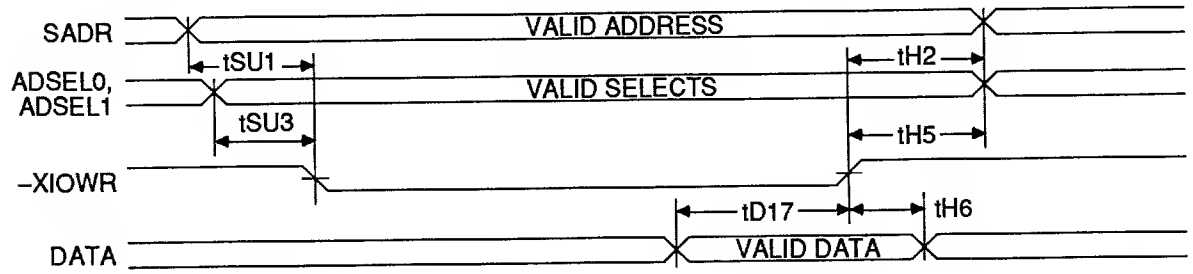


FIGURE 7. *INTERRUPT ACKNOWLEDGE TIMING DIAGRAM FOR INTERRUPT CONTROLLER (8259)

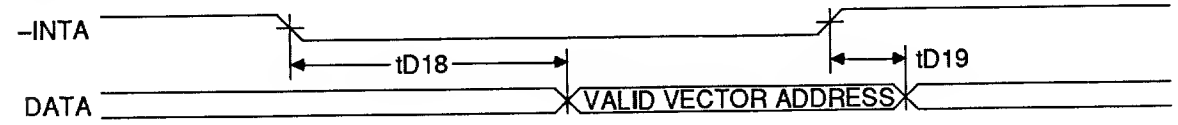
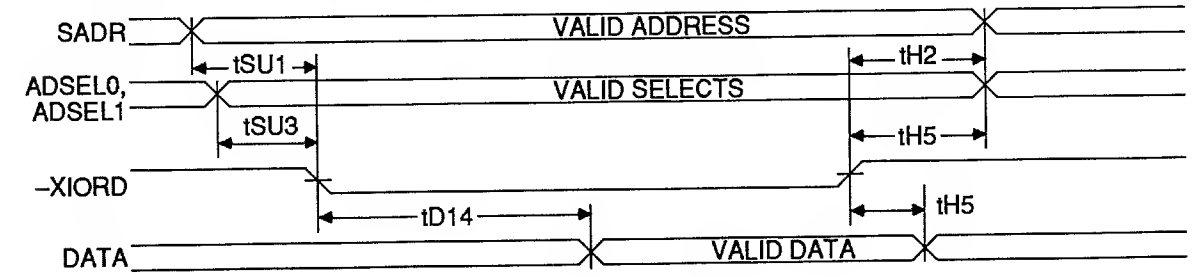


FIGURE 8. *READ TIMING DIAGRAM FOR INTERNAL REGISTERS



***Note:** Data Lines - Output Loading = 40 pF.

FIGURE 9. *WRITE TIMING DIAGRAM FOR INTERNAL REGISTERS

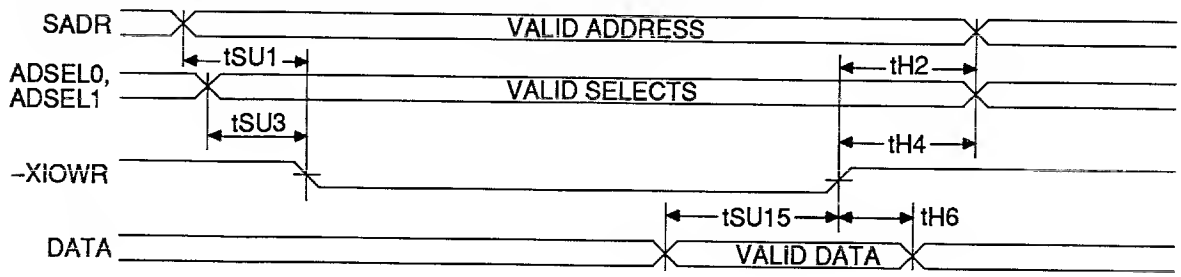


FIGURE 10. **TIMING DIAGRAM FOR FLOPPY OR HARD DISK CHIP SELECT

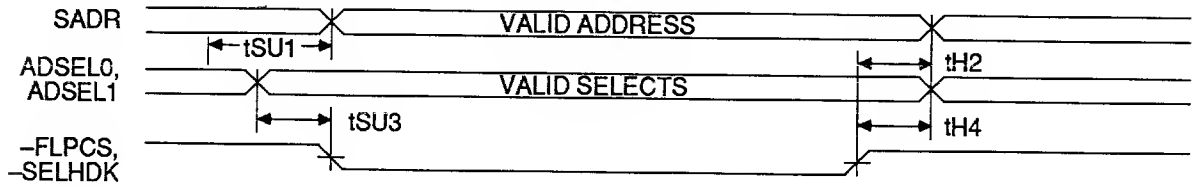


FIGURE 11. *READ TIMING DIAGRAM FOR REAL TIME CLOCK (58167A)

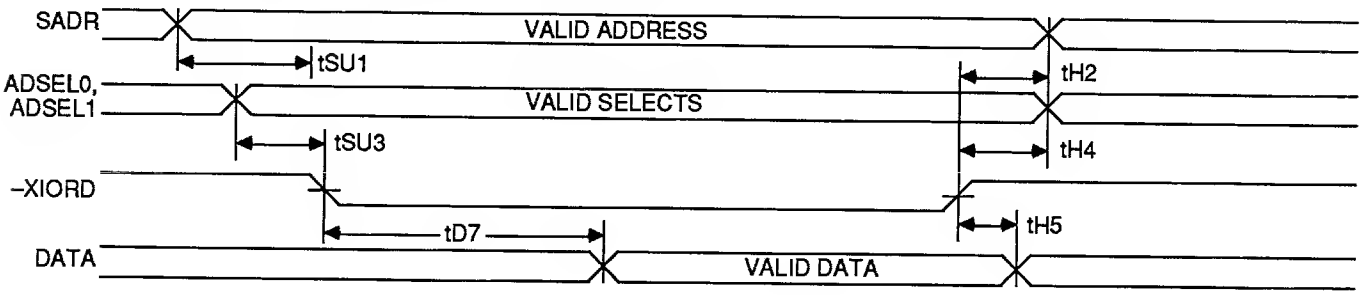
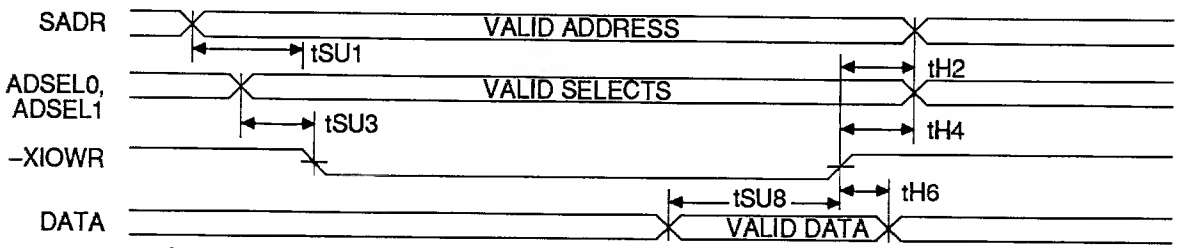


FIGURE 12. *WRITE TIMING DIAGRAM FOR REAL TIME CLOCK (58167A)



***Note:** Data Lines - Output Loading = 40 pF.
****Note:** FLPCSH - Output Loading = 20 pF. -SELHDK - Output Loading = 20 pF.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to VCC +0.3 V
Applied Output Voltage	−0.5 V to VCC +0.3 V
Applied Input Voltage	−0.5 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	Note
VOL	Output Low Voltage		0.45	V	Note
VIH	Input High Voltage	2.2	VCC + 0.5	V	Pins 16-19, 49, 94
VIH	Input High Voltage	2.0	VCC + 0.5	V	All Other Inputs*
VIL	Input Low Voltage	−0.5	0.8	V	TTL
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILI	Input Leakage Current	−150	10	µA	Pins 82-87
ILI	Input Leakage Current	−10	10	µA	All Other Inputs*
OLI	Output Leakage Current	−10	10	µA	
ICC	Operating Supply Current		40	mA	

Note: Output Current Driving Capabilities for VOH and VOL DC Parameters

IOH	IOL	VL82C032 Pins
−400 µA	20 mA	−LED, PD0-PD7
−400 µA	16 mA	J1DATA, J2DATA, J1CLOCK, J2CLOCK
−400 µA	10 mA	−INIT, −STROBE, −SELIN, −AUTOFD
−400 µA	8 mA	XD0-XD7, KEYLOCK, −SELHDK
−400 µA	4 mA	INTR, SPKOUT, −FLPCS, −XBFRD, TXD1, TXD2, −DTR1, −DTR2, −RTS1, −RTS2
−400 µA	2 mA	DRVTYPE, −PRE, −RD3F0, −RD3F1, −TIMER2

* RTCLKIN (Pin 56) is a crystal input and is not intended to conform to typical TTL input levels. For testing purposes it is driven to 4.0 V and 0.2 V for a logic high and low respectively.

VLSI TECHNOLOGY, INC.

VL82C037

IBM VGA®-COMPATIBLE VIDEO GRAPHICS CONTROLLER

FEATURES

- Single-chip VGA video graphics device that is completely compatible in the following systems:
  - –IBM PC/AT-compatible
  - –IBM PC/XT-compatible
  - –IBM PS/2-compatible
- Fully compatible with IBM VGA in all modes
- Provides 800 x 600 element high-resolution graphics with 16 colors
- Flicker-free operation in all video modes
- Supports 132-column text modes
- Supports both digital and analog monitor

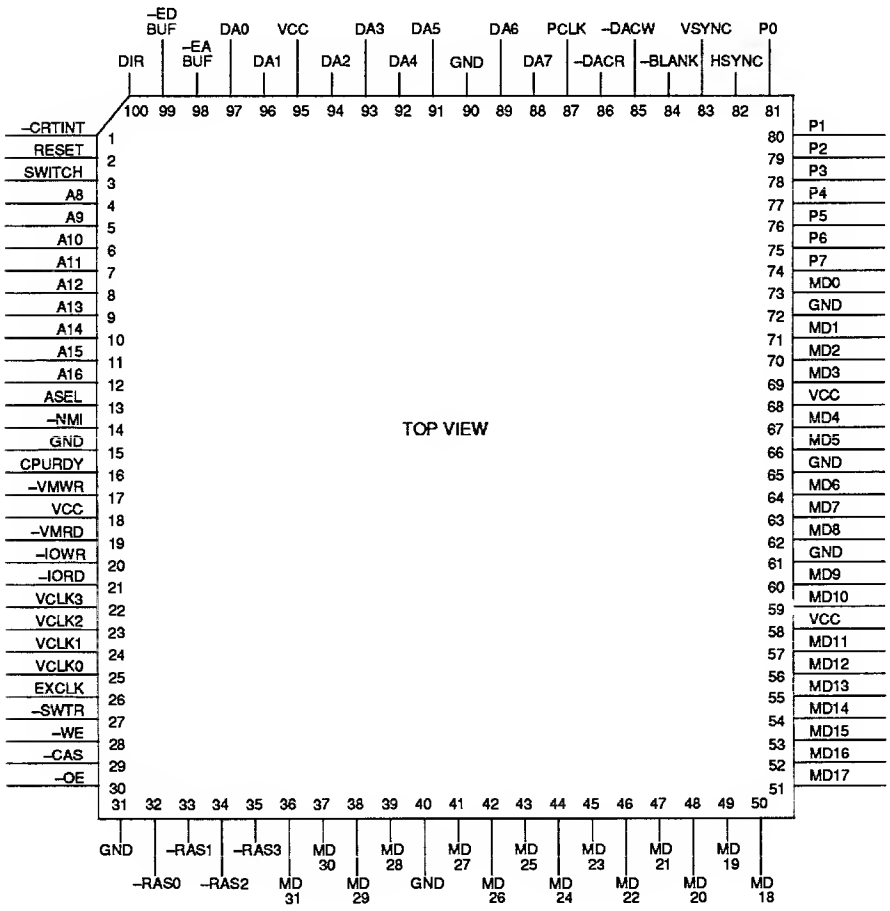
DESCRIPTION

The VL82C037 VGA-compatible Video Graphics Controller is a single-chip, high-integration, high resolution graphics device intended for use in IBM PS/2® Model 30-compatible systems as well PC/AT- and PC/XT-compatible systems. It provides high resolution graphics up to 800 x 600 elements with 16 colors.

The VL82C037 is fully compatible with IBM VGA in all modes, as well as being fully compatible with Hercules graphics. VL82C037 compatibility also extends to IBM EGA BIOS® (basic input/output system), CGA and MDA. It is also flicker-free in all modes. It supports an external digital-to-analog look-up table. The VL82C037 is available from VLSI Technology, Inc. in an industry-standard plastic 100-pin flatpack.

PIN DIAGRAM

VL82C037



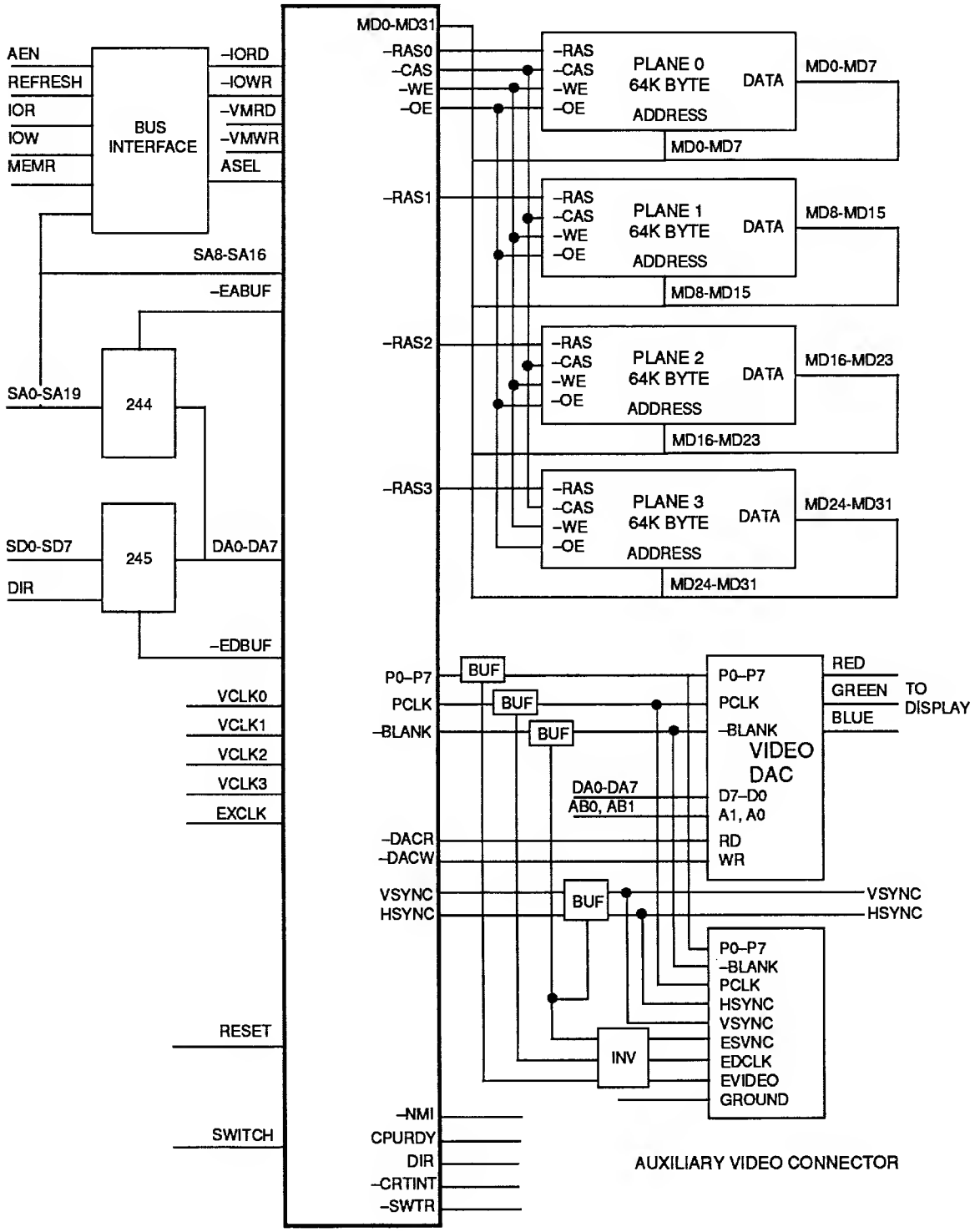
ORDER INFORMATION

Part Number	Package
VL82C037-FC	Plastic Flatpack

Notes: Operating temperature range is 0°C to +70°C.

IBM PS/2®, IBM VGA®, and IBM BIOS® are registered trademarks of IBM Corp.

SYSTEM BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–CRTINT	1	O	Display vertical retrace interrupt. An active low open collector.
RESET	2	I	System reset signal, active high.
SWITCH	3	I	Signal that detects the type of monitor. The state of this input can be read at Input Status Register 0 (Address 03C2) Bit 4.
A8-A16	4-12	I	CPU address bus bits 8 through16.
ASEL	13	I	Active high, to select VGA address to decode.
–NMI	14	O	Non maskable interrupt. An active low open collector.
CPURDY	16	O	An open collector active high output to signal processor that the VGA is ready for access.
–VMWR	17	I	Active low, video memory write signal.
–VMRD	19	I	Active low, video memory read signal.
–IOWR	20	I	Active low, I/O write signal.
–IORD	21	I	Active low, I/O read signal.
VCLK3	22	I	32.514 MHz input clock signal.
VCLK2	23	I	Reserved
VCLK1	24	I	28.322 MHz input clock signal.
VCLK0	25	I	25.175 MHz input clock signal.
EXCLK	26	I	External clock signal.
–SWTR	27	O	Read DIP switch control signal. Active during I/O read from address 03DF (Index = 10).
–WE	28	O	Video memory write enable for bank A (first 256K video memory). An active low signal.
–CAS	29	O	Column address strobe to all planes. An active low signal.
–OE	30	O	Output enable signal to memory bank A (first 256K video memory). It is active low.
–RAS0-RAS3	32-35	O	Row address strobe to planes 0-3. An active low signal.
MD31	36	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 3.
MD30	37	I/O	Display memory address/data time multiplexed bus line 6, interface to video memory plane 3.
MD29	38	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 3.
MD28	39	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 3.
MD27	41	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 3.
MD26	42	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 3.
MD25	43	I/O	Display memory address/data time multiplexed bus line 1, interface to video memory plane 3.
MD24	44	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 3.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MD23	45	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 2.
MD22	46	I/O	Display memory address/data time multiplexed bus line 6, interface to video memory plane 2.
MD21	47	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 2.
MD20	48	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 2.
MD19	49	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 2.
MD18	50	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 2.
MD17	51	I/O	Display memory address/data time multiplexed bus line 1, interface to video memory plane 2.
MD16	52	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 2.
MD15	53	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 1.
MD14	54	I/O	Display memory address/data time multiplexed bus line 6, interface to video memory plane 1.
MD13	55	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 1.
MD12	56	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 1.
MD11	57	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 1.
MD10	59	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 1.
MD9	60	I/O	Display memory address/data time multiplexed bus line 1, interface to video memory plane 1.
MD8	62	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 1.
MD7	63	I/O	Display memory address/data time multiplexed bus line 7, interface to video memory plane 0.
MD6	64	I/O	Display memory address /data time multiplexed bus line 6, interface to video memory plane 0.
MD5	66	I/O	Display memory address/data time multiplexed bus line 5, interface to video memory plane 0.
MD4	67	I/O	Display memory address/data time multiplexed bus line 4, interface to video memory plane 0.
MD3	69	I/O	Display memory address/data time multiplexed bus line 3, interface to video memory plane 0.
MD2	70	I/O	Display memory address/data time multiplexed bus line 2, interface to video memory plane 0.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
MD1	71	I/O	Display memory address/data time multiplexed bus line I, interface to video memory plane 0.
MD0	73	I/O	Display memory address/data time multiplexed bus line 0, interface to video memory plane 0.
P7-P0	74-81	O	Video color look up table address bits 7 through 0.
HSYNC	82	O	Horizontal SYNC signal for monitor.
VSYNC	83	O	Vertical SYNC signal for monitor.
–BLANK	84	O	An active low blanking signal to external palette chip.
–DACW	85	O	An active low I/O write signal for external palette chip (256 color look up table).
–DACR	86	O	An active low I/O read signal for external palette chip (256 color look up table).
PCLK	87	O	Pixel clock signal for external palette chip (256 color look up table).
DA7-DA0	88, 89 91-94 96, 97	I/O	Multiplexed address/data bus bits 7 through 0.
–EABUF	98	O	Active low, enable external address buffer.
–EDBUF	99	O	Active low, enable external data buffer.
DIR	100	O	Control signal for bidirectional data bus transceiver.
VCC	18, 58 68, 95		System Power : +5 V
GND	15, 31, 40 61, 65, 72 90		System Ground

5

FUNCTIONAL DESCRIPTION

INTRODUCTION

The VGA single chip is a standard video controller for PS/2 line machines including Model 50, 60 and 80. With the same architecture, it can be used on Model 30 and PC/XT/AT systems too. Several new things supported by IBM VGA include higher resolution (640 x 480), new video mode, 256 colors support for 320 x 200 graphics mode, up to 64 shades of grey display for monochrome monitor, and eight fonts loaded into video RAM simultaneously. In the VL82C037 chip, even more functions are added to gain performance.

The host can access both VGA registers and video memory by setting up bus address and read/write commands to read or write 8-bit data. Video RAM and screen refresh activities occur concurrently and independently by assigning appropriate memory access cycles to each of them.

Most registers are readable so that BIOS and driver software can determine the current state of video. In the basic configuration, 256K byte of memory is needed as the display buffer. Four planes of video memory are controlled by four different –RAS (Row Address Strobe) signals, one –CAS (Column Address Strobe), one –WE (Write Enable), and one –OE (Output Enable) signal. The video data bus is time multiplexed with the video address bus in a way that outputs –RAS and –CAS address early in the memory cycle and inputs 8-bit data for read or output for write late in the memory cycle.

NMI (Non-Maskable Interrupt) is generated by trapping accesses to certain I/O ports so that backward compatibility can be achieved through software emulation. The VGA chip provides a 'DIRectional' signal to control data flow to the system data bus for CPU Read or Write.

MAJOR COMPONENTS

There are four major components of VL82C037 contained within a single 100-pin plastic flatpack. They are described below:

CRT CONTROLLER

The VL82C037 CRT Controller provides synchronization control, timing generation and supplies video memory addressing to display memory. Flexible timing configuration options are allowed by accessing I/O registers through software control. During the blanking period, an 8-bit refresh counter is placed on the memory address lines. A split screen feature is also provided to allow two windows. This is done using the Preset Row Scan Register, the Line Compare Register, and the Horizontal Panning Register to pan part of the screen while the rest remains stationary.

SEQUENCER

The VL82C037 Sequencer takes care of basic memory timing for the display memory and the character clock for the control of memory fetches.

The state machine in the sequencer automatically assigns appropriate memory access cycles to the CPU and CRT Controller during active display. The sequencer can also protect the entire memory plane by selectively masking out planes through the Mask register.

GRAPHICS CONTROLLER

The Graphics Controller provides a data path for both CPU Read/Write and CRT Read access to the display memory. For CRT access it directs data to the Attribute Controller while for CPU access it directs data to the system bus. It handles two basic modes which are alphanumeric and graphics. In alphanumeric mode, data is sent in parallel directly to the Attribute Controller. In graphics mode memory data is shifted out serially to the Attribute Controller.

Data formatting and manipulation are implemented for the various modes. A color comparator is provided for fast color comparison in the application of color painting modes. Since the Graphics Controller can process 32-bit data (8-bits from each plane) at a time, a fast color presetting and area fill operations can be achieved.

ATTRIBUTE CONTROLLER

The VL82C037 Attribute Controller provides video shifting, attribute processing and an internal palette of 16 colors selectable from a possible 64 colors. Pixel panning is also provided for both graphics and text modes. Underline, cursor and blinking logic are interpreted and manipulated here. The final output of Attribute Controller is 8-bit wide color data to be sent to the external color look-up table for final color mapping.

MEMORY AND CLOCK CONSIDERATIONS

In basic configuration, eight 64K x 4-bit dynamic RAM's should be used to configure 256K byte of video memory. The supported speed of DRAM and CLOCK are related to the graphics resolution as shown in Table 1.

VGA REGISTERS

All the registers in the VGA can be categorized into six groups for the different function blocks in the hardware. In the VL82C037 VGA chip, the system microprocessor data latches are readable for faster save and restore of the VGA state in the VGA BIOS. The VGA also provides the system microprocessor interface for the video DAC (external color pallete chip). The DAC has one address register which can be accessed through address hex 03C7 for read, and hex 03C8 for write. Table 2 lists the registers and the I/O address where they are located. It also lists whether or not they are read/write, read-only, or write-only.

Note that the PEL Mask Register must not be written to by application code or destruction of the color look-up table data may occur.

GENERAL REGISTERS

This section describes the general registers. The (?) in some of the addresses is controlled by bit 0 of the Miscellaneous Output Register.

TABLE 1. RESOLUTION REQUIREMENTS

DRAM	120 ns	120 ns	100 ns
CLOCK	28 MHz	25 MHz	36 MHz
RESOLUTION	720 x 400	640 x 480	800 x 600
COLORS	16	16	16

TABLE 2. VGA REGISTERS

Register Group	R/W	Mono Emulation	Color Emulation
General Registers			
Miscellaneous	W	03C2	03C2
	R	03CC	03CC
Input Status 0	RO	03C2	03C2
Input Status 1	RO	03BA	03DA
Feature Control	W	03BA	03DA
	R	03CA	03CA
VGA Enable	RW	03C3	03C3
PEL Address (Write)	RW	03C8	03C8
PEL Address (Read)	WO	03C7	03C7
PEL Data Register	RW	03C9	03C9
PEL Mask	RW	03C6	03C6
Sequencer Registers			
Address Register	RW	03C4	03C4
Data Registers	RW	03C5	03C5
CRTC Registers			
Address Register	RW	03B4	03D4
Data Registers	RW	03B5	03D5
Graphics Registers			
Address Register	RW	03CE	03CE
Data Register	RW	03CF	03CF
Attribute Registers			
Address Register	RW	03C0	03C0
Data Registers	W	03C0	03C0
	R	03C1	03C1
Extended Registers			
Address Register	RW	03DE	03DE
Data Registers	RW	03DF	03DF

TABLE 3. GENERAL REGISTERS

Name	Read Port	Write Port
Miscellaneous Output	03CC	03C2
Input Status 0	03C2	—
Input Status 1	03?A	—
Feature Control	03CA	03?A
VGA Enable	03C3	03C3
DAC State	03C7	—

TABLE 4. VERTICAL SIZE REGISTER

Bit 7	Bit 6	Vertical Size
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

TABLE 5. CLOCK REGISTERS

CSEL2	CSEL1	CSEL0	CLOCK
0	0	0	25.175 MHz
0	0	1	28.322 MHz
0	1	0	External Input Clock
0	1	1	Reserved
1	0	0	14.161 MHz
1	0	1	16.257 MHz
1	1	0	Reserved
1	1	1	32.514 MHz

Miscellaneous Output Register
Read-03CC **Write-03C2**

Bit 7, 6 The Polarity of Vertical/ Horizontal Sync is used to select the vertical size as shown in Table 4.

Bit 5 Selects between two pages of memory when in the Odd/Even modes (mode 0-5, 7). A logical 0 selects the low page of memory; a logical 1 selects the high page of memory. This bit is provided for diagnostic use.

Bit 4 Reserved

Bit 3, 2 These two bits select the clock source. In VL82C037 VGA the third bit is defined in Extended Registers and used with these two bits to select a wider range of clock source for different video modes. See Table 5.

Bit 1 A logical 0 disables Video RAM address decode from the system microprocessor; a logical 1 enables Video RAM to the system microprocessor.

Bit 0 A logical 0 sets CRTC addresses to Hex 03BX and Input Status Register 0's address to 03BA for Monochrome emulation. A logical 1 sets CRTC addresses to Hex 03DX and Input Status Register 0's address to Hex 03DA for color emulation.

Input Status Register 0
Read-Only **Address = 03C2**

Bit 7 A logical 1 indicates a vertical retrace interrupt is pending. A logical 0 indicates the vertical retrace interrupt is cleared.

Bit 6, 5 Reserved

Bit 4 This bit allows the power-on initialization to determine if a monochrome or color monitor

is connected to the system. It reflects the state of the switch input.

Bit 3-0 Reserved

Input Status Register 1
Read-Only **Address = 03?A**
Bits 7, 6 Reserved

Bits 5, 4 These two bits are used for diagnostics. They are connected to two of the eight color outputs of the Attribute Controller. The two bits defined in the Color Plane Enable Register control the multiplexer for the color output wiring and are described in Table 6.

Bit 3 A logical 1 occurs during a vertical retrace interval. A logical 0 shows that video information is being displayed.

Bits 2, 1 Reserved

Bit 0 A logical 1 indicates a horizontal or vertical retrace interval. A logical 0 indicates that the internal Display Enable Signal is active. Some programs use this status bit to restrict screen updates to blanked display intervals. The VL82C037 has been designed to eliminate this software requirement, so display screen updates may be made at any time.

Feature Control Register
Read = 03CA **Write = 03?A**
Bits 7-4 Reserved

Bits 3 This bit should always be set to 0 to enable normal vertical sync output to the monitor; when bit 3 = 1, the "vertical sync" output is the logical OR of "vertical sync" and "vertical display enable". It is normally set to 0.

Bits 2-0 Reserved

Video Subsystem Enable Register
Read-03C3 **Write-03C3**
Bits 7-1 Reserved
Bit 0 A logical 1 enables video I/O and memory address decoding. A 0 disables the video I/O and memory address decoding.

SEQUENCER REGISTERS

This section describes the registers in the Sequencer Control block. See Table 7.

Sequencer Address Register
Read-03C4 **Write-03C4**
Bits 7-3 Reserved
Bits 2-0 A binary value pointing to the register where data is to be written or read.

Reset Register
Port = 03C5 **Index 0**
Bits 7-2 Reserved

Bit 1 A logical 0 directs the sequencer to synchronously clear and halt. Bits 1 and 0 must be 1 to allow the sequencer to operate. This bit must be set to 0 before changing either bit 3 or bit 0 of the Clocking Mode register, or bit 3 or bit 2 of the Miscellaneous Output Register, or bit 5, bit 4 or bit 3 of the Bandwidth Control Register.

Bit 0 A logical 0 directs the sequencer to asychronously clear and halt. Bit 1 and 0 must both be 1 to allow the sequencer to operate. Resetting the sequencer with this bit can cause data loss in the dynamic video RAM.

Clocking Mode Register
Port = 03C5 **Index 1**
Bits 7, 6 Reserved

Bit 5 When set to 1, turns off the video screen and assigns maximum memory bandwidth to the system CPU. A logical 0 puts the screen into normal operation. Synchronization pulses are maintained during blanking. This bit can be used for fast full-screen updates.

Bit 4 When set to 1, the internal shift registers are loaded every fourth character clock. When set to 0, they are loaded every character clock. When 32 bits are fetched each cycle and used together in the shift registers, this mode is useful.

Bit 3 A logical 0 selects normal the dot clock directly from the sequencer master clock input. A logical 1 will select master clock divided by two as dot clock. Normally, dot clock divided by two is used for 320 and 360 horizontal resolution modes.

Bit 2 When set to 1, the internal shift load registers are loaded every other character clock. When set to 0, and bit 4 is set to 0, the internal shift load registers are loaded every character clock. This mode is useful when 16 bits are fetched per cycle and chained together in the shift load registers.

Bit 1 Reserved

Bit 0 A logical 0 directs the sequencer to generate nine dot wide character clocks. A logical 1 generates eight dot wide character clocks from the

TABLE 6. REGISTER BITS

Color Plane Register		Input Status 1 Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

TABLE 7. SEQUENCER REGISTERS

Register Name	I/O Port	Index
Sequencer Address	03C4	—
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

TABLE 8. MAP SELECT (1)

Bit 5	Bit 3	Bit 2	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

TABLE 9. MAP SELECT (2)

Bit 4	Bit 1	Bit 0	Map	Table Location
0	0	0	0	1st 8K of Map 2
0	0	1	1	3rd 8K of Map 2
0	1	0	2	5th 8K of Map 2
0	1	1	3	7th 8K of Map 2
1	0	0	4	2nd 8K of Map 2
1	0	1	5	4th 8K of Map 2
1	1	0	6	6th 8K of Map 2
1	1	1	7	8th 8K of Map 2

sequencer. Select nine dots for alphanumeric modes only. For nine dot modes, the ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also, see the Line Graphics bit in the Mode Control Register in the Attribute Register section.

Map Mask Register
Port = 03C5 **Index = 02**

Bits 7-4 Reserved

Bits 3-0 A logical 1 enables the CPU to write to the corresponding memory map. These bits are used to write protect any memory map. When all four bits are logical 1, a 32-bit write operation can be performed by the CPU with only one memory cycle. This is useful for intensive screen updates in graphics modes. For odd/even modes, maps 0 and 1, and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation for CPU write.

Character Map Select Register
Port = 03C5 **Index = 03**

Bits 7, 6 Reserved

Bits 5,3,2 Selects font table from map 2 according to Table 8 when attribute bit 3 is a 1.

Bits 4,1,0 Selects font table from map 2 according to Table 9 when attribute bit 3 is a 0.

Note: Bit 3 of the attribute byte normally controls the foreground intensity in text modes. This bit, however, may be redefined as a switch between character sets. For this feature to work, the value of Character Map Select A must not equal the value of Character Map Select B.

Memory Mode Register
Port = 03C5 **Index = 04**

Bits 7-4 Reserved

Bit 3 A logical 0 enables the CPU to access data sequentially within a bit map by use of the Map Mask Register. A logical 1 causes two low-order address bits (A0, A1) to select the map that will be accessed according to Table 10. For read operation by the CPU, these two bits are also used to select the map in the graphics section.

TABLE 10. MAP SELECT (3)

A1	A0	Map Selected
0	0	Map 0
0	1	Map 1
1	0	Map 2
1	1	Map 3

Bit 2 A logical 0 directs even CPU addresses to access maps 0 and 2, while odd CPU addresses access maps 1 and 3. A logical 1 causes access to data within a bit map sequentially.

Bit 1 A logical 1 shows that greater than 64K bytes of video memory is being used. This is set to permit the VGA to use 256K bytes of video memory. This also enables character map selection. (See Character Map Select Register.)

Bit 0 Reserved

CRT CONTROLLER REGISTERS

This section describes the registers in the CRT Controller. See Table 11.

CRT Controller Address Register
Port = 03?4

Bits 7, 6 Reserved

Bit 5 Test bit, must remain 0.

Bit 4-0 Binary value programmed in these bits selects one of the CRT Controller registers where data is to be accessed.

Note: All CRT Controller Registers are read/write registers.

Horizontal Total Register
Port = 03?5 **Index = 0**

In the CRT Controller, there is a horizontal character counter which counts character clock inputs generated by the Sequencer and compares this against the value of the Horizontal Total Register to provide horizontal timings. The horizontal total defines the total number of characters in the horizontal scan interval including the retrace time.

5

TABLE 11. CRT CONTROLLER REGISTERS

Register Name	Port	Index
CRT Controller Address Register	03?4	—
Horizontal Total	03?5	00
Horizontal Display Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Start Vertical Retrace	03?5	10
End Vertical Retrace	03?5	11
Vertical Display Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blank	03?5	15
End Vertical Blank	03?5	16
CRTC Mode Control	03?5	17
Line Compare	03?5	18

? = B or D in accordance with Bit 0 of Miscellaneous Output register.

TABLE 12. SKEW

Bit 6	Bit 5	Amount of Skew
0	0	Zero Characters
0	1	One Characters
1	0	Two Characters
1	1	Three Characters

Bits 7-0 The total number of characters minus 5.

Horizontal Display Enable End Register
Port = 03?5 **Index = 01**

This register defines the length of the horizontal display enable signal. It determines the number of displayed character positions per horizontal line.

Bits 7-0 Total number of displayed characters minus 1.

Start Horizontal Blanking Register
Port = 03?5 **Index = 02**

Bit 7-0 This 8-bit value determines when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

End Horizontal Blanking Register
Port = 03?5 **Index = 03**

Bit 7 Test Bit

Bits 6, 5 Bits 6 and 5 indicate the magnitude of display enable skew. Display enable skew control is necessary to give adequate time for the CRT Controller to interrogate the display buffer in order to obtain a character and attribute code. It must also access the character generator font and access the Horizontal PEL Panning register in the Attribute Controller. The display enable signal must be skewed one character clock unit for every access. This allows the video output to be in synchronization with the horizontal and vertical retrace signals. See Table 12.

Bits 4-0 A binary value programmed in these bits is compared to the six least-significant bits of the horizontal character counter to determine the status of the horizontal blanking signal. When the values are equal the horizontal blanking signal becomes inactive. Use the following algorithm to calculate the value of the register:

Value of Start Blanking register + width of blanking signal in character clock units = 6-bit

result to be programmed into these bits. Bit number 5 is located in the End Horizontal Retrace register.

Start Horizontal Retrace Register
Port = 03?5 **Index = 04**

Bits 7-0 This register is used to center the screen horizontally and to specify the character position at which the Horizontal Retrace Pulse becomes active. The value programmed is a binary count of the character position at which the signal becomes active.

End Horizontal Retrace Register
Port = 03?5 **Index = 05**

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

Bit 7 This is bit number 5 of End Horizontal Blanking. The first four bits are located in the End Horizontal Blanking register (index hex 03).

Bits 6, 5 These bits control the skew of the Horizontal Retrace signal. See Table 12.

Bits 4-0 A value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive. Use the following algorithm to calculate the end of the retrace signal:

Value of Start Horizontal Retrace Register + Width of Horizontal Retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace Register.

Vertical Total Register
Port = 03?5 **Index = 06**

The 8-bit binary value gives the number of horizontal scan lines on the CRT screen, minus 2, including vertical retrace. This is the low-order 8-bits of a 10-bit value. Bit 8 of this register is located in the CRT Controller Overflow register (index 07, bit 0). Bit 9 of this register is located in the CRT Controller Overflow register (index 07, bit 5).

Bits 7-0 Total number of horizontal scan lines, minus 2.

Overflow Register
Port = 03?5 **Index = 07**

Bit 7 Bit 9 of the Start Vertical Retrace register.

Bit 6 Bit 9 of the Vertical Display Enable End Register.

Bit 5 Bit 9 of the Vertical Total Register.

Bit 4 Bit 8 of the Line Compare Register.

Bit 3 Bit 8 of the Start Vertical Blanking Register.

Bit 2 Bit 8 of the Start Vertical Retrace Register.

Bit 1 Bit 8 of the Vertical Display Enable End Register.

Bit 0 Bit 8 of the Vertical Total Register.

Preset Row Scan Register
Port = 03?5 **Index = 08**

Bit 7 Reserved

Bits 6, 5 Bits 6 and 5 control byte panning when programmed as multiple shift modes. (This is currently not used.) The PEL Panning register in the attribute section allows panning of up to eight single PELs. When in single byte shift modes the CRT Controller start address is increased by one, while attribute panning is reset to 0. This is done to pan the next higher PEL. When used for multiple shift modes, the byte pan bits are extensions to the Horizontal PEL Panning Register in the Attribute Controller. In this manner, panning across the width of the video output shift is achieved. In the 32-bit shift mode, the byte pan and PEL panning bits provide up to 31 bits of panning capability. To pan from position 31 to 32, the CRT Controller start address is incremented and PEL and byte panning is reset to 0. These bits should normally be set to 0.

Bits 4-0 A binary value to specify the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the row scan is cleared (not preset).

Maximum Scan Line Register
Port = 03?5 **Index = 09**

Bit 7 A logical 1 causes the clock to the row scan counter to be divided by 2 and enables 200 to 400 line conversion. This allows the older 200-line modes to be displayed as 400 lines on the display (i.e. each line is displayed twice). When this bit is a 0, the clock to the row scan counter is equal to the horizontal scan rate.

Bit 6 Bit 9 of the Line Compare Register.

Bit 5 Bit 9 of the Start Vertical Blank Register.

Bits 4-0 These bits specify the number of lines per character row. The number to be programmed is the maximum row scan number minus 1.

Cursor Start Register
Port = 03?5 **Index = 0A**

Bits 7, 6 Reserved

Bit 5 A logical 1 turns off the cursor, a logical 0 turns on the cursor.

Bits 4-0 The value of these five bits tells the row scan line of a character where cursor is to begin.

Note that when Cursor Start is programmed with a value greater than the Cursor End, no cursor is generated.

Cursor End Register
Port = 03?5 **Index = 0B**

Bit 7 Reserved

Bits 6, 5 These bits control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks. Each additional skew moves the cursor right one position on the screen. See Table 13.

Bits 4-0 These bits specify the row scan line where the cursor is to end.

TABLE 13. CLOCK SKEW

Bit 6	Bit 5	Function
0	0	Zero-character clock skew
0	1	One-character clock skew
1	0	Two-character clock skew
1	1	Three-character clock skew

Start Address High Register
Port = 03?5 Index = 0C

Bits 7-0 These are the high-order 8 bits of the start address. The 16-bit value from the high-order and low-order Start Address Registers is the first address after the vertical retrace on each screen refresh.

Start Address Low Register
Port = 03?5 Index = 0D

Bits 7-0 These are the low-order 8 bits of the start address.

Cursor Location High Register
Port = 03?5 Index = 0E

Bits 7-0 These are the high-order 8 bits of the cursor location.

Cursor Location Low Register
Port = 03?5 Index = 0F

Bits 7-0 These are the low-order 8 bits of the cursor location.

Start Vertical Retrace Register
Port = 03?5 Index = 10

Bits 7-0 These are the low-order 8 bits of the vertical retrace pulse start position in horizontal scan lines. Bit 8 and 9 are in the CRTC Overflow register.

End Vertical Retrace Register
Port = 03?5 Index 11

Bit 7 A logical 0 enables writing to CRTC registers 0-7. A logical 1 disables writing to these registers. Note that the line compare bit 4 in register 07 is not protected.

Bit 6 A logical 0 selects three refresh DRAM cycles. A logical 1 selects five refresh cycles per horizontal line. Five refresh cycles are used for slow (15.75 KHz) sweep rate displays.

Bit 5 A logical 0 enables a vertical retrace interrupt. This occurs on IRQ2. Since this may be a "shared" interrupt level, the Input Status register 0, bit 7, must be checked to determine if the VGA caused the interrupt to occur.

Bit 4 A logical 0 clears a vertical retrace interrupt. An interrupt handler has to reset an internal flip-flop by writing a 0 to this bit, then setting the bit to 1 so that the flip-flop does not hold interrupts inactive. Note that you should not change the other bits in this register when changing this bit. Read this register first before resetting this flip-flop so that the value of the other bits can be preserved.

Bits 3-0 These bits determine the horizontal scan count value when the vertical retrace output signal becomes inactive. Use the following algorithm to calculate the vertical retrace signal end:

Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal scan line units = 4-bit result to be programmed into the End Vertical Retrace register.

Vertical Display Enable End Register
Port = 03?5 Index = 12

Bits 7-0 These are the low-order 8 bits of a 10-bit register that determines the vertical display enable end position. Bits 8 and 9 of this register are contained in the CRT Controller Overflow register bits 1 and 6 respectively.

Offset Register
Port = 03?5 Index = 13

Bits 7-0 This register defines the logical line width of the screen. Starting memory address for the next character row is larger than the current character row by a factor of 2X or 4X this value. A word or doubleword address may be used to program the Offset Register, depending on the method of clocking the CRT Controller.

Underline Location Register
Port = 03?5 Index = 14

Bit 7 Reserved

Bit 6 A logical 1 enables doubleword mode for memory addresses. Also, see the description of the CRT Controller Mode Control register bit 6.

Bit 5 When this bit is set to 1, the memory address counter is clocked with the character clock divided by 4. This bit is used when doubleword addresses are used.

Bits 4-0 This register determines the horizontal row scan of a character row where an underline occurs. The scan line number desired is one greater than the number programmed.

Start Vertical Blanking Register
Port = 03?5 Index = 15

Bits 7-0 These are the low-order 8 bits of a 10-bit register. The value of this register determines when the vertical blanking signal becomes active. Bit 8 is located in the CRT Controller Overflow register bit 3. Bit 9 is contained in the CRT Controller Maximum Scan Line register bit 5. The horizontal scan line count (at which the vertical blanking signal becomes active) is one greater than the value of these 10 bits.

End Vertical Blanking Register
Port = 03?5 Index = 16

Bits 7-0 This register defines the horizontal scan count value at the time the vertical blank output signal goes inactive. The register must be programmed in whole units of horizontal scan lines. Use the following algorithm to obtain the vertical blank signal end value:

(Value of Start Vertical Blank register - 1) + width of vertical blank signal in horizontal scan unit = 8-bit result to be programmed into the End Vertical Blank register.

CRTC Mode Control Register
Port = 03?5 Index =17

Bit 7 A logical 0 clears horizontal and vertical retrace. A logical 1 enables horizontal and vertical retrace. This bit does not reset any other registers or outputs.

Bit 6 A logical 0 selects word address mode which shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. A logical 1 selects the byte address mode. Note that bit 6 of the Underline Location register also controls the addressing. When it is a 0, bit 6 of this register has control. When it is a 1, the addressing is forced to be shifted by two bits. (See Table 14.)

Bit 5 This bit selects the memory address counter bit MA13 or bit MA15, and it appears on the MA0 output in the word address mode. A logical 1 selects MA15. MA13 is selected for the case where only 64K memory is installed. Since 256K memory is normally installed for VL82C037, MA15 should be selected only in odd/even mode.

Bit 4 Reserved

Bit 3 A logical 0 causes the memory address counter to be clocked with the normal character clock input. A logical 1 clocks the memory address counter with the character clock input divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 A logical 0 selects normal horizontal retrace. A logical 1 selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter. This bit can be used to effectively double the vertical resolution capability of the CRT Controller. The 10-bit vertical counter has a maximum of 1024 scan lines. If the vertical counter is clocked with the horizontal retrace divided by 2, then the vertical resolution is doubled to 2048 horizontal scan lines.

Bit 1 A logical 0 selects row scan counter bit 1 for CRT memory address bit MA14. A logical 1 selects MA14 counter bit for CRT memory address bit MA14.

Bit 0 When this bit is a logical 0, row scan address bit 0 is substituted for memory address bit 13 during active display time. This allows compatibility with the 6845 CRTC. A logical 1 enables memory address bit 13 to appear on the memory address output bit 13 of the CRT Controller.

Line Compare Register
Port = 03?5 Index = 18

Bits 7-0 This register is the lower byte of the 10-bit line compare target. When the vertical counter matches this value, the internal start of the line counter is reset. This causes an area of the screen not to be affected by scrolling. Bit 9 is in the Maximum Scan Line register. Bit 8 of this register is in the Overflow Register.

TABLE 14. REGISTER MODES

Memory Address	Byte Mode	Word Mode	Doubleword Mode
MA0/RFA0	MA0	MA15/MA13	MA12
MA1/RFA1	MA1	MA0	MA13
MA2/RFA2	MA2	MA1	MA0
MA3/RFA3	MA3	MA2	MA1
MA4/RFA4	MA4	MA3	MA2
MA5/RFA5	MA5	MA4	MA3
MA6/RFA6	MA6	MA5	MA4
MA7/RFA7	MA7	MA6	MA5
MA8/RFA8	MA8	MA7	MA6
MA9	MA9	MA8	MA7
MA10	MA10	MA9	MA8
MA11	MA11	MA10	MA9
MA12	MA12	MA11	MA10
MA13	MA13	MA12	MA11
MA14	MA14	MA13	MA12
MA15	MA15	MA14	MA13

GRAPHICS CONTROLLER REGISTERS

This section describes the registers in the Graphics Controller. See Table 15.

Graphics Address Register
Port = 03CE

Bits 7-4 Reserved

TABLE 15. GRAPHICS CONTROLLER REGISTERS

Register Name	Port	Index
Graphics Address	03CE	–
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

TABLE 16. DATA FUNCTIONS

Bit 4	Bit 3	Function
0	0	Data Unmodified
0	1	Data ANDed with Latched Data
1	0	Data ORed with Latched Data
1	1	Data XORed with Latched Data

TABLE 17. ROTATE FUNCTIONS

Bit 2	Bit 1	Bit 0	Function
0	0	0	No Rotate
0	0	1	Rotate 1 Position
0	1	0	Rotate 2 Positions
0	1	1	Rotate 3 Positions
1	0	0	Rotate 4 Positions
1	0	1	Rotate 5 Positions
1	1	0	Rotate 6 Positions
1	1	1	Rotate 7 Positions

TABLE 18. MAP DATA

MS 1	MS 0	Function
0	0	Read Data from Map 0
0	1	Read Data from Map 1
1	0	Read Data from Map 2
1	1	Read Data from Map 3

Bits 3-0 A binary value in these bits selects the other registers in the Graphics Controller section.

Set/Reset Register
Port = 03CF **Index = 00**

Bits 7-4 Reserved

Bits 3-0 During CPU memory write with write mode 0, the value of these bits will be written to all eight bits of the respective memory map if Set/Reset mode is enabled for the corresponding map.

Enable Set/Reset Register
Port = 03CF Index = 01

Bits 7-4 Reserved

Bits 3-0 A logical 1 enables the Set/Reset function. When enabled, the respective memory map is written with the value of the Set/Reset register if write mode 0 is selected. However, when write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system microprocessor data.

Color Compare Register
Port = 03CF **Index = 02**

Bits 7-4 Reserved

Bits 3-0 These bits represent a 4-bit color value to be compared. If the system microprocessor sets read mode 1 and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the four maps equal the color compare register.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the eight bit positions of the selected byte are then compared across the four maps and a 1 is returned in each bit position where the bits of all four maps equal their respective color compare values.

Data Rotate Register
Port = 03CF **Index = 03**

Bits 7-5 Reserved

Bits 4, 3 Data in the system microprocessor latches can operate logically with data written to memory. If rotate function is selected, it is applied before the logical function. See Table 16.

Bits 2-0 These bits specify the number of positions to right-rotate the system microprocessor data bus during system microprocessor memory writes. This operation is done when the write mode is 0. To write non-rotated data, the bits should be set to 0. See Table 17.

Read Map Select Register
Port = 03CF **Index = 04**

Bits 7-2 Reserved

Bits 1, 0 These bits select the memory map number from which the system microprocessor reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0, 1 (2, 3). See Table 18.

Graphics Mode Register
Port = 03CF **Index = 05**

Bit 7 Reserved

Bit 6 A logical 0 permits bit 5 to handle the loading of the Shift Registers. A logical 1 supports the 256 color mode (only for 320 x 200 resolution).

Bit 5 A logical 1 instructs the Shift Registers in the graphic section to format the serial data with odd numbered bits from both of the odd numbered maps and even numbered bits

TABLE 19. FUNCTION DECODE

Bit-1	Bit-0	Function
0	0	The system microprocessor data is rotated by the number or counts in the Rotate Register that each memory map is written with, unless Set/Reset is enabled for the map. When the map Set/Reset is enabled, they are written with 8-bits of the value in the Set/Reset Register for that map.
0	1	The contents of the system microprocessor latches are written to each memory map. A system read operation loads these latches.
1	0	8-bits of the value of data bit n fills memory map n (0-3).
1	1	The maps are written by the 8-bits contained in the Set/Reset Register for that specific map (Enable Set/Reset Register is a "don't care"). Rotated system microprocessor data is logically ANDed with Bit Mask Register data and forms an 8-bit value. This is the function that the Bit Mask Register performs in write modes 0 and 2. (See Bit Mask Register.)

Note that the logic function specified by the Function Select register is applied to data being written to memory following modes 0, 2, and 3 described above.

from both of the even numbered maps. This bit is used in modes 4 and 5.

Bit 4 A logical 1 enables the odd/even addressing mode, which can emulate the IBM CGA. The value which should be programmed is the value of the Memory Mode register bit 2 of the Sequencer.

Bit 3 A logical 0 causes the system microprocessor to read data from the memory map selected by the Read Map Select register, unless chain 4 (bit 3 of the Sequencer Memory Mode Register) is set to 1. In this case the Read Map Select register has no effect. When this bit is a logical 1, the system microprocessor reads the results of the comparison of the four memory maps and the Color Compare register.

Bit 2 Reserved

Bits 1,0 Write Mode (See Table 19.)

Miscellaneous Register
Port = 03CF **Index = 06**

Bits 7-4 Reserved

Bits 3, 2 These bits control the mapping of the regenerative buffer into the CPU address space. The bit functions are defined in Table 20.

Bit 1 When set to a logical 1, this bit instructs the system microprocessor address bit 0 to be replaced by a higher-order bit. The odd/even maps will be selected with odd/even values of the system microprocessor A0 bit, respectively.

Bit 0 This is the text mode addressing control. A logical 1 enables the graphics mode. The character generator address latches are disabled when set to graphics mode.

Color Don't Care Register
Port = 03CF **Index = 07**

Bits 7-4 Reserved

Bit 3 1 - Do the color compare for map 3.
0 - Don't Care for map 3.

Bit 2 1 - Do the color compare for map 2.
0 - Don't Care for map 2.

Bit 1 1 - Do the color compare for map 1.
0 - Don't Care for map 1.

Bit 0 1 - Do the color compare for map 0.
0 - Don't Care for map 0.

Bit Mask Register
Port = 03CF **Index = 08**

Bits 7-0 Bits programmed to a 1 allow writes to the corresponding bits in the maps. A logical 0 permits the corresponding bit n in each map to be locked at its current state, providing the location being written was the last location read by the system's microprocessor.

Note that the bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

ATTRIBUTE CONTROLLER REGISTERS

This section describes the registers in the Attribute Controller section. See Table 21.

TABLE 20. BYTE SELECT

Bit 3	Bit 2	Function
0	0	Hex A0000 for 128K Bytes
0	1	Hex A0000 for 64K Bytes
1	0	Hex B0000 for 32K Bytes
1	1	Hex B8000 for 32K Bytes

TABLE 21. ATTRIBUTE CONTROLLER REGISTERS

Register Name	Port	Index
Address Register	03C0	–
Palette Registers	03C0	00-0F
Attribute Mode Control Register	03C0	10
Overscan Color Register	03C0	11
Color Plan Enable Register	03C0	12
Horizontal PEL Panning Register	03C0	13
Color Select Register	03C0	14

Attribute Address Register
Port = 03C0
Bits 7, 6 Reserved

Bit 5 Bit 5 must be written to 0 before loading the Color Palette registers. Normal operation of the Attribute Controller requires that bit 5 be set to 1, which allows the video memory data to reach the palette registers.

Bits 4-0 A binary value in these bits points to the Attribute Data register where data is to be written.

The Address and Data registers can not be selected directly. An internal address flip-flop controls this selection. To initialize the flip-flop, an I/O Read instruction must be sent to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and then selects the Address register. The Address register is then loaded with an I/O Write to 03C0. The following I/O Write instruction to 03C0 loads the Data register. The flip-flop changes state each time an I/O Write instruction is sent to the Attribute Controller. It does not change when an I/O Read to 03C1 occurs.

Palette Registers
Write-03C0 Read-03C1 Index-00-0F
Bits 7, 6 Reserved

Bits 5-0 The attribute byte of text or graphic color value is indexed to these 16 Color Palette registers. The content of the selected Palette register is then used as a value sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers.

The Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image.

Attribute Mode Control
Port = 03C0 (W), 03C1 (R) Index = 10

Bit 7 This bit selects the source for palette bits P4 and P5, which go to the video DAC. A logic 0 selects bits 4 and 5 of the palette registers above. A logic 1 selects bits 0 and 1 of the Color Select Register.

Bit 6 A logical 1 causes the video pipeline to be sampled so that eight bits are available to select a color in the 256 color mode (hex 13). This bit must be a logical 0 in all other modes.

Bit 5 A logical 0 makes line compare have no effect on the output of the PEL Panning register. A logical 1 causes a successful line compare in the CRTC to force the output of the PEL Panning register to 0. When VSYNC occurs, the output reverts to its programmed value. This bit allows part of the screen to be panned while the rest remains stationary.

Bit 4 Reserved

Bit 3 This bit is set to 1 for blinking graphics modes and alphanumeric modes. A logical 0 selects the background intensity of the attribute input.

Bit 2 A logical 1 enables the special line graphics character codes for the monochrome emulation mode. A logical 0 causes the ninth dot to be the same as the background. When this bit is set to 1 it forces the ninth dot of a line graphic character to be the same as the eighth dot. Graphics character codes are hex C0 through hex DF. For character fonts that do not use the line graphics character codes in this range (hex C0 through hex DF) bit 2 should be a 0. If not, unwanted video information will be shown on the CRT screen.

Bit 1 A logical 1 sets monochrome emulation mode. A logical 0 sets color emulation mode.

Bit 0 A logical 0 selects text mode. A logical 1 selects graphics mode.

Overscan Color Register
Port = 03C0 (W), 03C1 (R) Index = 11

Bits 7-0 A binary value in this register determines the border color displayed on the CRT screen. The border color is displayed right after the Display Enable signal goes low and before the start of blanking period. The border is not supported in the 40-column text modes or the 320-PEL graphics modes, except for mode hex 13.

Color Plane Enable
Port = 03C0 (W), 03C1 (R) Index = 12
Bits 7, 6 Reserved

Bits 5, 4 Two of the eight color outputs will be selected, according to these two bits, to be available for reading on bits 4 and 5 of Input Status Register 1. See Table 22.

Bits 3-0 A logical 1 in each bit enables the respective display memory color plane. A logical 0 disables the color plane.

Horizontal PEL Panning
Port = 03C0 (W), 03C1 (R) Index = 13
Bits 7-4 Reserved

Bits 3-0 These four bits select the number of pixels to shift the video data to the left. PEL panning is available in both graphics and text modes. In modes 0+, 1+, 2+, 3+, 7 and 7+, the maximum shift is eight pixels. Mode 13 allows a maximum of three pixels. In the remaining modes, the image can be shifted a maximum of seven pixels. The order for shifting the image is shown in Table 23.

Color Select Register
Port = 03C0 (W), 03C1 (R) Index = 14
Bits 7-4 Reserved

Bits 3, 2 These bits are the two high-order bits of the 8-bit digital color value sent off-chip in all modes except the 256 color graphics. In the 256 color modes, the 8-bit attributes are stored in video memory. This becomes the 8-bit digital color value to be sent off-chip to the video DAC. These bits can be used to switch quickly among sets of colors in the video DAC.

Bits 1, 0 These two bits can be used to replace the P4 and P5 bits from the Attribute Palette registers to form the 8-bit digital color value sent off-chip. This is controlled by bit 7 of Attribute Mode Control register. By using this feature, sets of colors can be rapidly switched in the video DAC.

TABLE 22. COLOR PLANE AND STATUS

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

TABLE 23. PEL REGISTER

PEL Panning Register Value	Number of PELs Shifted to the Left		
	0+, 1+, 2+ 3+, 7, 7+	All Other Modes	Mode 13
0	1	0	0
1	2	1	–
2	3	2	1
3	4	3	–
4	5	4	2
5	6	5	–
6	7	6	3
7	8	7	–
8	0	–	–

TABLE 24. EXTENDED REGISTERS

Port	Index	R/W	Bits	Register
3DE	–	R/W	5	Extension Address Register
3DF	D	R/W	6	Bandwidth Control
3DF	E	R/W	4	I/O Trap Control
3DF	F	R	8	NMI Data Cache (FIFO)
3DF	10	R	8	Read DIP Switch

5

EXTENDED REGISTERS
A set of new registers have been added into the basic VGA to perform new features and enhancements. They are grouped under I/O port 3DE and 3DF for address and data access respectively. All except the NMI Data Cache register have both read and write access. A summary of these registers is given in Table 24.

03DE - EXTENSION ADDRESS REGISTER

Bit	Description
0-4	5-bit index pointer to the extension data registers.
5-7	Reserved

The contents of this register need to be programmed before the data register is accessed. The I/O address is 3DE for both read and write access.

03DF - BANDWIDTH CONTROL INDEX D

Bit	Description
0-2	Reserved
3-4	Bandwidth Control (See Table 25.)
5	Clock select bit 2 (CSEL2). Used with bit 2 and 3 of Miscellaneous Register. Up to eight different clock inputs can be selected from. (See Table 5.)
6-7	Reserved

03DF - I/O TRAP CONTROL INDEX E

Bit	Description
0	When set to 1, it turns on the trap and generates NMI for downward compatibility emulation. When set to 0, it turns off the NMI logic.
1-2	Backward Compatibility Mode (See Table 26.)
3-6	Reserved = 0
7	Graphics Latch read compatibility.

03DF - NMI DATA CACHE INDEX F

Bit	Description
0-7	First read of this register gets the address of the trapped I/O.

Second read gets the data of the trapped I/O. The size of the cache is two bytes wide and six rows deep. Each read will cause the read pointer to auto-increment and then reset at the end of the information.

Note that only the first 8 bits of the I/O address are saved into the cache. Since bit 7 is always 1 if there is an address saved at this position, the trapped software should check this bit to determine whether this is the last read or not.

Note that this is a read only register.

03DF - READ DIP SWITCH INDEX 10

Bit	Description
7	Reserved
6	DIP Switch 6
5	DIP Switch 5
4	DIP Switch 4
3	DIP Switch 3
2	DIP Switch 2
1	DIP Switch 1
0	DIP Switch 0

These bits can be read by the BIOS to determine the configuration desired.

TABLE 25. BANDWIDTH

Bit 4	Bit 3	Bandwidth
0	0	1-4
1	0	1-7
0	1	1-9
1	1	Reserved

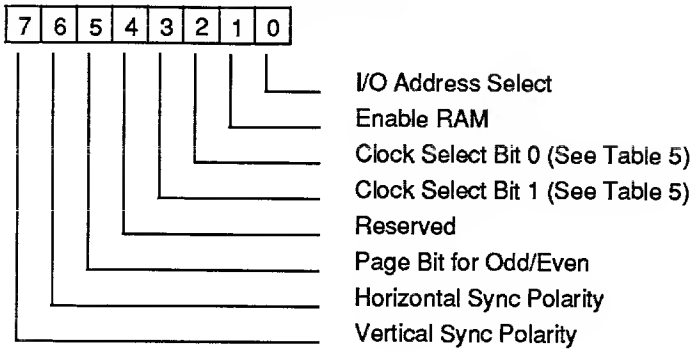
TABLE 26. GRAPHICS MODE

Bit 2	Bit 1	Mode
0	0	VGA
0	1	EGA
1	0	CGA
1	1	MCGA (MDA & HERC)

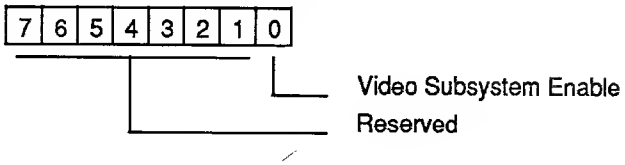
REGISTER SUMMARY

GENERAL REGISTERS

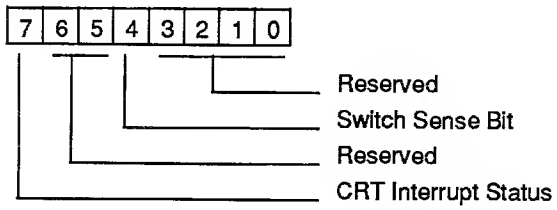
MISCELLANEOUS OUTPUT REGISTER
Address = 03CC (Read), 03C2 (Write)



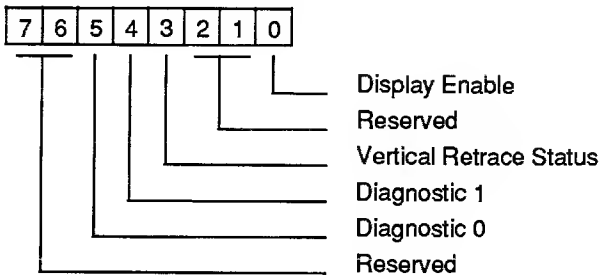
VIDEO SUBSYSTEM ENABLE REGISTER
Address = 03C3 (Read/Write)



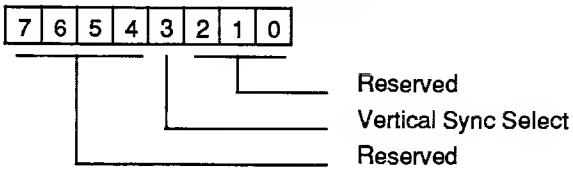
INPUT STATUS REGISTER 0
Address = 03C2 (Read Only)



INPUT STATUS REGISTER 1
Address = 03?A (Read Only)



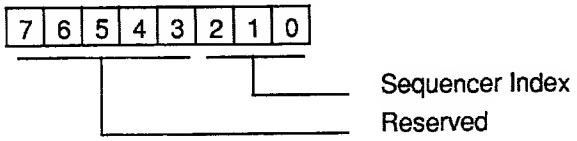
FEATURE CONTROL REGISTER
Address = 03CA (Read), 03?A (Write)



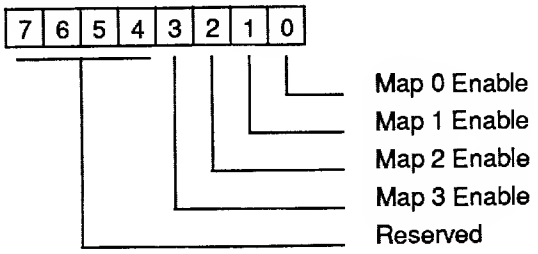
5

SEQUENCER REGISTERS

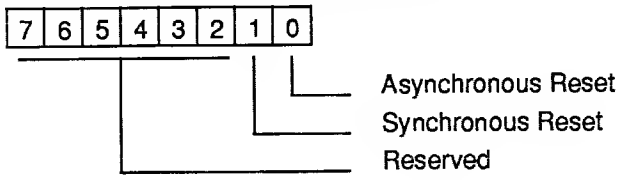
SEQUENCER ADDRESS REGISTER
Address = 03C4 (Read/Write)



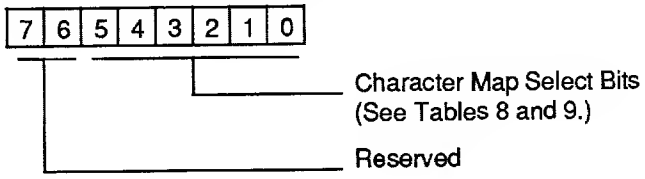
MAP MASK REGISTER
Address = 03C5 Index = 2 (Read/Write)



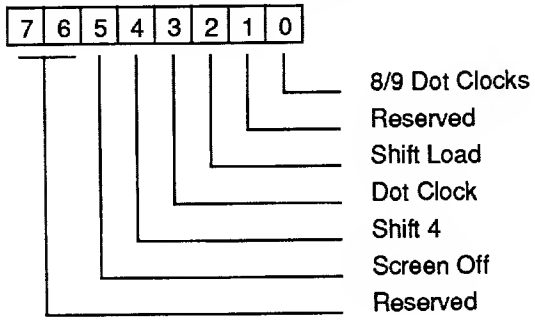
RESET REGISTER
Address = 03C5 Index = 0 (Read/Write)



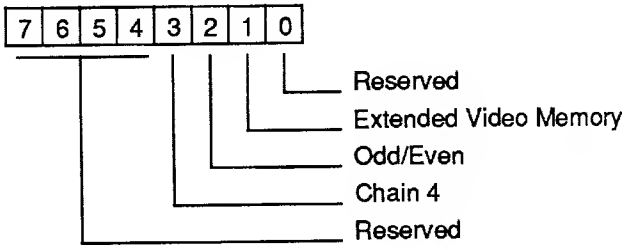
CHARACTER MAP SELECT REGISTER
Address = 03C5 Index = 3 (Read/Write)



CLOCKING MODE REGISTER
Address = 03C5 Index = 1 (Read/Write)

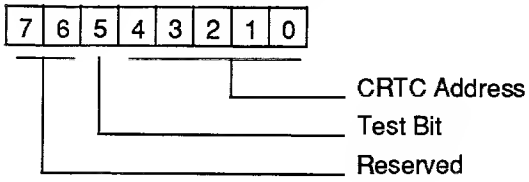


MEMORY MODE REGISTER
Address = 03C5 Index = 4 (Read/Write)

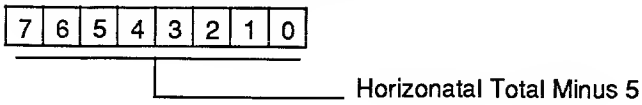


CRT CONTROLLER REGISTERS

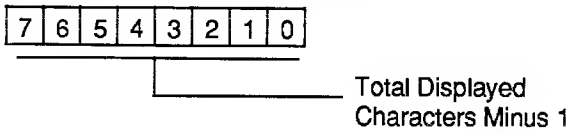
CRT CONTROLLER ADDRESS REGISTER
Address = 03?4 (Read/Write)



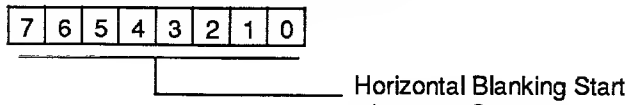
HORIZONTAL TOTAL REGISTER
Address = 03?5 Index 0 (Read/Write)



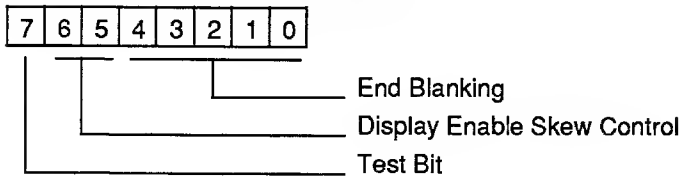
HORIZONTAL DISPLAY ENABLE END REGISTER
Address = 03?5 Index 1 (Read/Write)



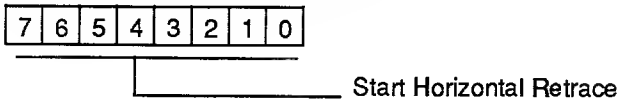
START HORIZONTAL BLANKING REGISTER
Address = 03?5 Index 2 (Read/Write)



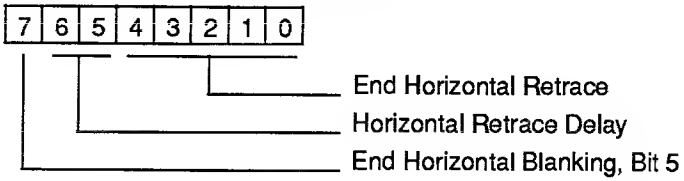
END HORIZONTAL BLANKING REGISTER
Address = 03?5 Index 3 (Read/Write)



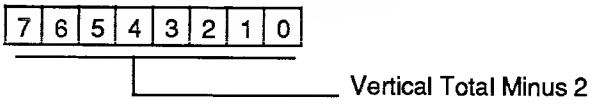
START HORIZONTAL RETRACE REGISTER
Address = 03?5 Index 4 (Read/Write)



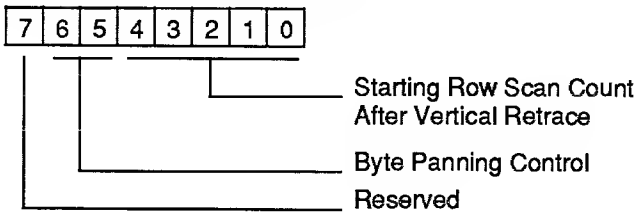
END HORIZONTAL RETRACE REGISTER
Address = 03?5 Index 5 (Read/Write)



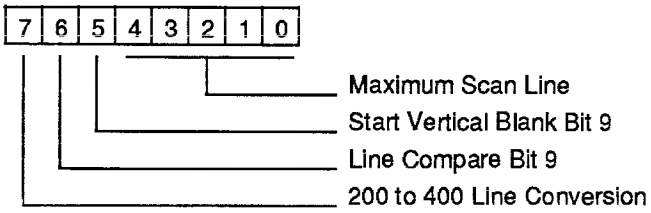
VERTICAL TOTAL REGISTER
Address = 03?5 Index 6 (Read/Write)



PRESET ROW SCAN REGISTER
Address = 03?5 Index 8 (Read/Write)



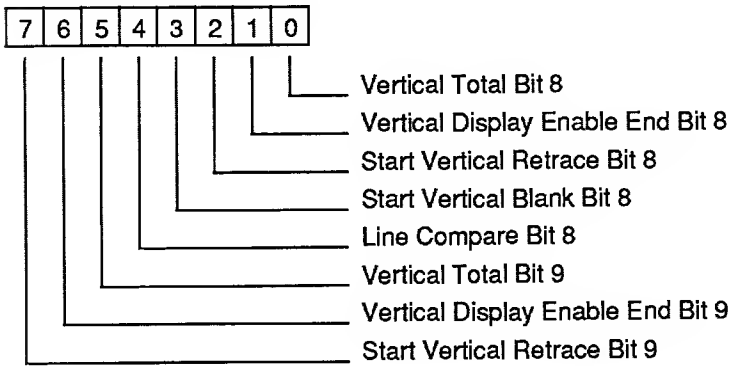
MAXIMUM SCAN LINE REGISTER
Address = 03?5 Index = 9 (Read/Write)



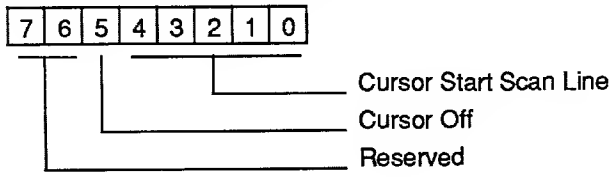
5

CRT CONTROLLER REGISTERS (Cont.)

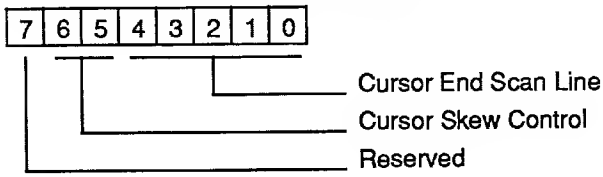
OVERFLOW REGISTER
Address = 03?5 Index 7 (Read/Write)



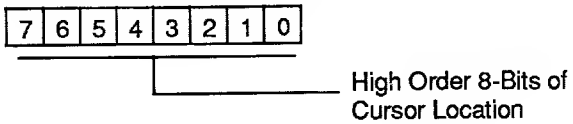
CURSOR START REGISTER
Address = 03?5 Index = A (Read/Write)



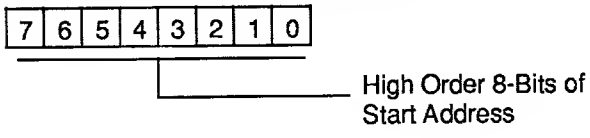
CURSOR END REGISTER
Address = 03?5 Index = B (Read/Write)



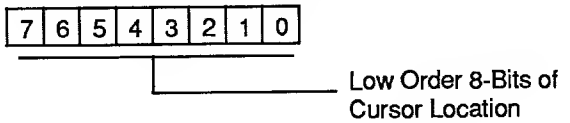
CURSOR LOCATION HIGH REGISTER
Address = 03?5 Index = E (Read/Write)



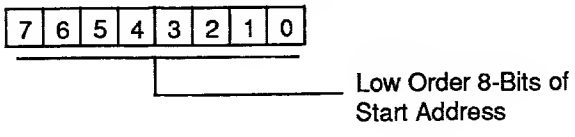
START ADDRESS HIGH REGISTER
Address = 03?5 Index = C (Read/Write)



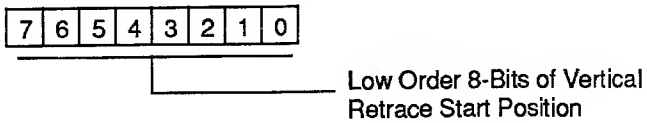
CURSOR LOCATION LOW REGISTER
Address = 03?5 Index = F (Read/Write)



START ADDRESS LOW REGISTER
Address = 03?5 Index = D (Read/Write)

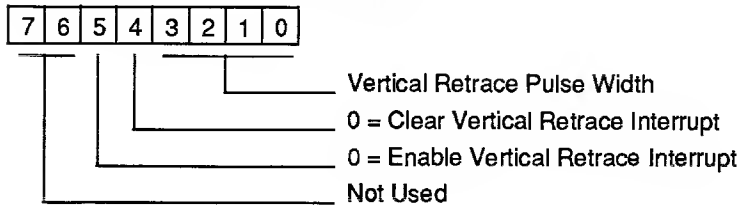


START VERTICAL RETRACE REGISTER
Address = 03?5 Index = 10 (Read/Write)

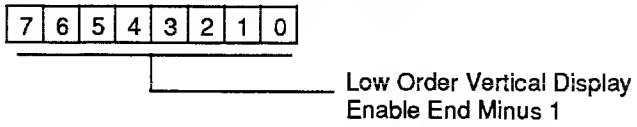


CRT CONTROLLER REGISTERS (Cont.)

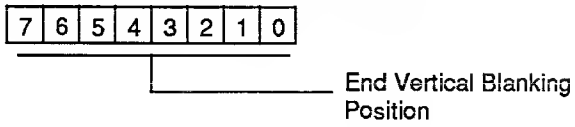
END VERTICAL RETRACE REGISTER
Address = 03?5 Index = 11 (Read/Write)



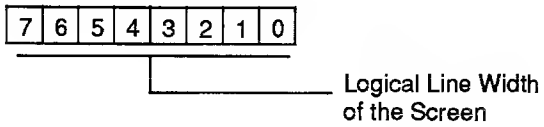
VERTICAL DISPLAY ENABLE END REGISTER
Address = 03?5 Index = 12 (Read/Write)



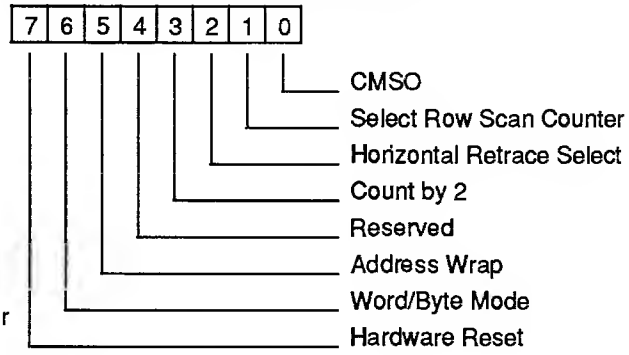
END VERTICAL BLANKING REGISTER
Address = 03?5 Index = 16 (Read/Write)



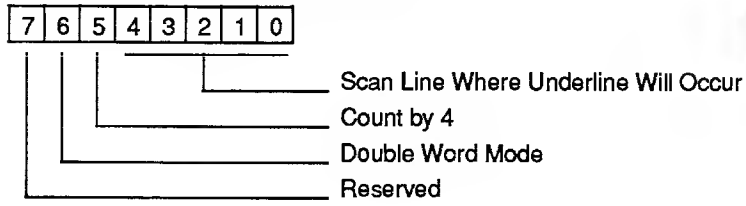
OFFSET REGISTER
Address = 03?5 Index = 13 (Read/Write)



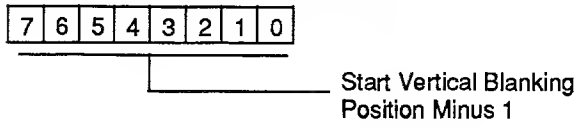
CRTC MODE CONTROL REGISTER
Address = 03?5 Index = 17 (Read/Write)



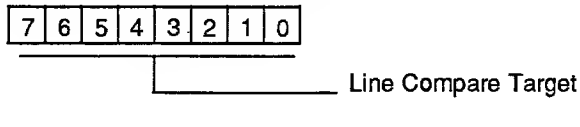
UNDERLINE LOCATION REGISTER
Address = 03?5 Index = 14 (Read/Write)



START VERTICAL BLANKING REGISTER
Address = 03?5 Index = 15 (Read/Write)



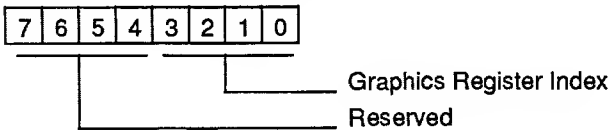
LINE COMPARE REGISTER
Address = 03?5 Index = 18 (Read/Write)



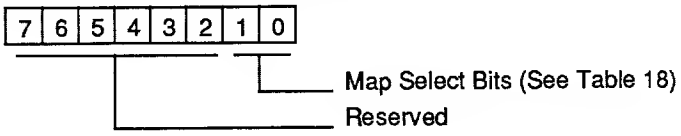
5

GRAPHICS CONTROLLER REGISTERS

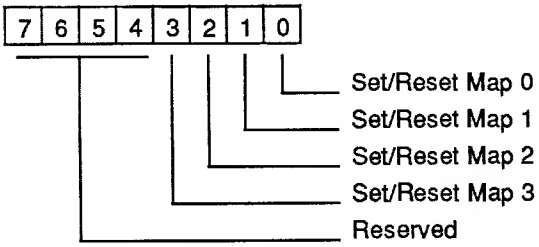
GRAPHICS ADDRESS REGISTER
Address = 03CE (Read/Write)



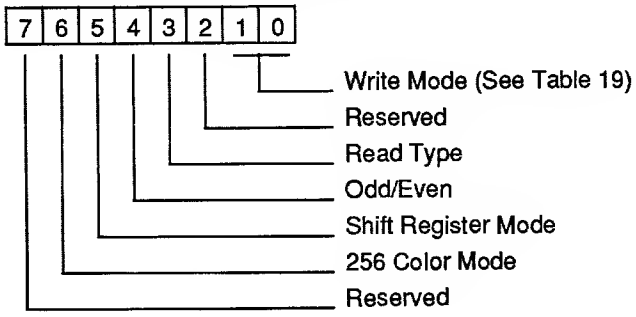
READ MAP SELECT REGISTER
Address = 03CF Index = 4 (Read/Write)



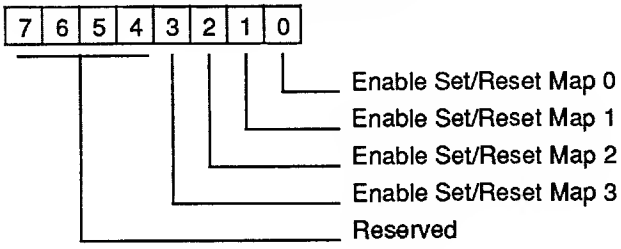
SET/RESET REGISTER
Address = 03CF Index = 0 (Read/Write)



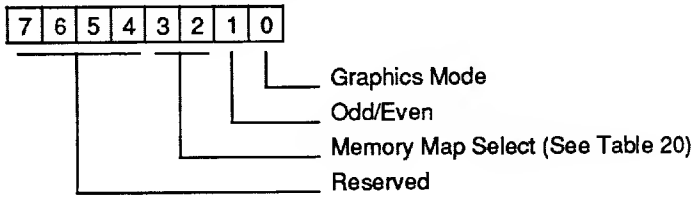
GRAPHICS MODE REGISTER
Address = 03CF Index = 5 (Read/Write)



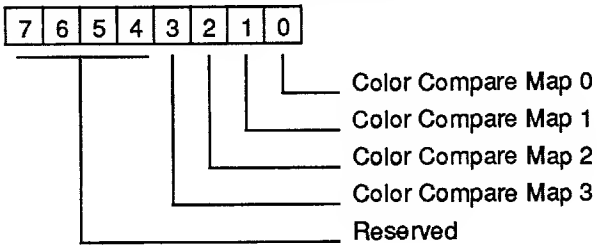
ENABLE SET/RESET REGISTER
Address = 03CF Index = 1 (Read/Write)



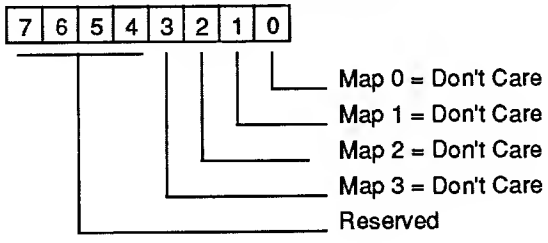
MISCELLANEOUS REGISTER
Address = 03CF Index = 6 (Read/Write)



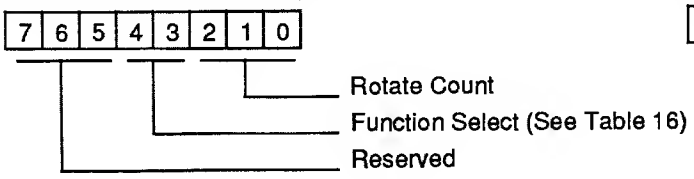
COLOR COMPARE REGISTER
Address = 03CF Index = 2 (Read/Write)



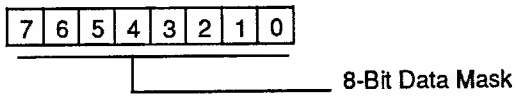
COLOR DON'T CARE REGISTER
Address = 03CF Index = 7 (Read/Write)



DATA ROTATE REGISTER
Address = 03CF Index = 3 (Read/Write)

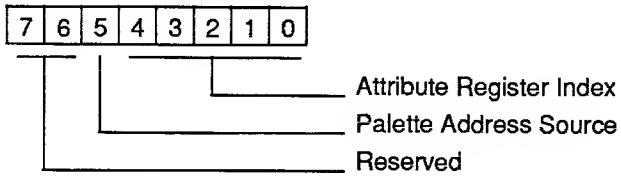


BIT MASK REGISTER
Address = 03CF Index = 8 (Read/Write)

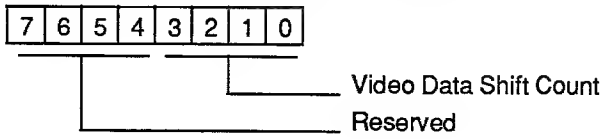


ATTRIBUTE CONTROLLER REGISTERS

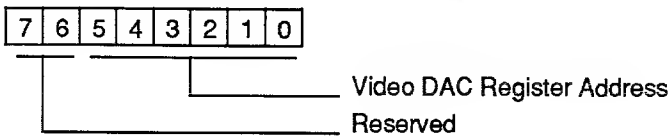
ATTRIBUTE ADDRESS REGISTER
Address = 03C0 (Read/Write)



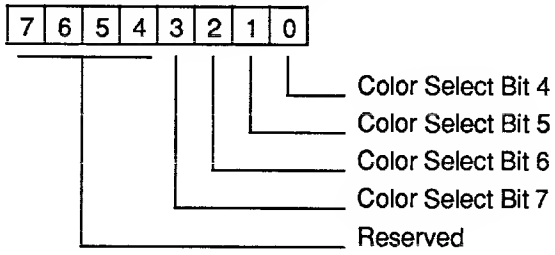
HORIZONTAL PEL PANNING REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 13



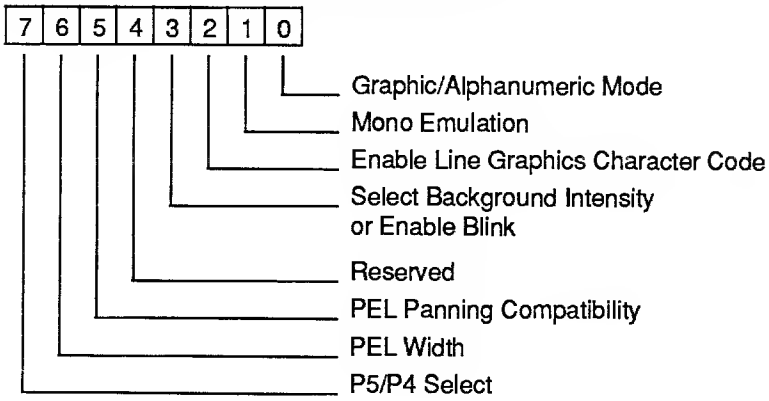
PALETTE REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 0-F



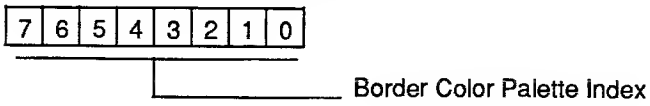
COLOR SELECT REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 14



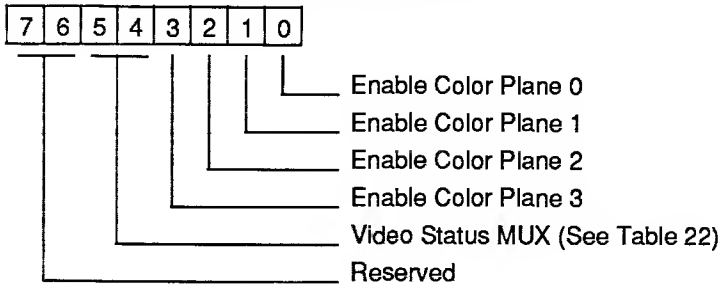
ATTRIBUTE MODE CONTROL REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 10



OVERSCAN COLOR REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 11



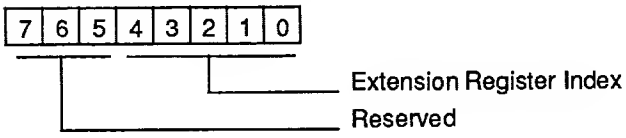
COLOR PLANE ENABLE REGISTER
Address = 03C0 (Write), 03C1 (Read) Index = 12



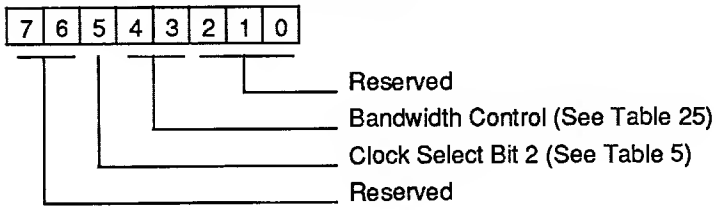
5

EXTENDED REGISTERS

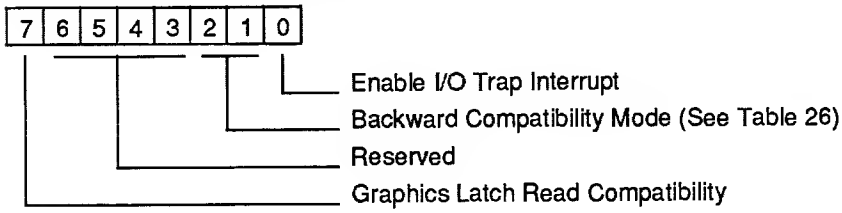
EXTENSION ADDRESS REGISTER
Address = 03DE (Read/Write)



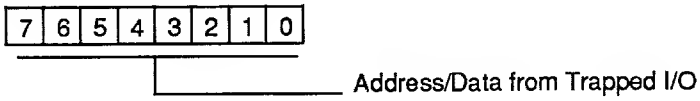
BANDWIDTH CONTROL REGISTER
Address = 03DF Index = D (Read/Write)



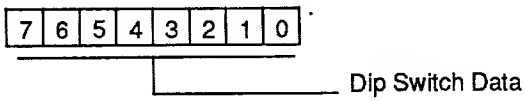
I/O TRAP CONTROL REGISTER
Address = 03DF Index = E (Read/Write)



NMI DATA CACHE REGISTER
Address = 03DF Index = F (Read Only)



DIP SWITCH READ REGISTER
Address = 03DF Index = 10 (Read Only)



AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

I/O READ/WRITE, DAC READ/WRITE, SWITCH READ (See Figures 1, 2, 8, 9 & 10.)

Symbol	Parameter	Min	Max	Units	Conditions
tSU1	Address Setup Time	60	–	ns	
tSU2	ASEL Setup Time	30	–	ns	
tH3	Address Hold Time	0	–	ns	
tH4	ASEL Hold Time	0	–	ns	
t5	Command Pulse Width	200	–	ns	Note
tD6	Write Data Delay	–	80	ns	
tH7	Write Data Hold Time	0	–	ns	
tD8	–EDBUF and –EABUF Delay	–	50	ns	
tD9	Read Data Valid Delay	–	120	ns	
tH10	Read Data Hold Time	10	–	ns	
tD11	Read to DIR Delay	–	45	ns	
tD12	Read to DAC Read Delay	–	50	ns	
tD13	Write to DAC Write Delay	–	50	ns	
tD14	Read to Switch Read Delay	–	40	ns	

Note: 200 ns when VCLK0 = 25 MHz; otherwise, three clocks +80 ns.

5

MEMORY READ/WRITE (See Figures 3 & 4.)

Symbol	Parameter	Min	Max	Units	Conditions
tSU15	Address Setup Time	60	–	ns	
tSU16	ASEL Setup Time	30	–	ns	
tH17	Address Hold Time	0	–	ns	
tH18	ASEL Hold Time	0	–	ns	
tD19	Write Data Delay	–	80	ns	
tH20	Write Data Hold Time	0	–	ns	
tD21	–EDBUF and –EABUF Delay	–	50	ns	
tD22	Read to DIR Delay	–	45	ns	
tD23	Command to CPURDY Low Delay	–	40	ns	
tD24	RD Data from CPURDY High Delay	–	15	ns	
tH25	Valid RD Data Hold Time	–	45	ns	

AC CHARACTERISTICS (Cont.)

DRAM READ/WRITE (See Figures 6 & 7.)

Symbol	Parameter	Min	Max	Units	Conditions
tSU26	Row Address Setup	10	–	ns	
tH27	Row Address Hold Time	.5 tCLK	–	ns	
t28	–RAS Low Time	4 tCLK –10	–	ns	
t29	–RAS High Time	3 tCLK	–	ns	
tSU30	Column Address Setup Time	10	–	ns	
tH31	Column Address Hold Time	tCLK	–	ns	
t32	–CAS Low Time	4.5 tCLK	–	ns	
t33	–CAS High Time	2.5 tCLK –10	–	ns	
tD34	–RAS to –OE Delay	2.5 tCLK –10	–	ns	
tD35	–RAS to –WE Delay	2.5 tCLK –10	–	ns	
tD36	–WE to –RAS High	tCLK	–	ns	
tD37	–RAS to –CAS Reference	1.5 tCLK –10	–	ns	
tSU38	Data to –WE Setup Time	10	–	ns	
tH39	Data to –WE Hold Time	tCLK	–	ns	

CLOCK AND VIDEO (See Figure 5.)

Symbol	Parameter	Min	Max	Units	Conditions
tCLK	CLKIN Cycle	28	–	ns	
tD40	P0-P7 Delay	–	80	ns	
tD41	–BLANK Delay	–	80	ns	
tD42	HSYNC/VSYNC Delay	–	80	ns	
tD43	CLKIN to PCLK Delay	–	60	ns	

TIMING DIAGRAMS

FIGURE 1. I/O READ TIMING

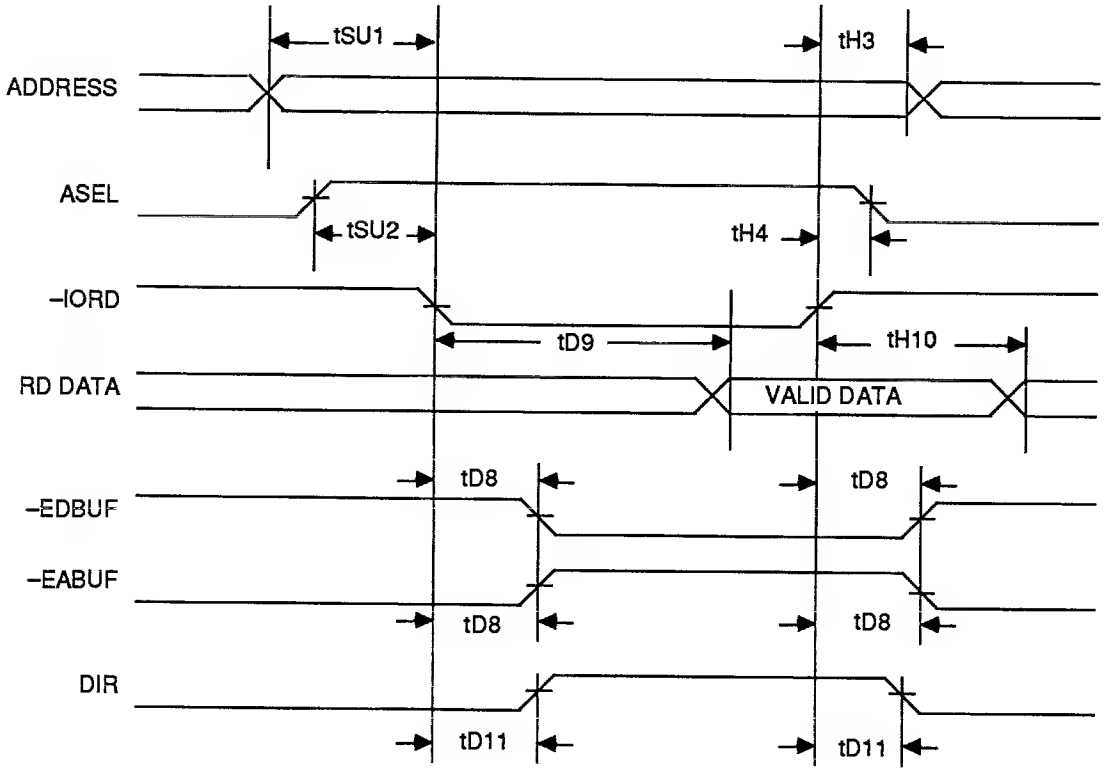
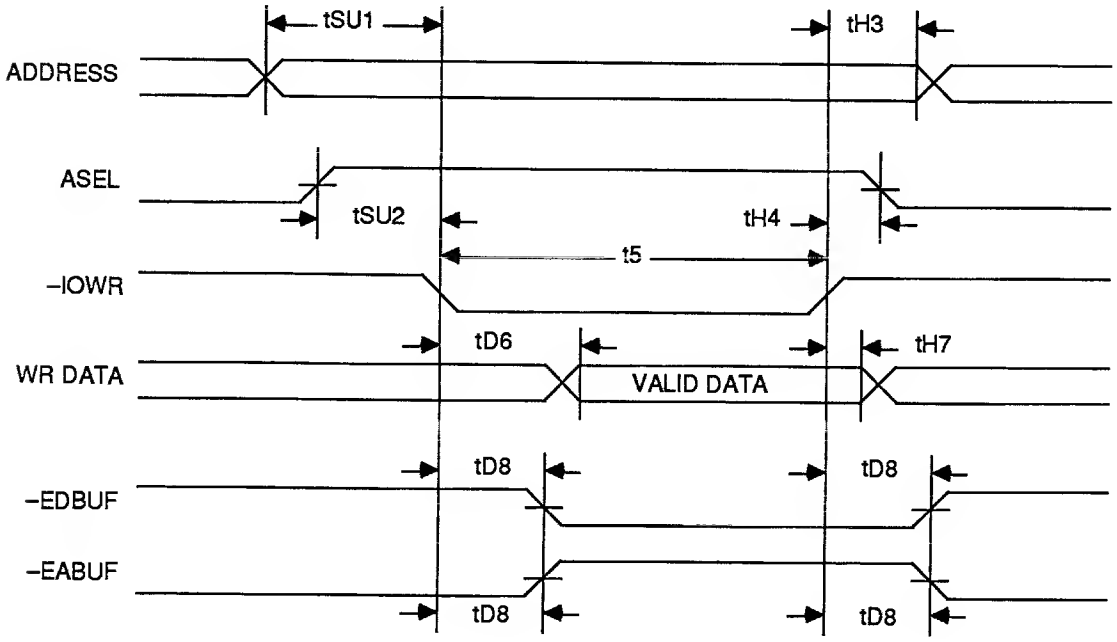


FIGURE 2. I/O WRITE TIMING



5

FIGURE 3. MEMORY READ TIMING

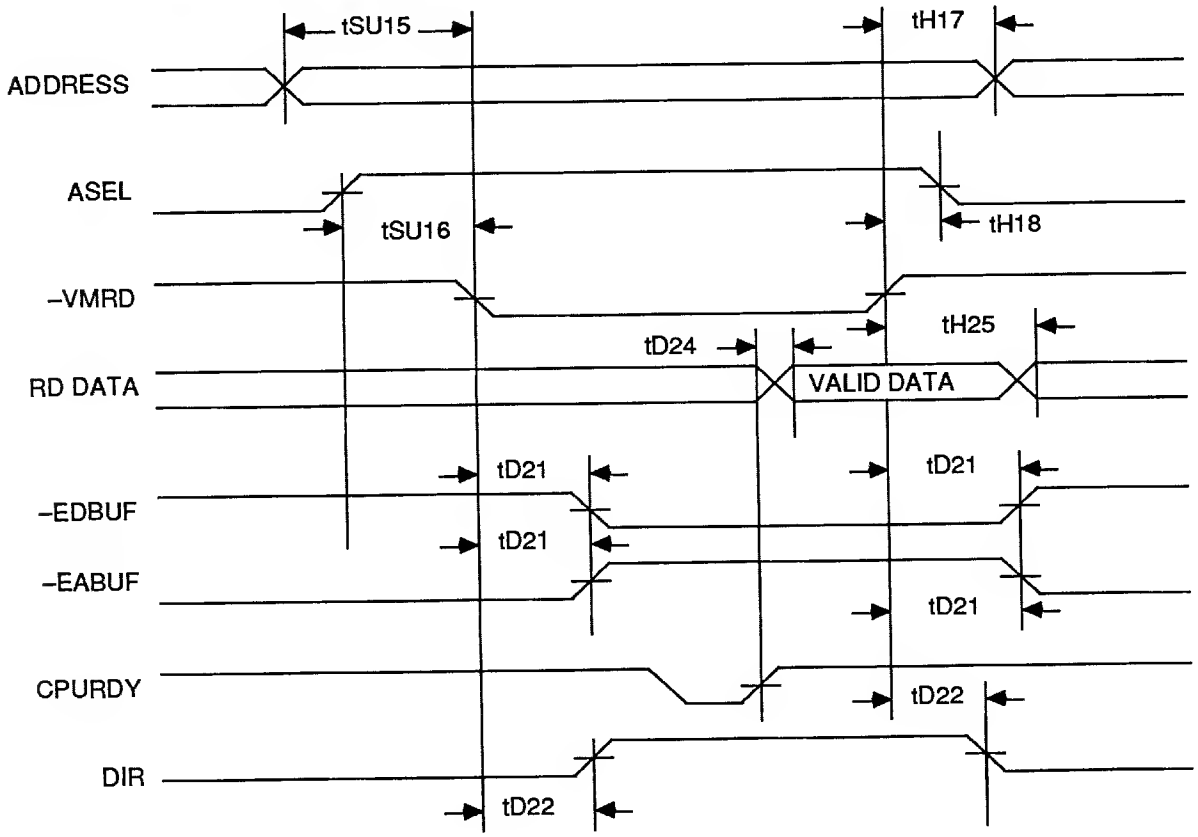


FIGURE 4. MEMORY WRITE TIMING

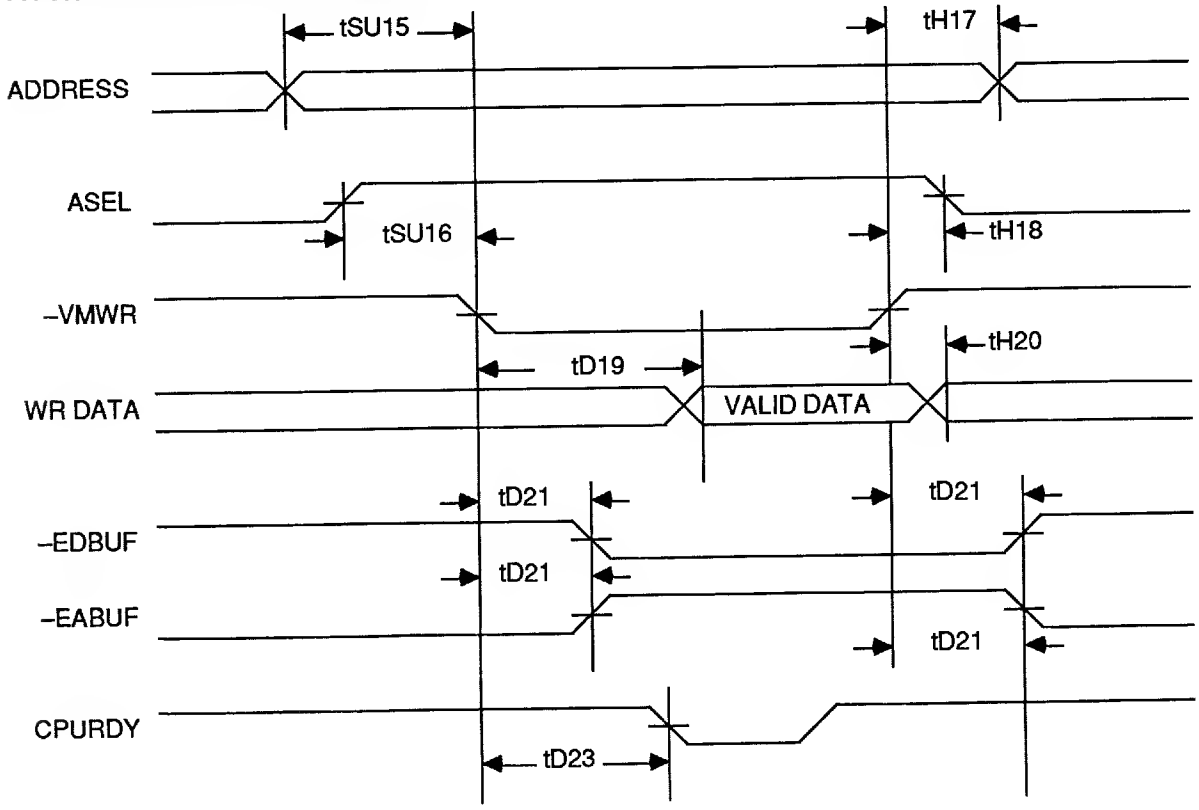


FIGURE 5. CLOCK AND VIDEO TIMING

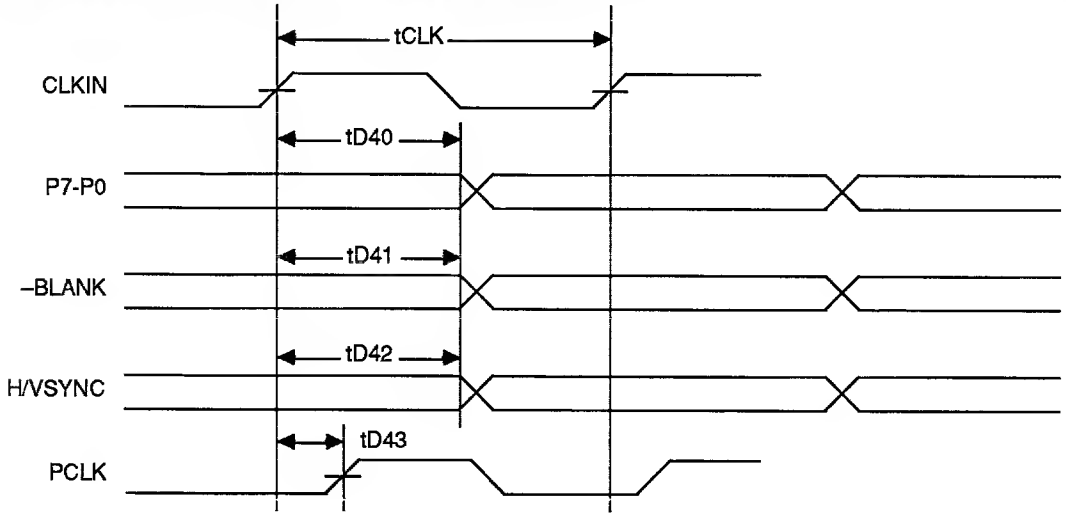


FIGURE 6. DRAM READ TIMING

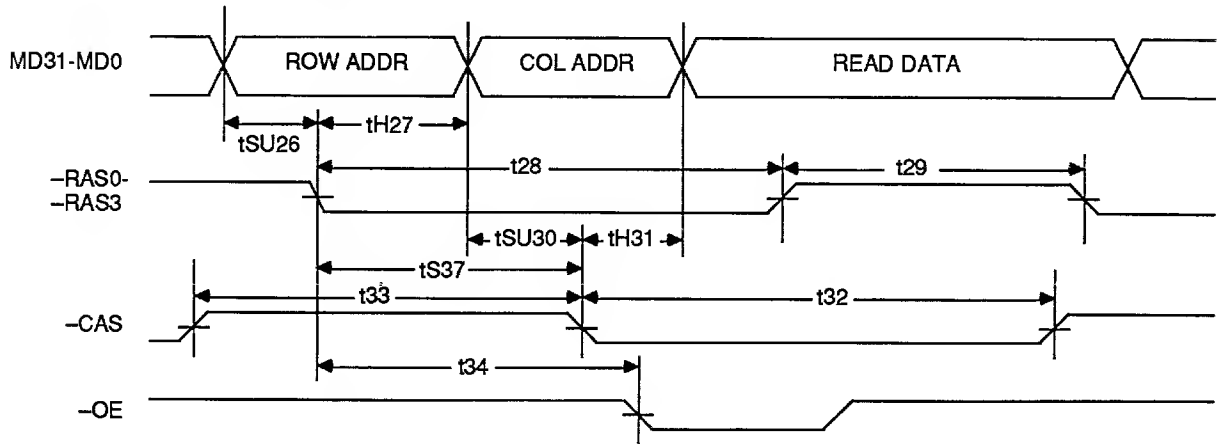


FIGURE 7. DRAM WRITE TIMING

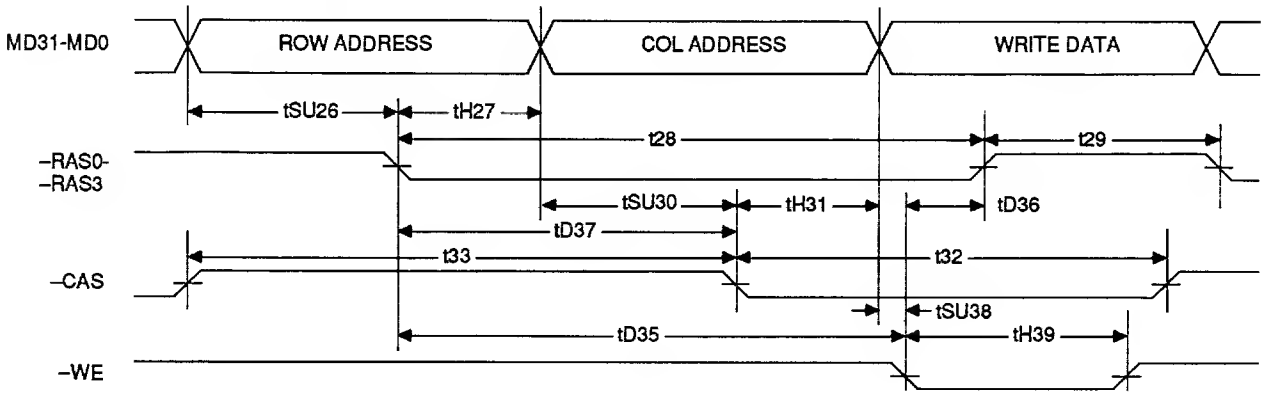


FIGURE 8. DAC READ TIMING

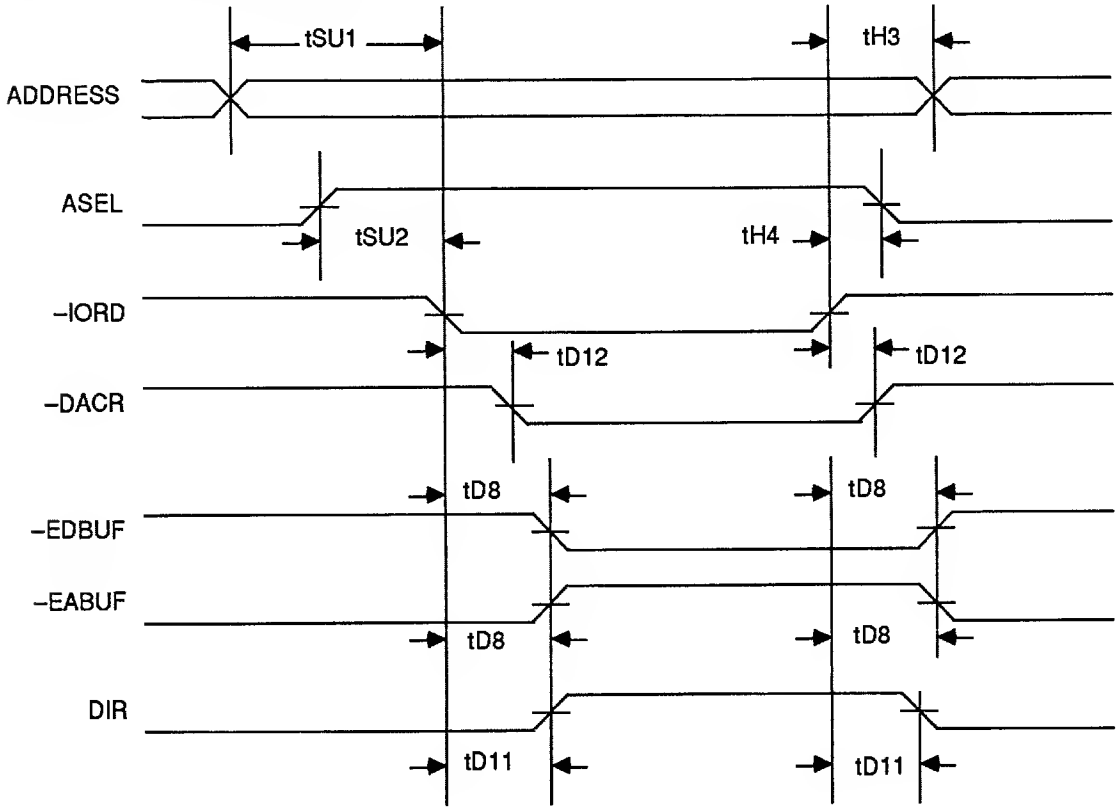


FIGURE 9. DAC WRITE TIMING

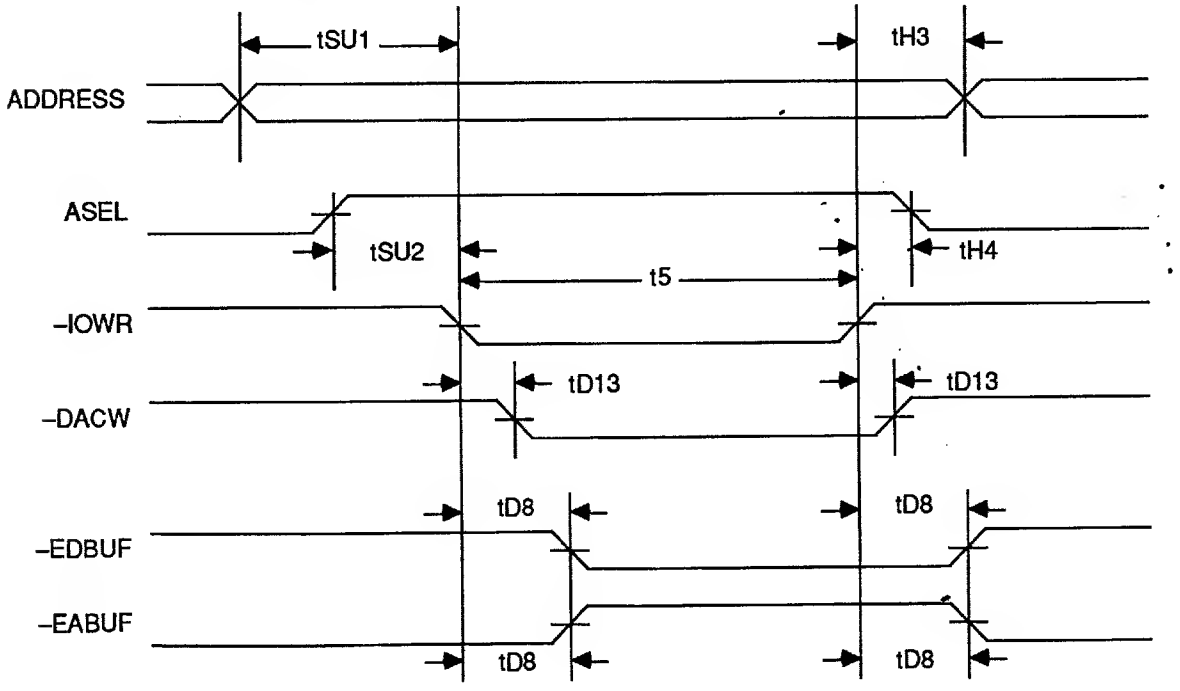
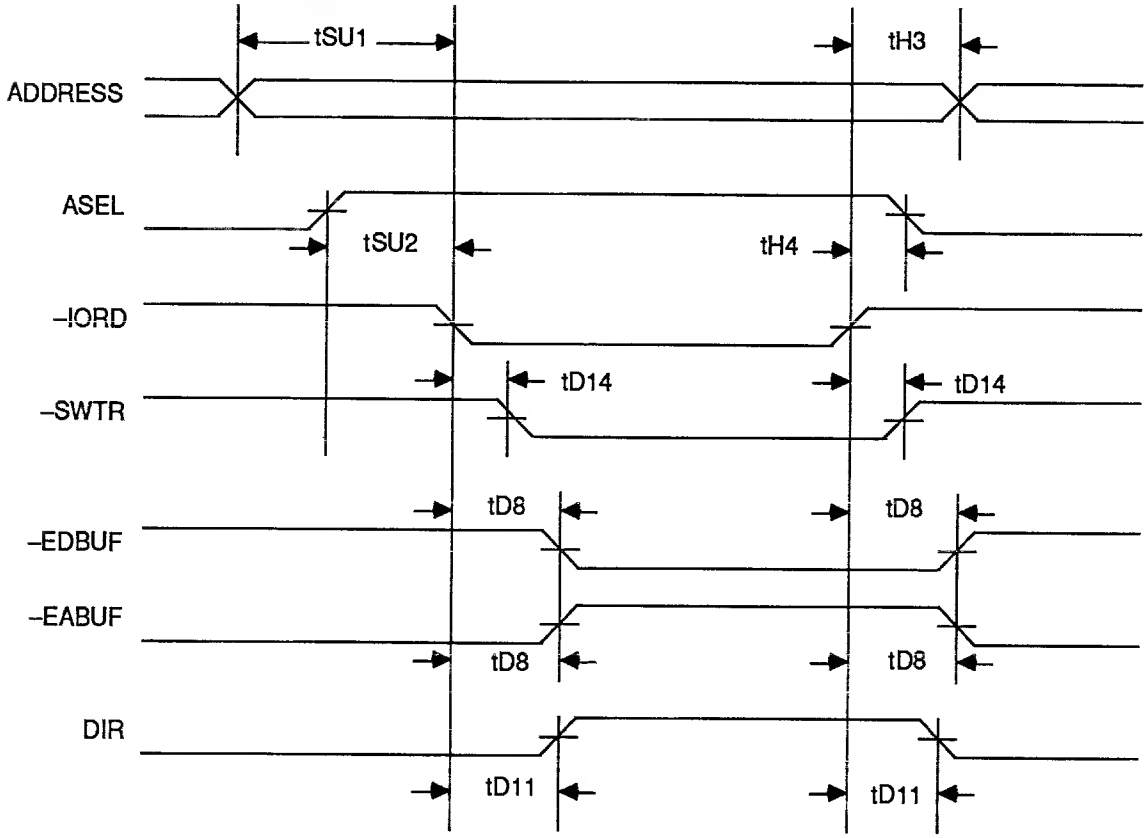


FIGURE 10. SWITCH READ TIMING



5

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–40°C to +125°C
Supply Voltage to Ground Potential	–0.5 V to VCC +6.0 V
Applied Input Voltage	–0.5 V to VCC +0.5 V
DC Input Current	± 20 mA
Lead Temperature	300°C

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%, GND = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
VIH	Input High Voltage	2.0	VCC	V	VCC = 5.25 V
VIL	Input Low Voltage	–0.5	0.8	V	VCC = 5.25 V
VOH	Output High Voltage	2.4	–	V	IOH (See Note 2)
VOL	Output Low Voltage	–	0.4	V	IOL (See Note 1)
IIN	Input Leakage Current	–10	10	µA	VIN = VCC/GND
IOZ	3-State Output Leakage Current	–10	10	µA	VOUT = VCC/GND
IDD	IDD Dynamic Current	–	80	mA	VCC = 5.25 V

Note 1: 2 mA Output Pads: –EABUF, –EDBUF, DIR, –CRTINT, –NMI, CPURDY, –SWTR, HSYNC, VSYNC, –BLANK, –DACR, –DACW, PCLK
4 mA Output Pads: P7-P0, DA7-DA0, MD31-MD0.
8 mA Output Pads: –RAS0—RAS3, –WE
12 mA Output Pads: –OE
20 mA Output Pads: –CAS

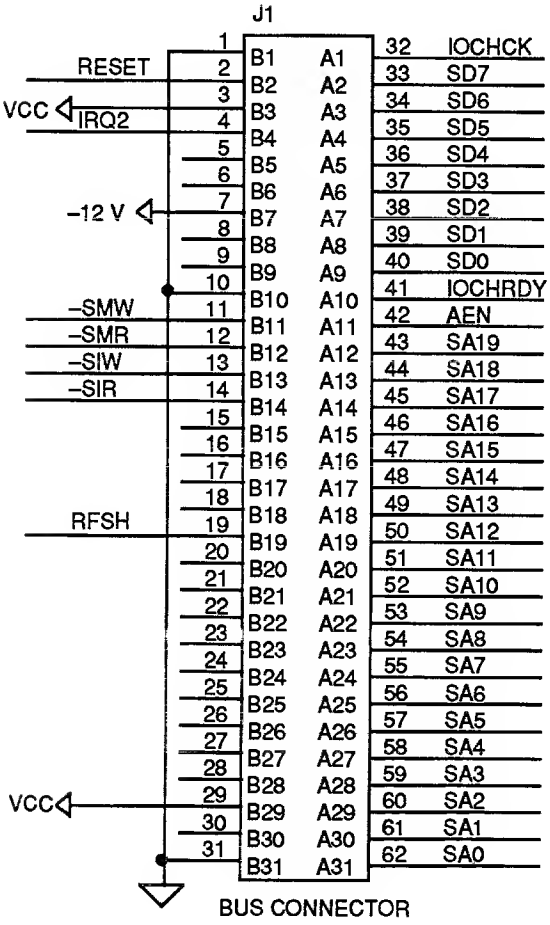
Note 2: –200 µA Output Pads: –EABUF, –EDBUF, DIR, –CRTINT, –NMI, CPURDY, –SWTR, HSYNC, VSYNC, –BLANK, –DACR, –DACW, P7-P0, DA7-DA0, MD31-MD0, PCLK
–1 mA Output Pads: –RAS0, –RAS1, –RAS2, –RAS3, –WE
–3.3 mA Output Pads: –OE, –CAS

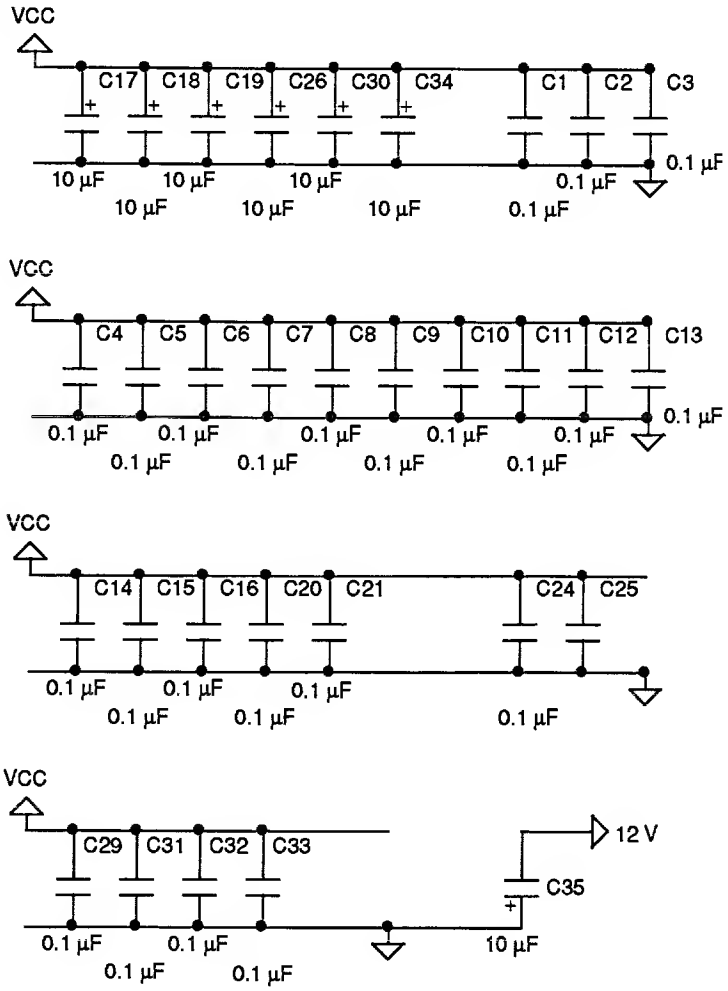
VGA ADD-ON CARD

VLSI Logic Products group has made available an XT-compatible evaluation board for the VL82C037. The board has a 15-pin connector for connecting a stand VGA analog monitor, and a 9-pin connector for connecting older style digital monitors. The DIP switch bank is used to configure the board for the type of monitor being used, according to the following table:

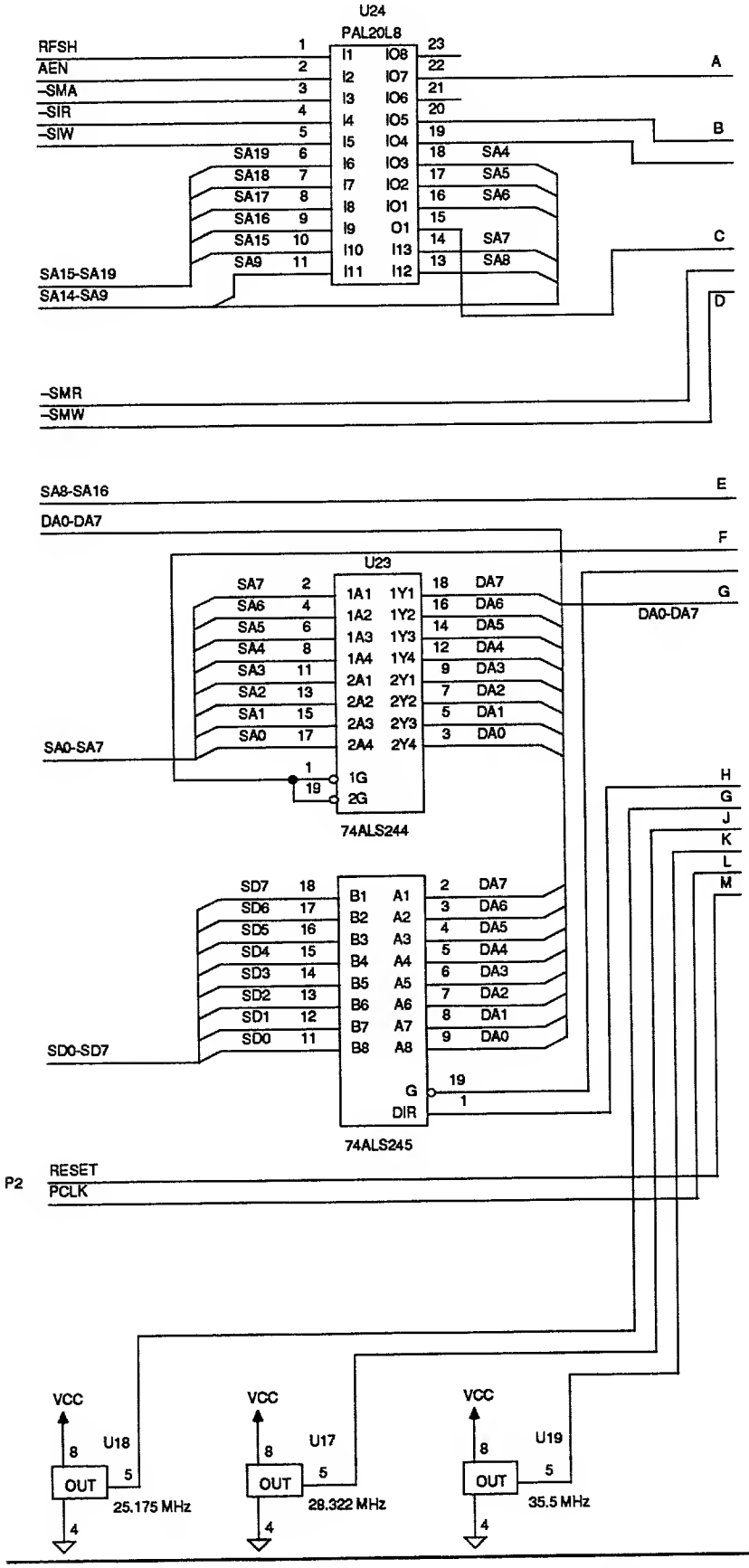
The board is capable of supporting non-standard video modes which can be set using a program called VGAMODE.EXE, which is available on request. The non-standard text modes supported are 132 columns by 25 rows, and 132 columns by 43 rows. The 132 x 43 mode requires a high speed multisync monitor. The 800 x 600 16 color graphics mode requires 100 ns DRAMs and a 36 MHz clock, and is not supported on this board. Other software is available which demonstrates hardware panning and a 160 column by 50 row text display mode.

SW4	SW3	SW2	SW1	MONITOR
off	x	x	x	IBM Analog Monitor (Mono or Color)
on	off	off	off	Digital Monochrome
on	off	off	on	Digital CGA
on	off	on	off	Digital EGA
on	off	on	on	NEC MultiSync or Compatible (Analog)
on	on	off	off	NEC MultiSync Plus (Analog)
on	on	off	on	Reserved
on	on	on	off	Reserved
on	on	on	on	Reserved

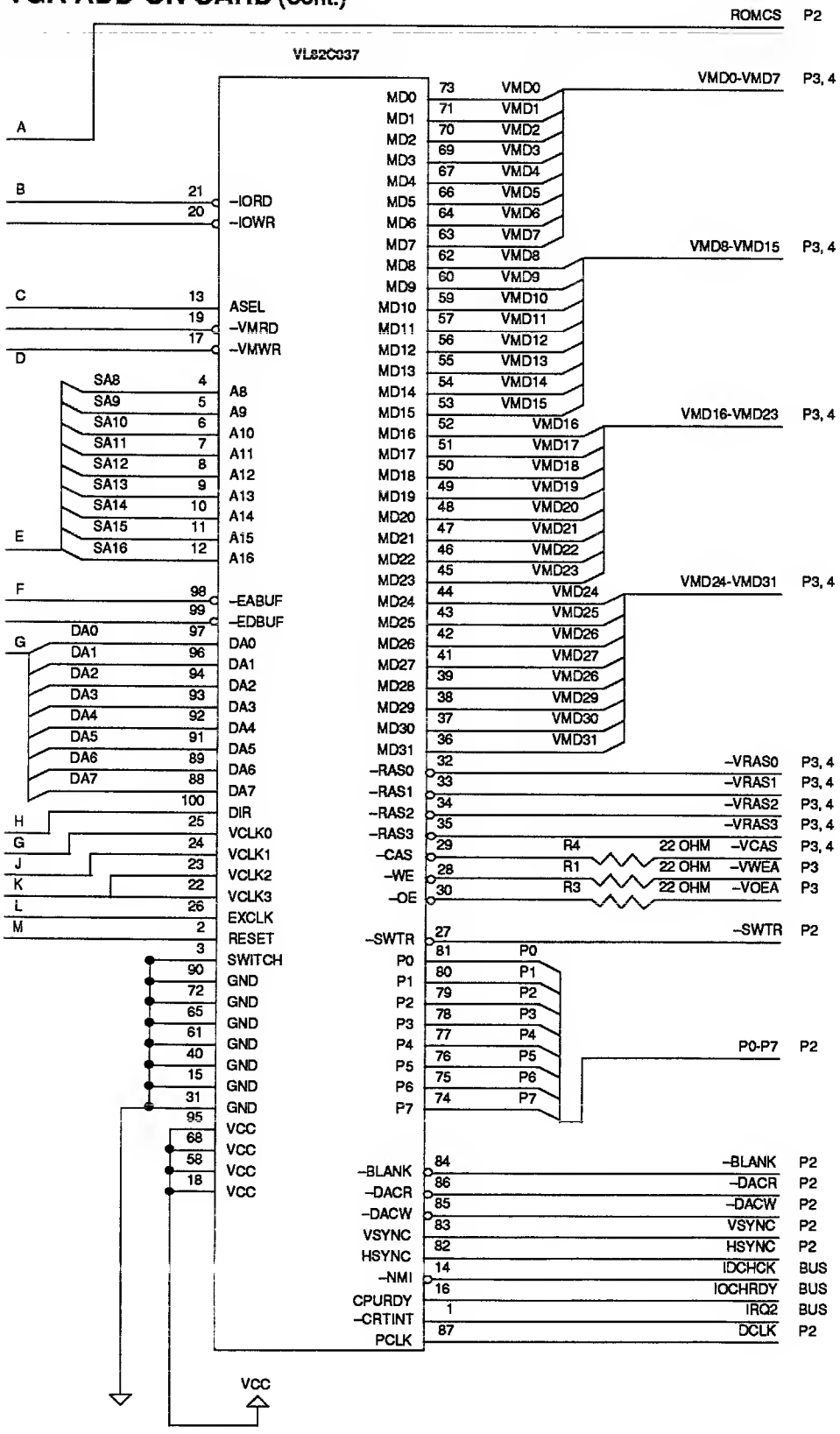




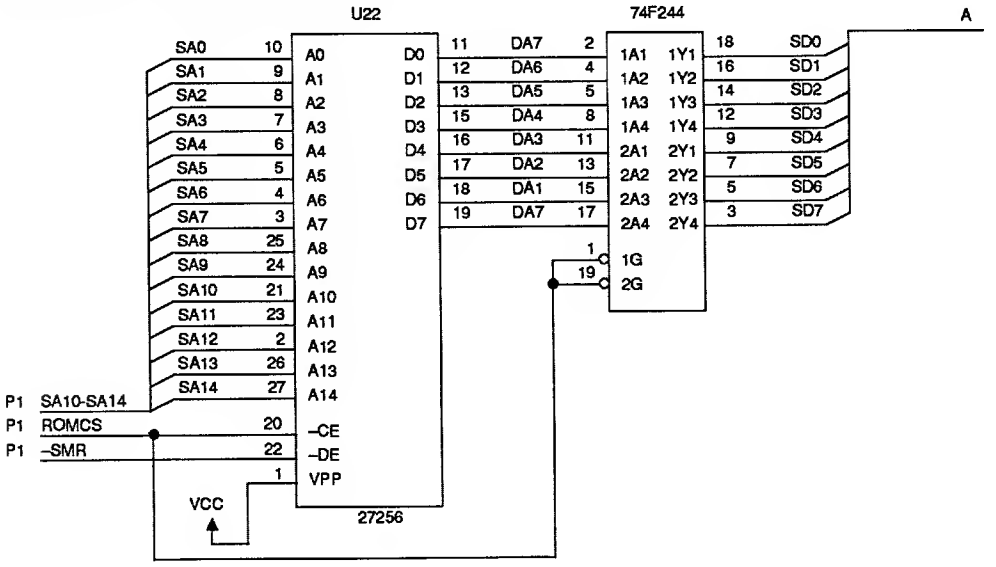
VGA ADD-ON CARD (Cont.)

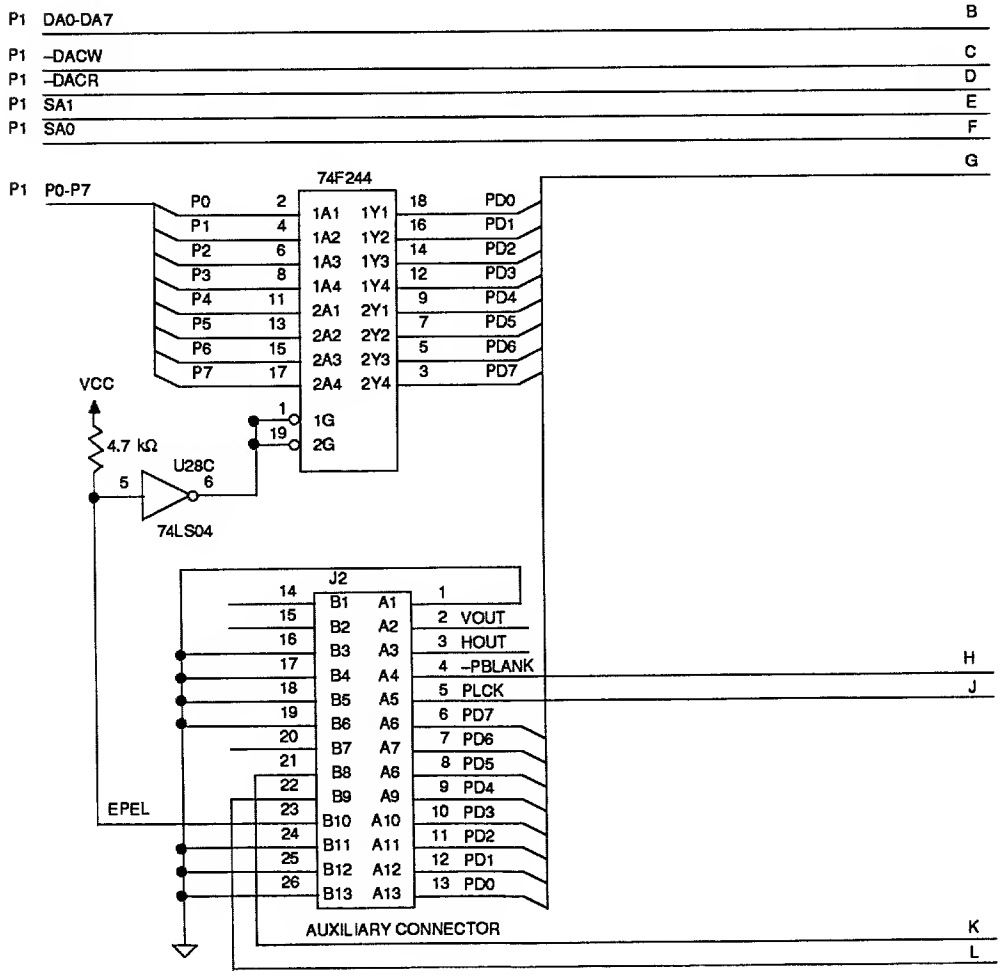


VGA ADD-ON CARD (Cont.)

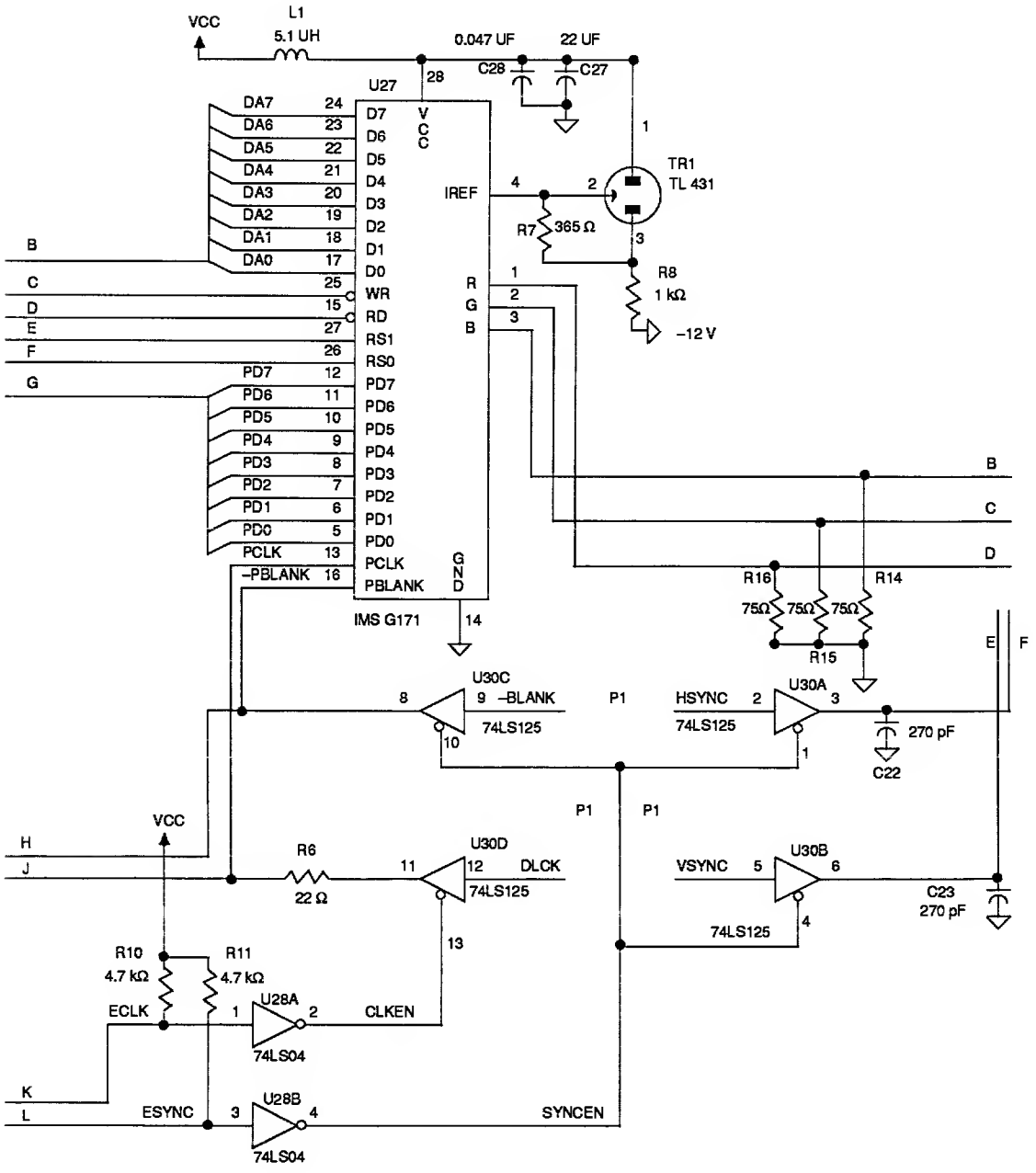


VGA ADD-ON CARD (Cont.)



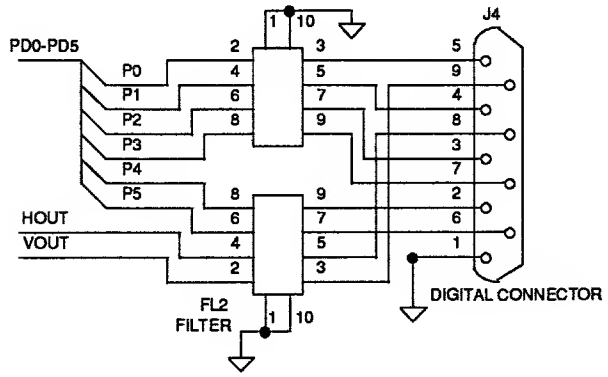


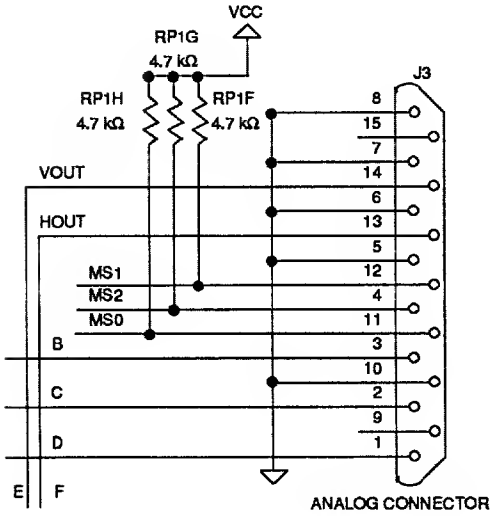
VGA ADD-ON CARD (Cont.)

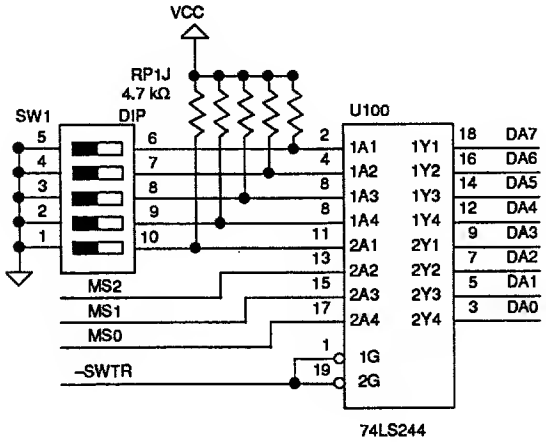


VGA ADD-ON CARD (Cont.)

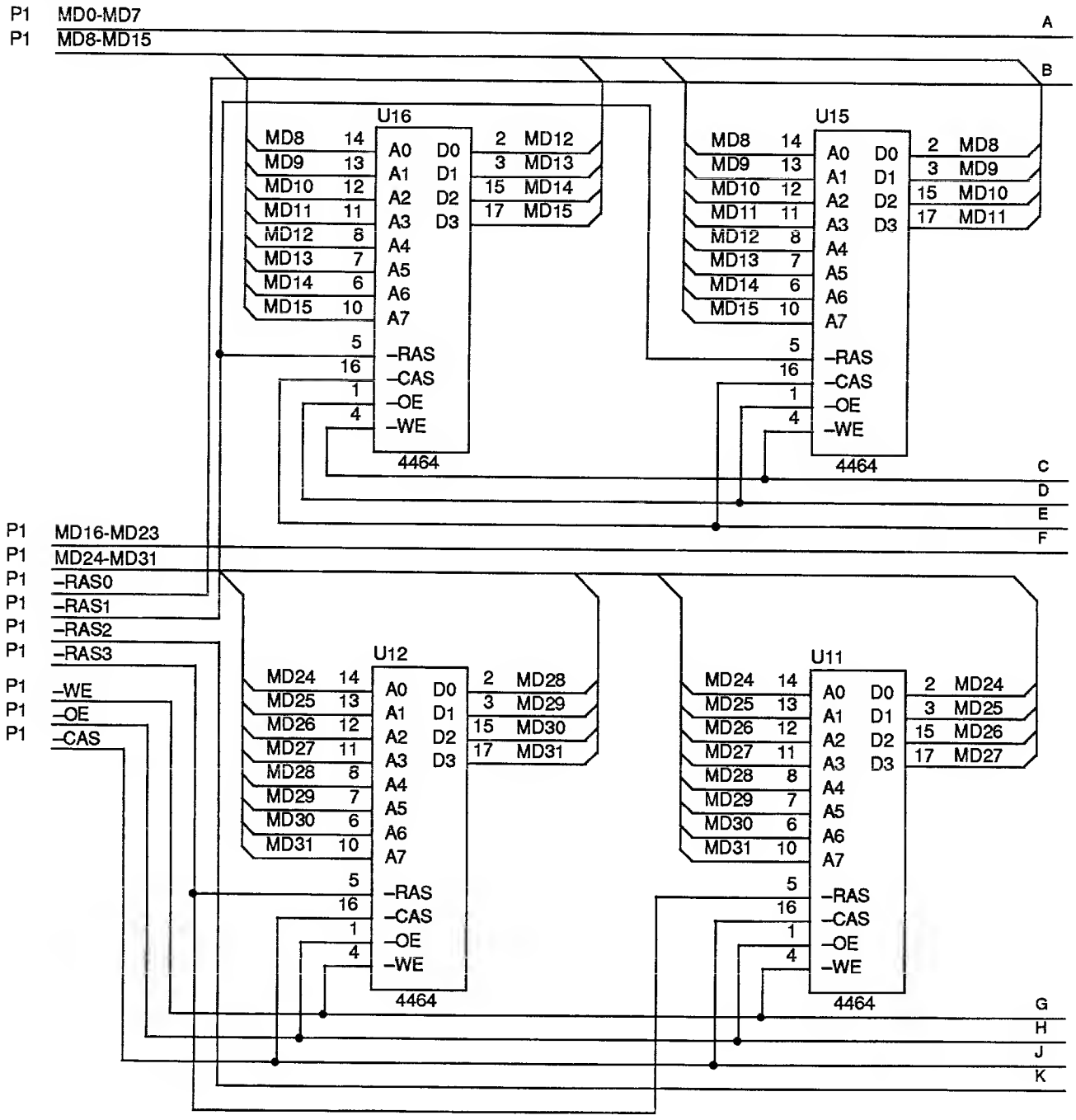
A SD0-SD7 P1



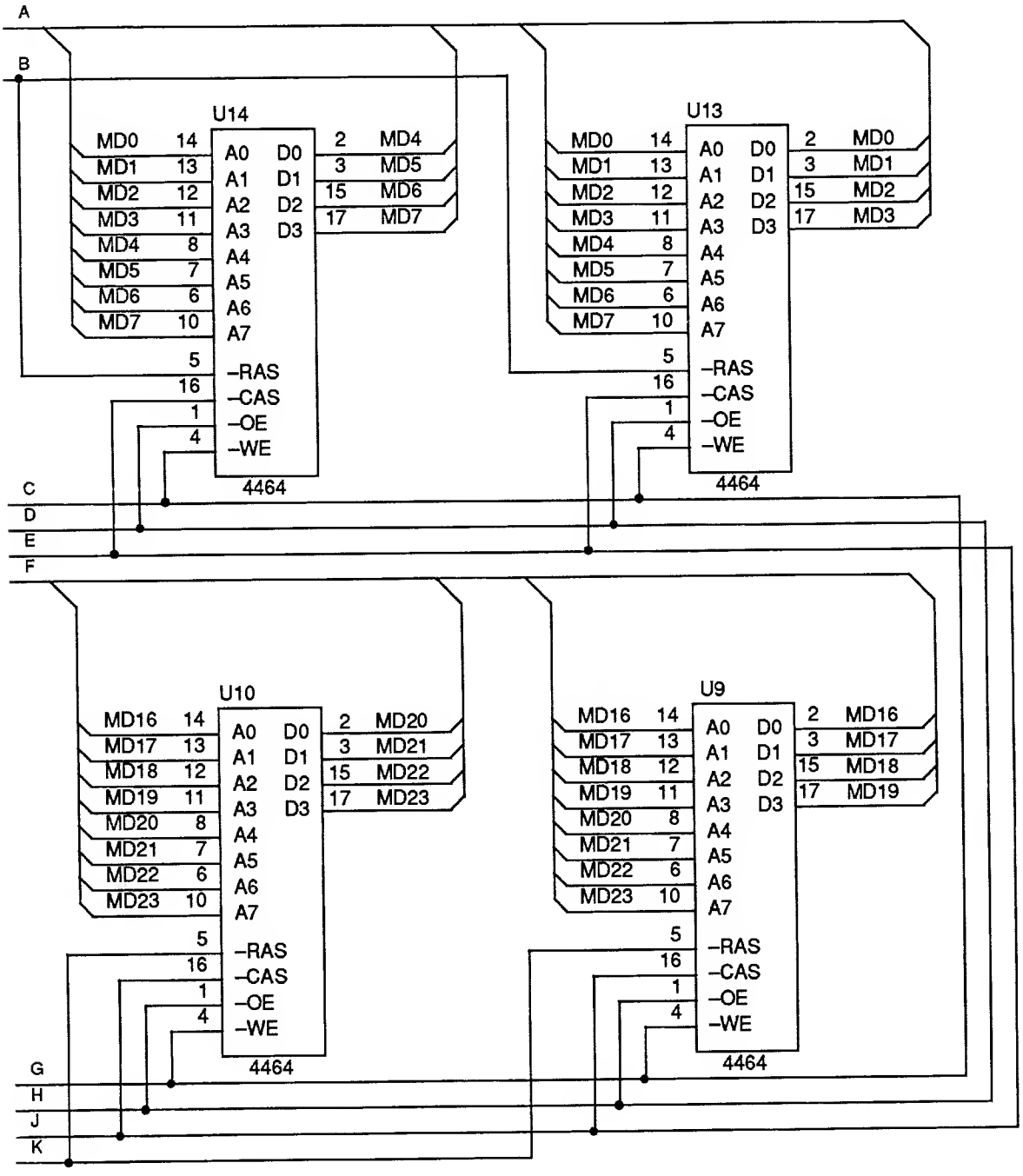




VGA ADD-ON CARD - FIRST BANK OF MEMORY



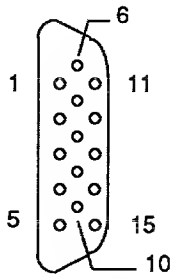
VGA ADD-ON CARD - FIRST BANK OF MEMORY (Cont.)



DISPLAY CONNECTOR

Analog Monitor Connector

—> 15-pin D-shell Display Connector

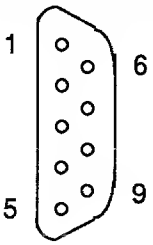


Pin Number	I/O	Output	Monochrome	Color
1	O	Red	No Pin	Red
2	O	Green	Mono	Green
3	O	Blue	No Pin	Blue
4	NA	Reserved	No Pin	No Pin
5	NA	Digital G	Self Test	Self Test
6	NA	Red Rtn	Key Pin	Red Rtn
7	NA	Green Rtn	Mono Rtn	Green Rtn
8	NA	Blue Rtn	No Pin	Blue Rtn
9	NA	Plug	No Pin	No Pin
10	NA	Digital G	Digital G	Digital G
11	NA	Reserved	No Pin	Digital G
12	NA	Reserved	Digital G	No Pin
13	O	HSYNC	HSYNC	HSYNC
14	O	VSYNC	VSYNC	VSYNC
15	NA	Reserved	No Pin	No Pin

Note: Red Rtn, Green Rtn, Blue Rtn = Analog Grounds
Digital G = Digital ground for sync returns and self test

Digital Monitor Connector

—> 9-pin D-shell Display Connector



Pin Number	Signal Description
1	Ground
2	Secondary Red
3	Primary Red
4	Primary Green
5	Primary Blue
6	Secondary Green/Intensity
7	Secondary Blue/Mono Video
8	Horizontal Retrace (Hsync)
9	Vertical Retrace (Vsync)

5

AUXILIARY VIDEO CONNECTOR

Pin Number	Signal Description
A1	Ground
A2	VSYNC
A3	HSYNC
A4	Blank
A5	PCLK
A6	P7
A7	P6
A8	P5
A9	P4
A10	P3
A11	P4
A12	P1
A13	P0
B1	Reserved
B2	Reserved
B3	Ground
B4	Ground
B5	Ground
B6	Ground
B7	Reserved
B8	ECLK
B9	ESYNC
B10	EPEL
B11	Ground
B12	Ground
B13	Ground

PARTS LIST

Resistors

Description	Quantity	Discrete
22 Ohm	4	R1, R3, R4, R6
75 Ohm	3	R14, R15, R16
365 Ohm	1	R7
1K Ohm	1	R8
4.7K Ohm	3	R10, R11, R12

Resistor Network

Description	Quantity	Discrete
4.7K Ohm 10-Pin	1	RP1

Capacitors

Description	Quantity	Discrete
0.1 µF DCAP	17	C8, C9, C10, C11, C12, C13, C14, C15, C16, C20, C21, C24, C25, C29, C31, C32, C33
10 µF TCAP	7	C17, C18, C19, C26, C30, C34, C35
0.047 µF DCAP	1	C28
270 pF DCAP	2	C22, C23

Semiconductors

Description	Quantity	Discrete
74ALS245	1	U29
74ALS244	1	U23
74LS244	2	U26, U100
74F244	1	U25
4464-10 DRAM	8	U9, U10, U11, U12, U13, U14, U15, U16
OTI-036/ IMS G171 DAC	1	U27
27256-200 EPROM	1	U22
PAL20L8-15	1	U24
VL82C037	1	U21

Crystal Oscillators

Description	Quantity	Discrete
25.175 MHz	1	U18
28.322 MHz	1	U17
35.5 MHz	1	U19

Connectors

Description	Quantity	Discrete
15-Pin D-shell	1	J3
9-Pin D-shell	1	J4

Miscellaneous

Description	Quantity	Discrete
TL431 Volt. Regulator	1	TR1
10-Pin RC Network	2	FL1, FL2
5.1 µH Inductor	1	L1
4-position DIP Switch	1	SW1

PAL EQUATION (FOR THE ADD-ON CARD)

A 15 ns 20L8 PAL is required for interface between bus connector and VGA chip. The equation of the PAL is listed below.

PAL20L8
VGA BOARD

```
/RFSH AEN /SMRN /SIRN /SIWN SA19 SA18 SA17 SA16 SA15 SA9 GND
SA8 SA7 /ASEL SA6 SA5 SA4 /IOWR /IORD /SEL0 /ROMCS NC VCC

SEL0 = SA19 * /SA18 * SA17 * /RFSH +
       SA9 * SA8 * SA7 * SA6 * /SA5 * /RFSH * /AEN * SIWN +
       SA9 * SA8 * SA7 * SA6 * /SA5 * /RFSH * /AEN * SIRN +
       SA9 * SA8 * SA7 * /SA6 * SA5 * SA4 * /RFSH * /AEN * SIWN +
       SA9 * SA8 * SA7 * /SA6 * SA5 * SA4 * /RFSH * /AEN * SIRN
ASEL = /SEL0
ROMCS = SA19 * SA18 * /SA17 * /SA16 * /SA15 * /RFSH * SMRN
IORD = SIRN * /AEN
IOWR = SIWN * /AEN
```

VLSI TECHNOLOGY, INC.

SECTION 6

PERIPHERALS

Logic Products Division


VLSI TECHNOLOGY, INC.

VLSI TECHNOLOGY, INC.

VL16C450 • VL82C50A • VL82C50

ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- Full double buffering
- Independent control of transmit, receive, line status and data set interrupts
- Modem control signals include –CTS, –RTS, –DSR, –DTR, –RI and –DCD
- Programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd-, or no-parity bit generation and detection
  - 1-, 1 1/2- or 2-stop bit generation
  - Baud rate generation (DC to 56K baud)
- Full status reporting capabilities
- Three-state TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTIONS

The VL16C450 is an asynchronous communications element (ACE) that is functionally equivalent to the VL82C50A, but is an improved specification version of that part. The improved specifications provide ensured compatibility with state-of-the-art CPUs.

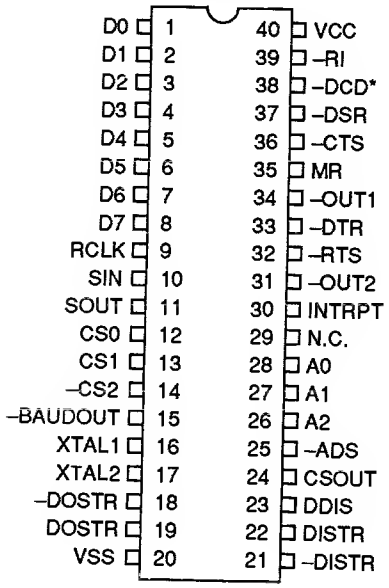
The VL16C450, VL82C50A, and VL82C50 ACEs serve as serial data input/output interfaces in microcomputer systems. They perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing, or break interrupt.

A programmable baud rate generation is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

The VLSI family of ACEs is available packaged in a plastic leaded chip carrier as well as a plastic DIP.

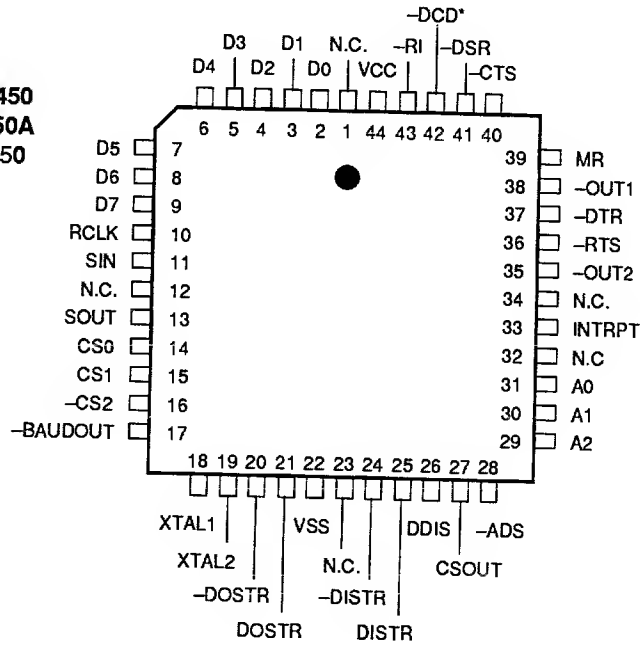
PIN DIAGRAMS

VL16C450
VL82C50A
VL82C50



*On the VL82C50, Pin 38 (Pin 42 on the PLCC package) is also called –RLSD.

VL16C450
VL82C50A
VL82C50



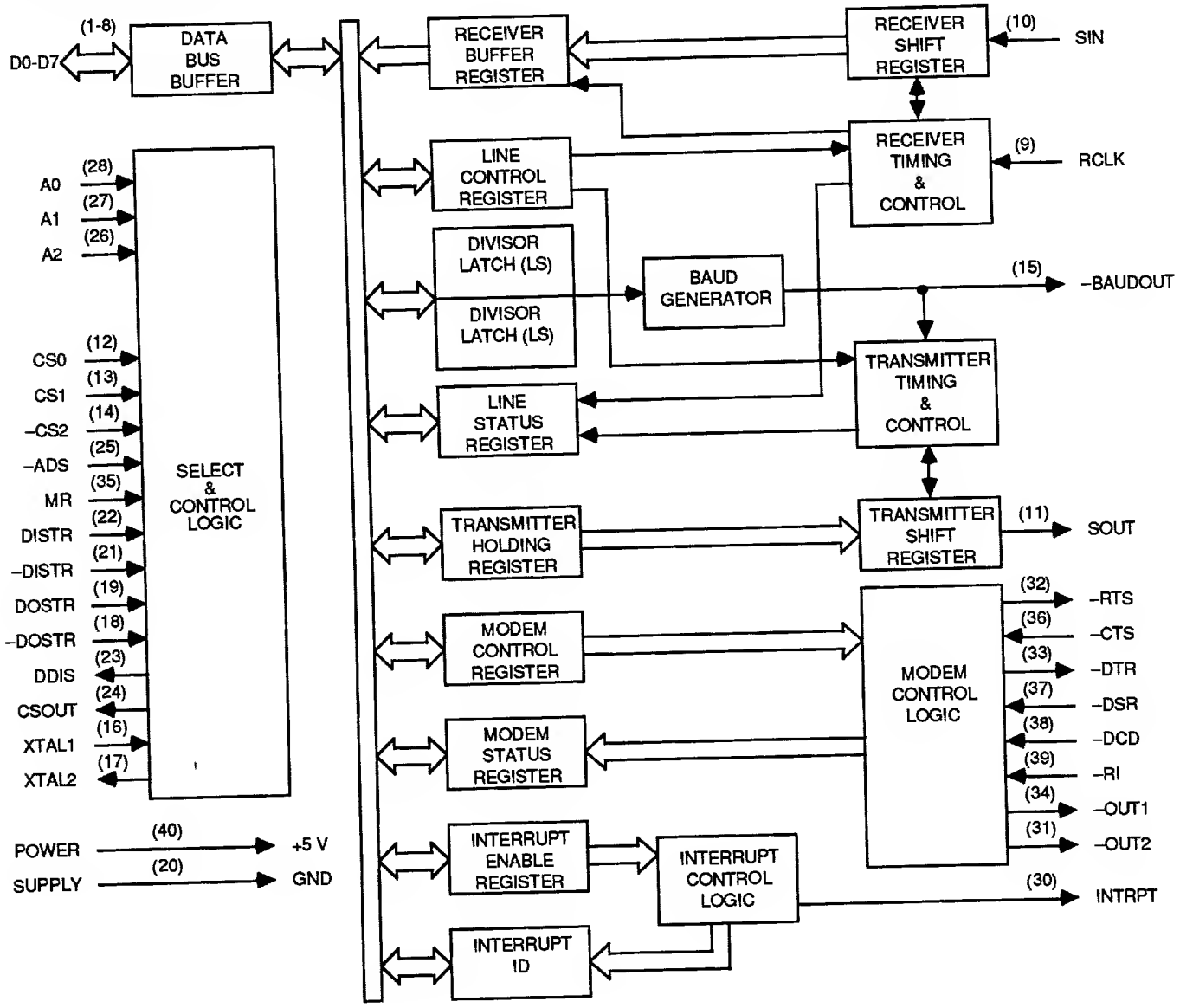
ORDER INFORMATION

Part Number	Clock Frequency	Package
VL16C450-PC VL16C450-QC	3.1 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)
VL82C50A-PC VL82C50A-QC	3.1 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)
VL82C50-PC VL82C50-QC	3.1 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

6

BLOCK DIAGRAM



Note: Applicable pin numbers (DIP) are included within parentheses.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (DIP)	Signal Type	Signal Description
D0-D7	1-8	I/O	Data Bits 0 through 7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the ACE and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
RCLK	9	I	Receive Clock Input - The external clock input to the ACE receiver logic (16X SIN data rate).
SIN	10	I	Serial Data Input - The serial data input moves information from the communication line or modem to the ACE receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data input is disabled when operating in the Loop Mode.
SOUT	11	O	Serial Data Output - This line is the serial data output from the ACE's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). SOUT is held in the mark condition when the transmitter is disabled, reset is true, the Transmitter Register is empty, or when in the Loop Mode.
CS0, CS1, –CS2	12-14	I	Chip Selects - The Chip Select inputs act as an enable for the device. When –CS2 is low and CS0 and CS1 are both high, the chip is selected.
–BAUDOUT	15	O	Baud Rate Output - This output signal for the transmitter section is equal to the internal reference frequency, divided by the selected divisor.
XTAL1	16	I	Crystal Input Pin 1 - Input for external timing reference input or pin of crystal (See Basic Configuration).
XTAL2	17	I	Crystal Input Pin 2 - Input for pin of crystal (See Basic Configuration).
–DOSTR	18	I	Write Strobe - This is an active low input which causes data from the data bus (D0-D7) to be input to the ACE.
DOSTR	19	I	Write Strobe - Same as –DOSTR, but uses an active high input.
VSS	20		Ground (0 V).
–DISTR	21	I	Read Strobe - This is an active low input which causes the ACE to output data to the data bus (D0-D7).
DISTR	22	I	Read Strobe - Same as –DISTR, but uses an active high input.
DDIS	23	O	Driver Disable - This pin goes low whenever the microprocessor is reading data from the ACE. This signal may be used to disable an external transceiver.
CSOUT	24	O	Chip Select Out - A high on this pin indicates that the chip has been selected by the chip select input pins.
–ADS	25	I	Address Strobe Input - When this pin is low, the state of the Register Select and Chip Select pins is latched internally.
A0-A2	28-26	I	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations.
NC	29		No Connection.
INTRPT	30	O	Interrupt Output - This pin goes high (when enabled by the Interrupt Enable Register) whenever a Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty, or Modem Status condition is detected.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number (DIP)	Signal Type	Signal Description
–OUT2	31	O	Output 2 - User defined output that can be set to an active low by programming bit 3 of the Modem Control Register to a high level. This signal is cleared (high) by writing a logic 0 to the OUT2 bit (MCR) or whenever a reset occurs.
–RTS	32	O	Request to Send - The –RTS pin is set low by writing a logic 1 to MCR bit 1 of the ACE's Modem Control Register. The –RTS pin is reset high by reset. A low on the –RTS pin indicates that the ACE has data ready to transmit.
–DTR	33	O	Data Terminal Ready - The –DTR pin can be set (low) by writing a logic 1 to MCR, Modem Control Register bit 0 of the ACE. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR) or whenever a reset occurs. When active (low), the –DTR pin indicates that the ACE is ready to receive data.
–OUT1	34	O	Output 1 - A user defined output that can be set to an active low by programming bit 2 of the Modem Control Register to a high level. This signal is cleared (high) by writing a logic 0 to the OUT1 bit (MCR) or whenever a reset occurs.
MR	35	I	Master Reset - When high, the reset input forces the ACE into an idle mode in which all data activities are suspended. The Modem Control Register (MCR) along with its output, is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume activities.
–CTS	36	I	Clear to Send - The logical state of the –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of the ACE. A change of state of the –CTS pin, since the previous reading of the MSR, causes the setting of DCTS in the Modem Status Register.
–DSR	37	I	Data Set Ready - The logical state of the –DSR pin is reflected in MSR(5) of the Modem Status Register. DDSR MSR(1) indicates whether the –DSR pin has changed state since the previous reading of the MSR.
–DCD (–RLSD)	38	I	Data Carrier Detect (Receive Line Signal Detect) - –DCD (–RLSD) is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD or RLSD) of the Modem Status Register. MSR(3) (DDCD or DRLSD) of the Modem Status Register indicates whether the –DCD (–RLSD) input has changed since the previous reading of the MSR. –DCD (–RLSD) has no effect on the receiver.
–RI	39	I	Ring Indicator Input - The –RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the ACE. The Modem Status Register output TERI MSR(2) indicates whether the RI input has changed from high to low since the previous reading of the MSR.
VCC	40		Power Supply - The power supply requirement is 5 V ±5%.

REGISTERS

Three types of internal registers are used in the serial channel of each ACE. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double-buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

LINE CONTROL REGISTER

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read. The contents of the LCR are described below in Figure 1.

LCR(0) and LCR(1) Word Length Select bit 1: The number of bits in each serial character is programmed as shown in Figure 1.

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver always checks for one stop bit.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This allows forced parity to a known state and the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic 0. The Break Control bit acts only on SOUT and does not effect the transmitter logic. If the following sequence is used, no invalid characters will be transmitted because of the break.

1. Load all "0"s pad character in response to THRE.
2. Set the break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), then clear the break when the normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB); LCR(7) must be set high (logic 1) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

LINE STATUS REGISTER

The Line Status Register (LSR) is a single register that provides status indications.

The Line Status Register shown in Table 2 is described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

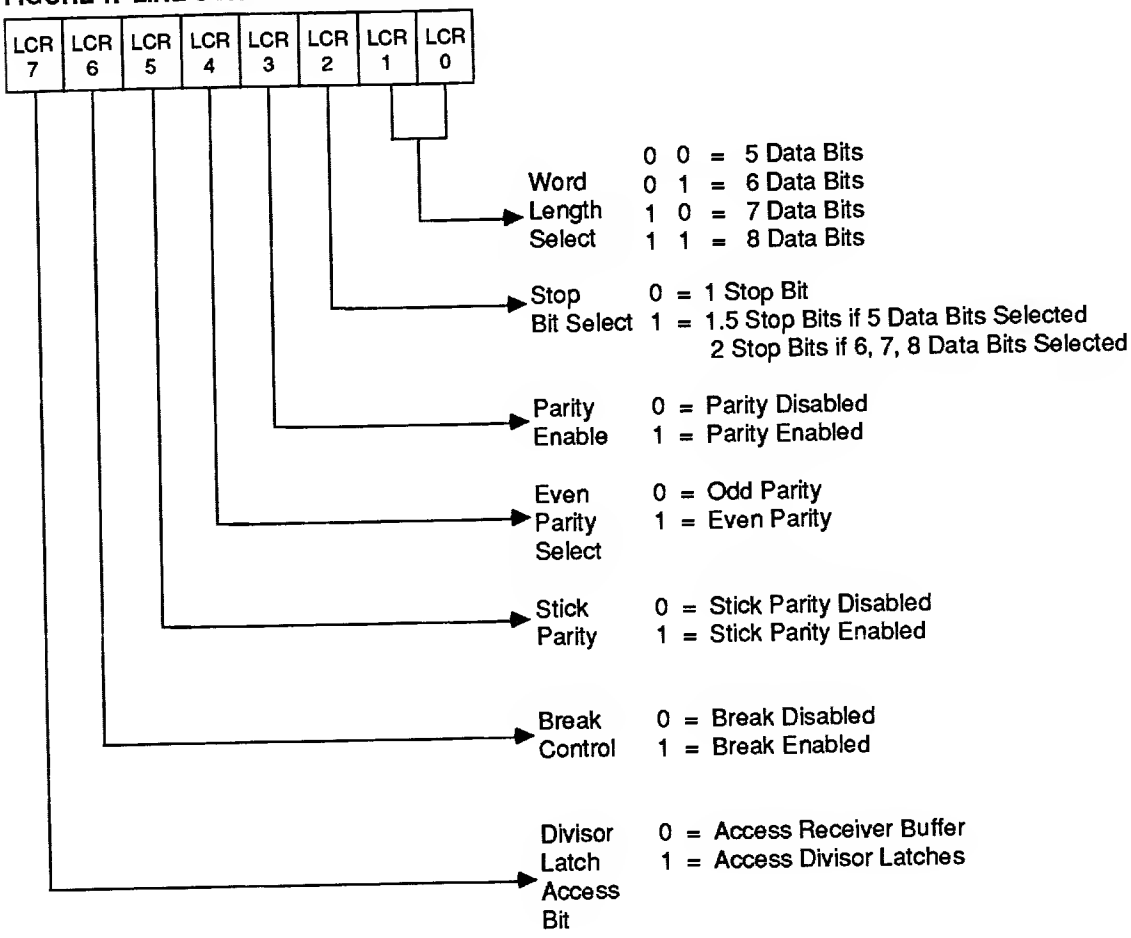
DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The serial channel is accessed when CS0 is low.

6

FIGURE 1. LINE CONTROL REGISTER



LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit LCR(4). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1)-LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading the Transmitter Holding Register by the CPU. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled IER(1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

MODEM CONTROL REGISTER

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 2. MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown as follows:

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	1	0
LSR(0) Data Ready (DR)	Ready	Not Ready
LSR(1) Overrun Error (OE)	Error	No Error
LSR(2) Parity Error (PE)	Error	No Error
LSR(3) Framing Error (FE)	Error	No Error
LSR(4) Break Interrupt (BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR(6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR(7) Not Used		

MCR(0): When MCR(0) is set high, the –DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the –RTS output is forced low. When MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(2): When MCR (2) is set high –OUT1 is forced low.

MCR(3): When MCR(3) is set high, the –OUT2 is forced low.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic 1) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs (–CTS, –DSR, –DCD (–RLSD), and –RI) are disconnected. The modem control outputs (–DTR, –RTS, –OUT1 and –OUT2) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high) on the VL16C450.

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Bits MCR(5)-MCR(7) are permanently set to logic 0.

MODEM STATUS REGISTER

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are –CTS, –DSR, –RI, and –DCD (–RLSD). MSR(4)-MSR(7) are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], an interrupt is generated whenever MSR(0)-MSR(3) is set to a one. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3.

MSR(0) Delta Clear to Send (DCTS): DCTS displays that the –CTS input to the serial channel has changed state since it was read last by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the –DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on –RI do not activate TERI.

MSR(3) Delta Data Carrier Detect [DDCD (DRLSD)]: DDCD (DRLSD) indicates that the –DCD (–RLSD) input to the serial channel has changed state since the last time it was read by the CPU.

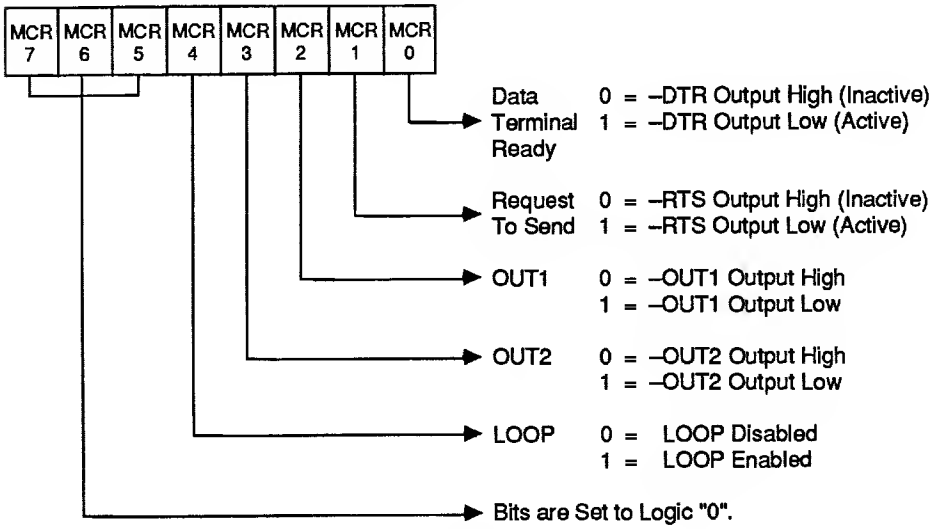
MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the complement of the –CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in Loop Mode [(MCR(4)=1], MSR(4) reflects the value of RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is the complement of

TABLE 3. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR(0)	DCTS	Delta Clear To Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DDCD (DRLSD)	Delta Data Carrier Detect
MSR(4)	–CTS	Clear To Send
MSR(5)	–DSR	Data Set Ready
MSR(6)	–RI	Ring Indicator
MSR(7)	–DCD (–RLSD)	Data Carrier Detect

FIGURE 2. MODEM CONTROL REGISTER



the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4)=1], MSR(5) reflects the value of DTR in the MCR.

MSR(6) Ring Indicator (RI): Is the complement of the –RI input (pin 39). If the channel is in the Loop Mode (MCR(4)=1), MSR(6) reflects the value of –OUT1 in the MCR.

MSR(7) Data Carrier Detect (DCD)/ Receive Line Signal Detect (RLSD): Data Carrier Detect/Receive Line Signal Detect indicates the status of the Data Carrier Detect/Receive Line Signal Detect (–DCD/–RLSD) input. If the channel is in the Loop Mode (MCR(4)=1), MSR(2) reflects the value of –OUT2 in the MCR.

Reading the MSR register will clear the delta modem status indications but has no effect on the other status bits.

For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read –DISTR operation, the status bit is not set until the trailing edge of the read.

If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read instead of being set again.

DIVISOR LATCHES

The ACE serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

RECEIVE BUFFER REGISTER

The receiver circuitry in the serial channel of the ACE is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits are 0's.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the CLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

TRANSMITTER HOLDING REGISTER

The Transmitter Holding Register (THR) holds character data until the Transmitter Shift Register is empty and ready to accept a new character. The transmitter and receiver word lengths are the same. If the character is less than eight bits, unused bits bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflects the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

SCRATCHPAD REGISTER (VL16C450 Only)

Scratchpad Register is an 8-bit Read/ Write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

INTERRUPT IDENTIFICATION REGISTER

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 4 and are described below:

IIR(0): IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 4.

IIR(3)-IIR(7): These five bits of the IIR are logic 0.

INTERRUPT ENABLE REGISTER

The Interrupt Enable Register (IER) is used to independently enable the four serial channel interrupt sources which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0)-IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 5 and below:

IER(0): When set to one, IER(0) enables the Received Data Available interrupt.

IER(1): When set to one, IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When set to one IER(2) enables the Receiver Line Status interrupt.

IER(3): When set to one, IER(3) enables the Modem Status Interrupt.

IER(4)-IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. The microprocessor should perform a write operation to the THR only if THRE is one. This causes THRE to be set to zero. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

TEMT remains low for the duration of the transmission of the data word. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word.

RECEIVER

Serial asynchronous data is input into the SIN pin. The ACE continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register when a full character is received, including parity and stop bits, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register which resets LSR(0). If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). If there is a parity error, the parity error is set in LSR(2). If a stop bit is not detected, a framing error indication is set in LSR(3).

If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5k bps are available. Tables 6, 7 and 8 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

MASTER RESET

After power up, the ACE MR input should be held high for one microsecond to reset the ACE circuits to an idle mode until initialization. A high on MR causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic

associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (reset low), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the ACE is given in Table 9.

PROGRAMMING

The serial channel of the ACE is programmed by the control register LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

TABLE 4. INTERRUPT IDENTIFICATION REGISTER

Interrupt Identification				Interrupt Set And Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –DCD (–RLSD)	MSR Read

X = Not Defined.

TABLE 5. SERIAL CHANNEL ACCESSIBLE REGISTERS

Address	Register Mnemonic	Register Bit Number							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0	THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0*	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1*	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
2	IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
3	LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
4	MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
5	LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
6	MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
7**	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*DLAB = 1
** VL16C450 Only

6

TABLE 6. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 7. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

TABLE 8. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 9. MASTER RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Are Permanently Low
Line Control Register	Reset	All Bits Low
Modem Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–OUT2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–OUT1	Reset	High

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5% (Note 1)

Symbol	Parameter	VL16C450		VL82C50A		VL82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
tADS	Address Strobe Width	60		90		90		ns	
tAS	Address Setup Time	60		90		90		ns	
tAH	Address Hold Time	0		0		0		ns	
tCS	Chip Select Setup Time	60		90		90		ns	
tCH	Chip Select Hold Time	0		0		0		ns	
tDIW	–DISTR/DISTR Strobe Width	125		175		175		ns	
tRC	Read Cycle Delay	175		500		500		ns	
RC	Read Cycle = tAR(1) + tDIW + tRC	360		755		755		ns	
tDD	–DISTR/DISTR to Drive Disable Delay		60		75		75	ns	100 pF Load Note 3
tDDD	Delay from –DISTR/DISTR to Data		125		175		175	ns	100 pF Load
tHz	–DISTR/DISTR to Floating Data Delay	0	100	100		100		ns	100 pF Load Note 3
tDOW	–DOSTR/DOSTR Strobe Width	100		175		175		ns	
tWC	Write Cycle Delay	200		500		500		ns	
WC	Write Cycle = tAW + tDOW + tWC	360		755		755		ns	
tDS	Data Setup Time	40		90		90		ns	
tDH	Data Hold Time	40		60		60		ns	
tCSC	Chip Select Output Delay from Select		100		125		125	ns	100 pF Load
tRA	Address Hold Time from –DISTR/DISTR	20		20		20		ns	Note 2
tRCS	Chip Select Hold Time from –DISTR/DISTR	20		20		20		ns	Note 2
tAR	–DISTR/DISTR Delay from Address	60		80		80		ns	Note 2
tCSR	–DISTR/DISTR Delay from Chip Select	50		80		80		ns	Note 2
tWA	Address Hold Time from –DOSTR/DOSTR	20		20		20		ns	Note 2
tWCS	Chip Select Hold Time from –DOSTR/DOSTR	20		20		20		ns	Note 2
tAW	–DOSTR/DOSTR Delay from Address	60		80		80		ns	Note 2
tCSW	–DOSTR/DOSTR Delay from Select	50		80		80		ns	Note 2
tMRW	Master Reset Pulse Width	1		1		1		µs	
tXH	Duration of Clock High Pulse	140		140		140			
tXL	Duration of Clock Low Pulse	140		140		140			External Clock (3.1 MHz Max)

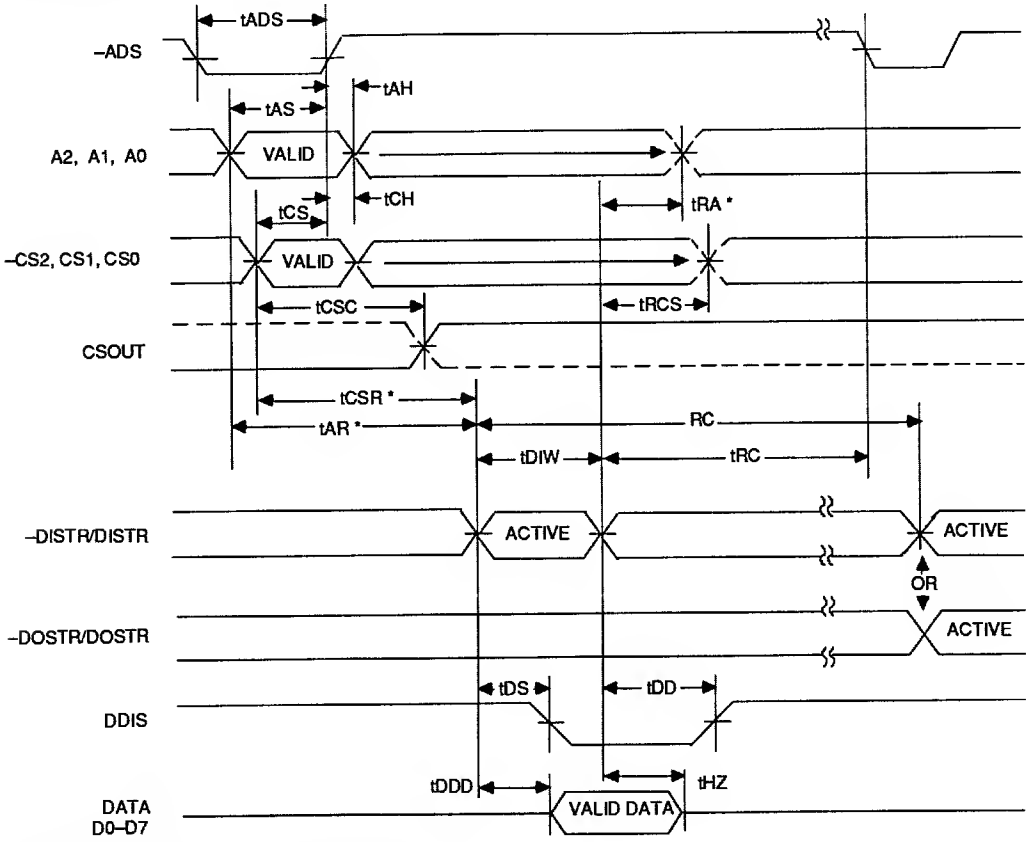
Notes: 1. All timings are referenced to valid 0 and valid 1. (See AC Test Points.)
2. Applicable only when –ADS is tied Low.
3. Charge and discharge time is determined by VOL, VOH and the external loading.

Symbol	Parameter	VL16C450		VL82C50A		VL82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Transmitter									
tHR1	Delay from Rising Edge of –DOSTR/DOSTR (WR THR) to Reset Interrupt		175		1000		N/A	ns	100 pF Load
tHR2	Delay from Falling Edge of –DOSTR/DOSTR (WR THR) to Reset Interrupt		N/A		N/A		1000	ns	100 pF Load
tIRS	Delay from Initial INTR Reset Interrupt		16		16		16	–BAUDOUT CYCLES	
tSI	Delay from Initial Write to Interrupt	8	24	8	24	8	24	–BAUDOUT CYCLES	
tSS	Delay from Stop to Next Start		100		100		100	ns	
tSTI	Delay from Start Bit Low to Interrupt (THRE) High		8		8		8	–BAUDOUT CYCLES	
tIR	Delay from –DISTR/DISTR (RD IIR) to Reset Interrupt (THRE)		250		1000		1000	ns	100 pF Load
Modem Control									
tMDO	Delay from –DOSTR/DOSTR (WR MCR) to Output		250		1000		1000	ns	100 pF Load
tSIM	Delay to Set Interrupt from Modem Input		250		1000		1000	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –DISTR/DISTR (RS MSR)		250		1000		1000	ns	100 pF Load
Baud Generator									
N	Baud Divisor	1	$2^{16}-1$	1	$2^{16}-1$	1	$2^{16}-1$		
tBLD	Baud Output Negative Edge Delay		125		250		250	ns	100 pF Load
tBHD	Baud Output Positive Edge Delay		125		250		250	ns	100 pF Load
tLW	Baud Output Down Time	425		425		425		ns	fX = 2 MHz, ÷2, 100 pF Load
tHW	Baud Output Up Time	330		330		330		ns	fX = 2 MHz, ÷2, 100 pF Load
Receiver									
tSCD	Delay from RCLK to Sample Time		2		2		2	µs	
tSINT	Delay from Stop to Set Interrupt		1		1		1	RCLK	100 pF Load
tRINT	Delay from –DISTR/DISTR (RD RBR/RDLSR) to Reset Interrupt		1		1		1	µs	100 pF Load

Note: 1. All timings are referenced to valid 0 and valid 1. (See AC Test Points.)

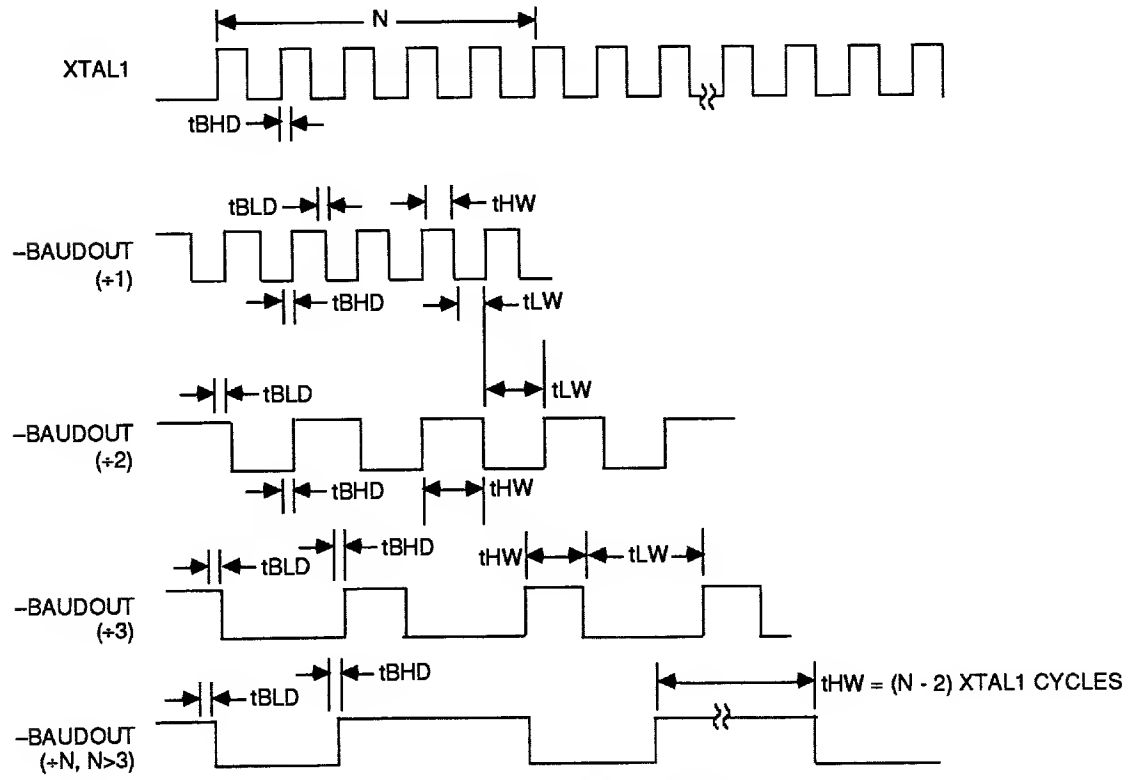
TIMING DIAGRAMS

READ CYCLE

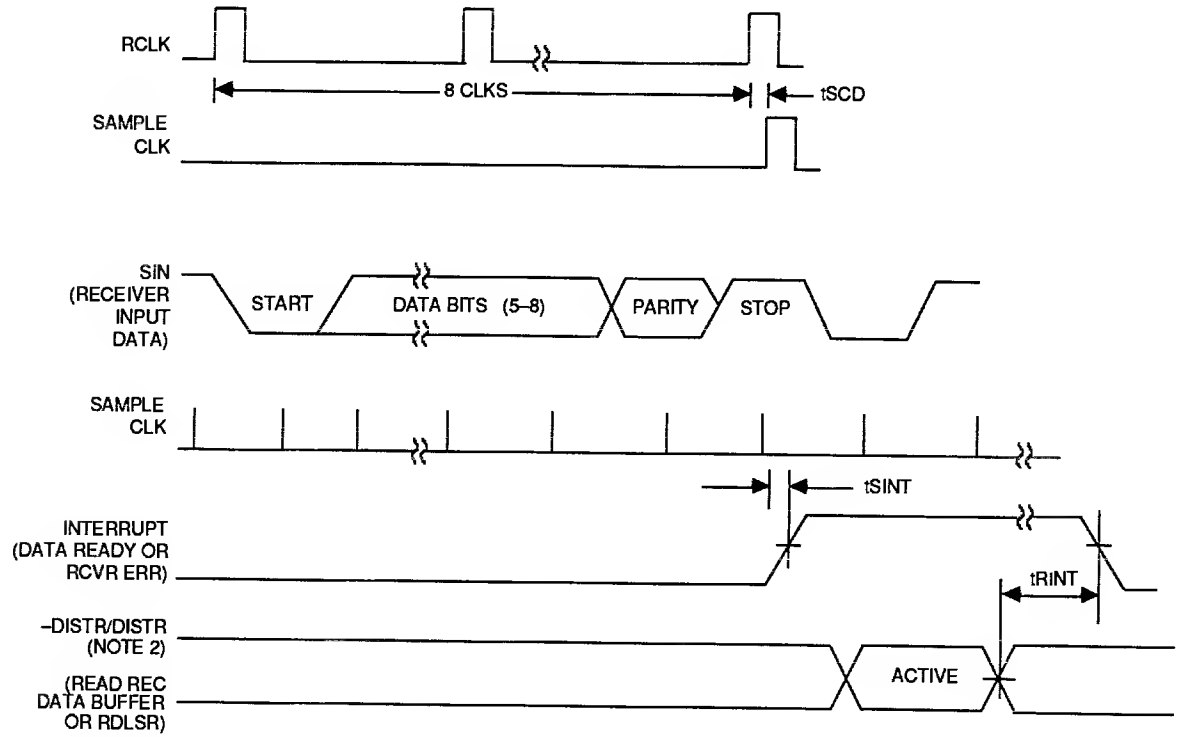


* Applicable only when –ADS is tied low.

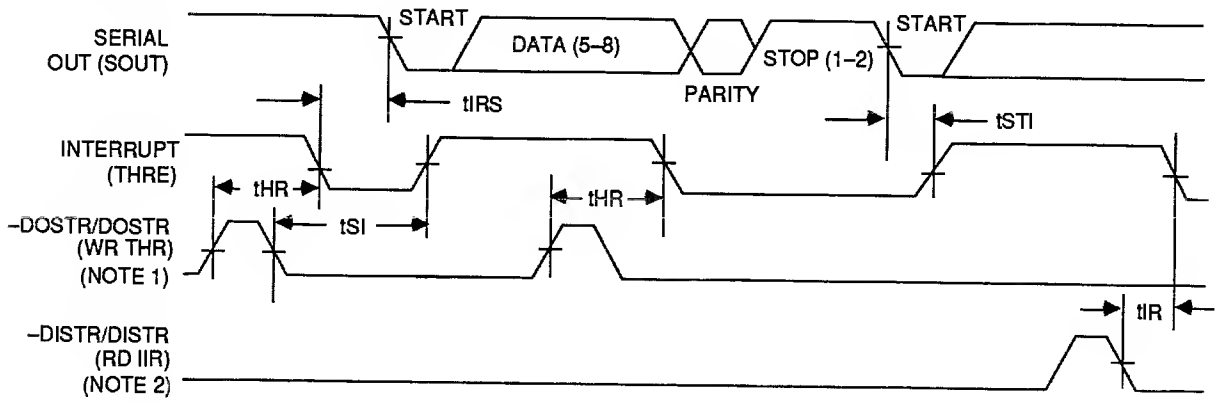
BAUDOUT



RECEIVER

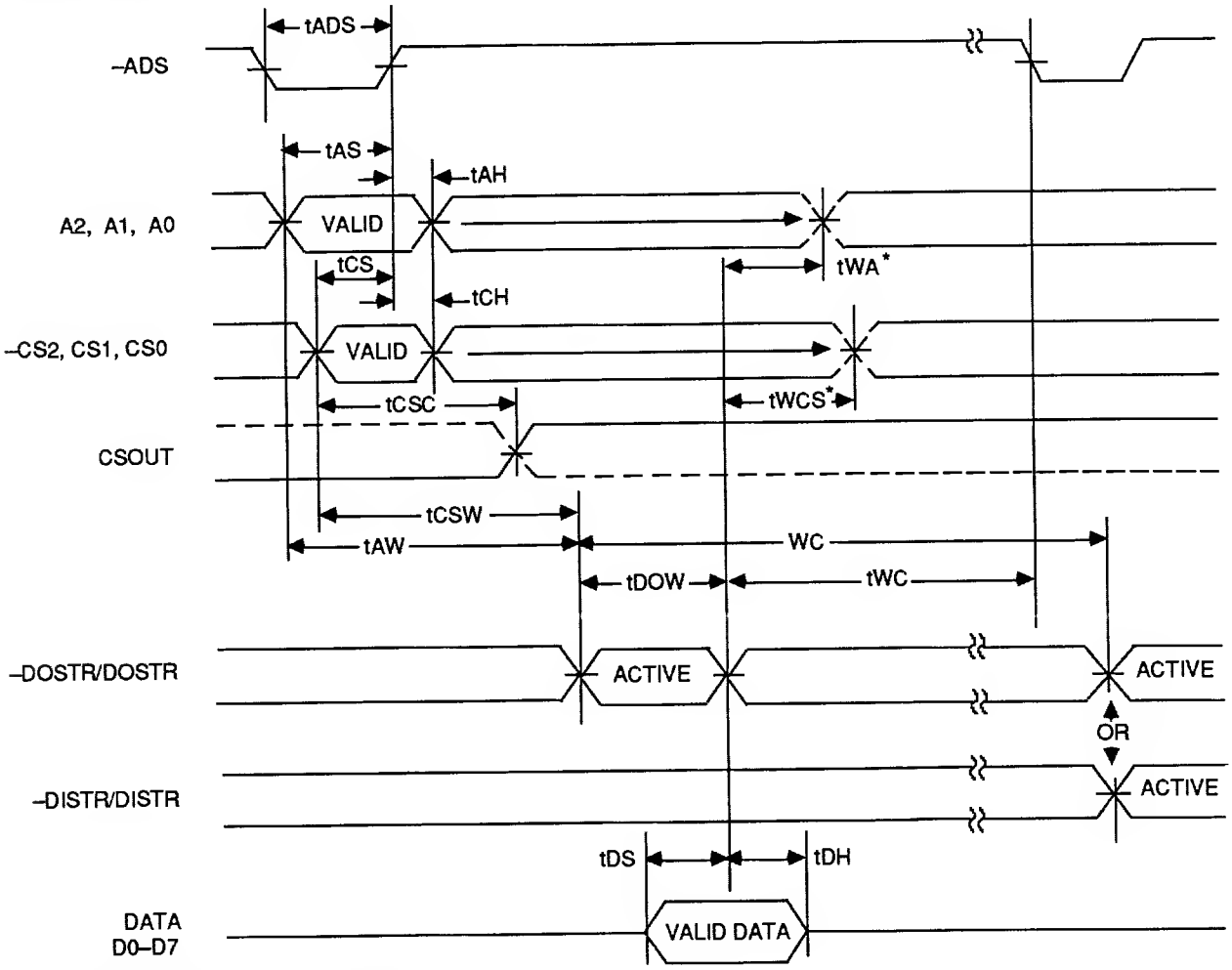


TRANSMITTER



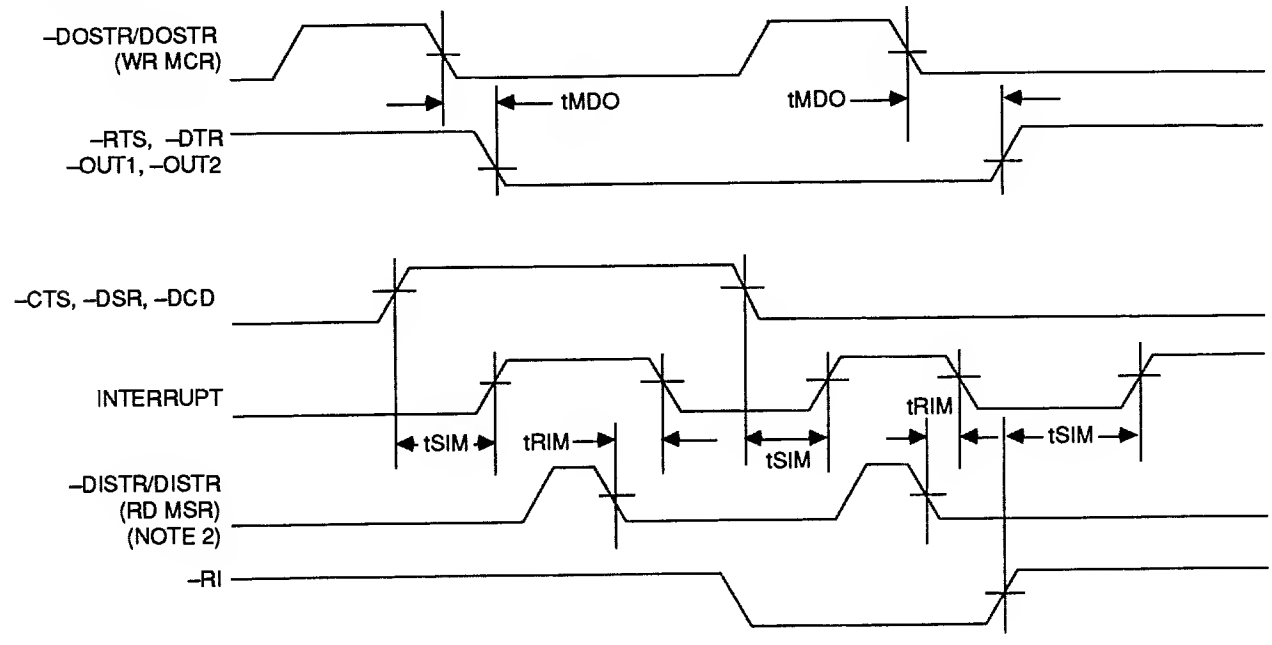
Notes: 1. See WRITE Timing Diagram.
2. See READ Timing Diagram.

WRITE CYCLE



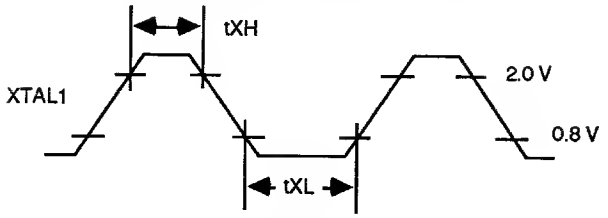
* Applicable only when –ADS is tied low.

MODEM CONTROLS

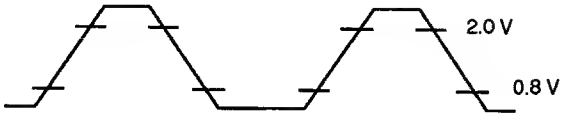


AC TESTING INPUT/OUTPUT WAVEFORMS

EXTERNAL CLOCK INPUT (3.1 MHz MAXIMUM)

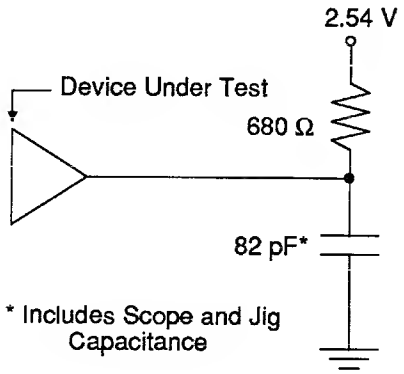


AC TEST POINTS



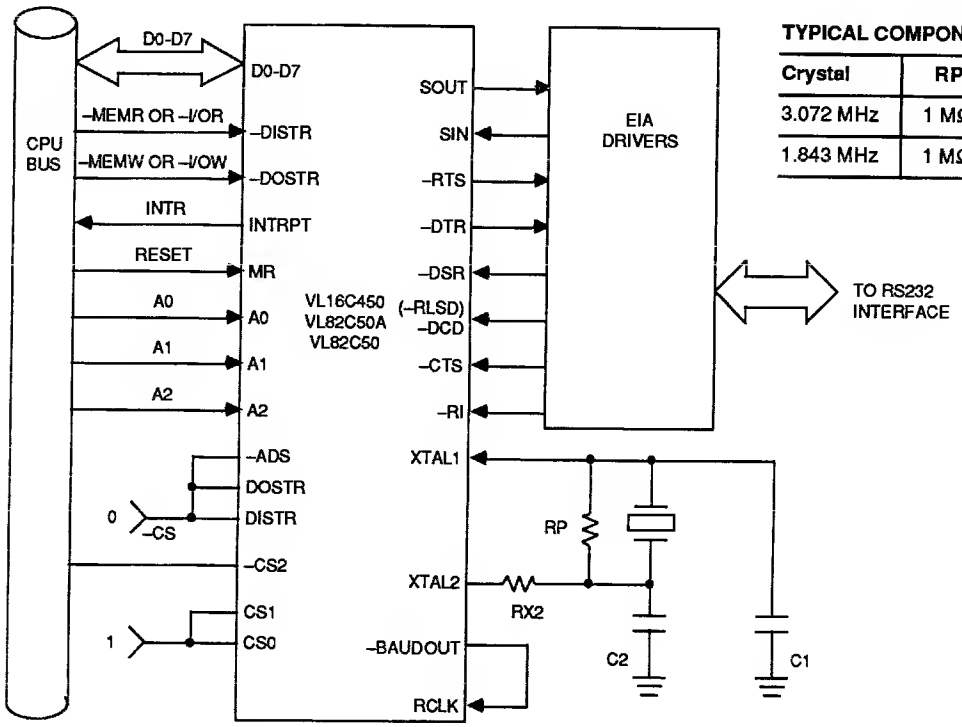
Note: All timings are referenced to valid 0 and valid 1.

TEST CIRCUIT



BASIC CONFIGURATION

VL16C450, VL82C50A, VL82C50



TYPICAL COMPONENT VALUES

Crystal	RP	RX2	C1	C2
3.072 MHz	1 MΩ	1.5 KΩ	10 - 30 pF	40 - 90 pF
1.843 MHz	1 MΩ	1.5 KΩ	10 - 15 pF	65 - 100 pF

6

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VCC +0.3 V
Applied Output Voltage	–0.5 V to VCC +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mV

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	VL16C450		VL82C50A		VL82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
VILX	Clock Input Low Voltage	–0.5	0.8	–0.5	0.8	–0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VIL	Input Low Voltage	–0.5	0.8	–0.5	0.8	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VOL	Output Low Voltage		0.4		0.4		0.4	V	IOL 1.6 mA on All
VOH	Output High Voltage	2.4		2.4		2.4		V	IOH = –1.0 mA
ICC (Ave)	Average Power Supply Current (VCC)		10		10		10	mA	VCC = 5.25 V, No Loads on SIN , –DSR –RLSD, –CTS, –DCD. –RI = 2.0 V. All Other Inputs = 0.8 V. Baud Rate Generator at 4 MHz. Baud Rate at 56K.
IIL	Input Leakage		±10		±10		±10	µA	VCC = 5.25 V VSS = 0 V All Other Pins Floating
ICL	Clock Leakage		±10		±10		±10	µA	VIN = 0 V, 5.25 V
IOZ	Three-State Leakage		± 20		± 20		± 20	µA	VCC = 5.25 V VSS = 0 V VOUT = 0 V, 5.25 V 1) Chip Deselected 2) Chip and Write Mode selected
VILMR	MR Schmitt VIL		0.8		0.8		0.8	V	
VIHMR	MR Schmitt VIH	2.0		2.0		2.0		V	

CAPACITANCE

Symbol	Parameter		Min.	Max.	Units
CI	Input Capacitance	Crystal		10	pF
		All Others		7	pF
CIO	I/O Capacitance			7	pF
COC	Output Capacitance	Crystal		10	pF
		All Other		7	pF

VL16C451

PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- VL16C450 with on-board Centronix printer interface
- Completely pin- and upward-compatible with the dual serial channel VL16C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

DESCRIPTION

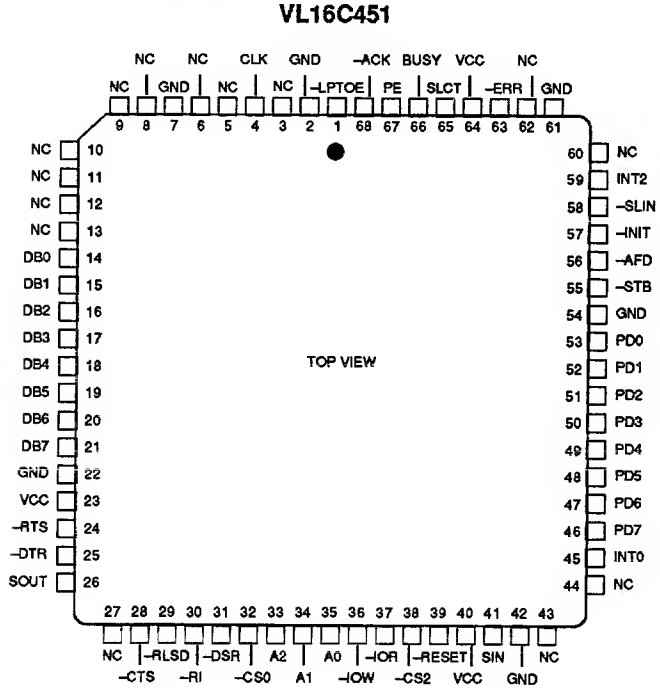
The VL16C451 is an enhanced version of the popular VL16C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the Parallel/Asynchronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operation being performed, and error conditions. It is fully pin- and upward-compatible with the dual serial channel VL16C452. The second serial channel of the VL16C452 occupies pins that are VCC, GND, or NC (not connected) on the VL16C451.

The VL16C451 also provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics interface. The parallel port, together with the serial port, provide IBM PC/AT-compatible computers with a single device to serve the two system ports.

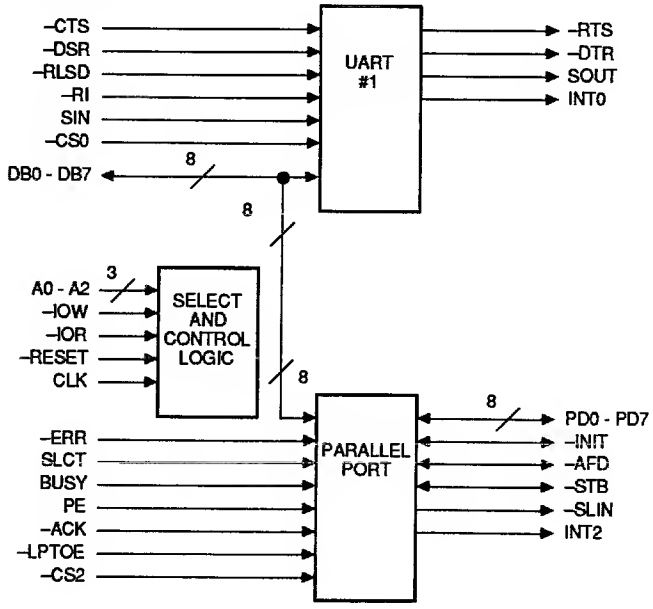
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

The VL16C451 is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C451-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–IOR	37	I	Read Strobe - This is an active low input which enables data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2, and the chip select.
–IOW	36	I	Write Strobe - This is an active low input which causes data from the data bus (DB0-DB7) to be input to the ACE or to the parallel port. The destination depends upon the register selected by the address inputs A0, A1, A2 and the chip selects.
DB0-DB7	14-21	I/O	Data Bits DB0-DB7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL16C451 and the CPU. These lines are normally in a high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	35, 34, 33	I	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels, Table 10 for the decode of the parallel line printer port.
CLK	4	I	Clock Input - The external clock input to the ACE baud rate divisor.
SOUT	26	O	Serial Data Output - This line is the serial data output from the ACE's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). SOUT is held in the mark condition when the transmitter is disabled, –RESET is true, the Transmitter Register is empty, or when in the Loop Mode.
–CTS	28	I	Clear to Send Input - The logical state of the –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of the ACE. A change of state of the –CTS pin, since the previous reading of the MSR, causes the setting of DCTS [MSR(0)] of the Modem Status Register.
–DSR	31	I	Data Set Ready Input - The logical state of the –DSR pin is reflected in MSR(5) of the Modem Status Register. DDSR [MSR(1)] indicates whether the –DSR pin has changed state since the previous reading of the MSR.
–DTR	25	O	Data Terminal Ready Output - The –DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of the UART. This signal is cleared (high) by writing a logic 0 to the –DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the –DTR pin indicates that the ACE is ready to receive data.
–RTS	24	O	Request to Send Output - The –RTS pin is set low by writing a logic 1 to MCR(1) bit 1 of the ACE's Modem Control Register. The –RTS pin is reset high by –RESET. A low on the –RTS pin indicates that the ACE has data ready to transmit. In half duplex operations, –RTS is used to control the direction of the line.
–RI	30	I	Ring Indicator Input - The –RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the ACE. The Modem Status Register output TERI [MSR(2)] indicates whether the –RI input has changed from high to low since the previous reading of the MSR.
–LPTOE	1	I	Parallel Data Output Enable - When low, this signal enables the Write Data Register to the PD0-PD7 lines. A high puts the PD0-PD7 lines in the high-impedance state allowing them to be used as inputs. –LPTOE is usually tied low for printer operation.
SIN	41	I	Serial Data Input - The serial data input moves information from the communication line or modem to the VL16C451 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the Loop Mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–RLSD	29	I	Receive Line Signal Detect - –RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Register. MSR(3) (DRLSD) of the Modem Status Register indicates whether the –RLSD input has changed since the previous reading of the MSR. –RLSD has no effect on the receiver.
–RESET	39	I	Reset - When low, the –RESET input forces the VL16C451 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its output is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0	45	O	Serial Channel Interrupt Output - This three-state output is enabled by the MCR bit 2. The serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of the serial channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service. Upon reset, the interrupt output will be in the high impedance state.
–CS0, –CS2	32, 38	I	Chip Selects - Each Chip Select input acts as an enable for the write and read signals for its channel. –CS0 enables the serial port, while –CS2 enables the the signals to the line printer port.
PD0-PD7	53-46	I/O	Parallel Data Bits (0-7) - These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when –LPTOE is held in the high state.
–STB	55	O	Line Printer Strobe - This open-drain line provides communication between the VL16C451 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
–AFD	56	O	Line Printer Autofeed - This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
–INIT	57	O	Line Printer Initialize - This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
–SLIN	58	O	Line Printer Select - This open-drain line selects the printer when it is active low.
INT2	59	O	Printer Port Interrupt - This signal is an active high, three-state output, generated by the positive transition of –ACK. It is enabled by bit 4 of the Write Control Register. Upon a reset, the interrupt output will be in the high impedance state.
–ERR	63	I	Line Printer Error - This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
SLCT	65	I	Line Printer Selected - This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	I	Line Printer Busy - This is an input line from the line printer that goes high when the line printer is not ready to accept data.
PE	67	I	Line Printer Paper Empty - This is an input line from the line printer that goes high when the printer runs out of paper.
–ACK	68	I	Line Printer Acknowledge - This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
VCC	23, 40, 64		Power Supply - The power supply requirement is 5 V ±5%.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
GND	2, 7, 22, 42, 54, 61		Ground (0 V) - All pins must be tied to ground for proper operation.
NC	3, 5, 6, 8-13, 27, 43, 44, 60, 62		No Connection

FUNCTIONAL DESCRIPTION

SERIAL CHANNEL REGISTERS

Three types of internal registers are used in the serial channel of the VL16C451. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The VL16C451 data registers are double-buffered so that read and write operations can be performed at the same time the ACE is performing the parallel-to-serial and serial-to-parallel conversion.

LINE CONTROL REGISTER

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described in Figure 1.

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The serial channel is accessed when –CS0 is low.

LCR (0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in Figure 1.

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for one stop bit.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

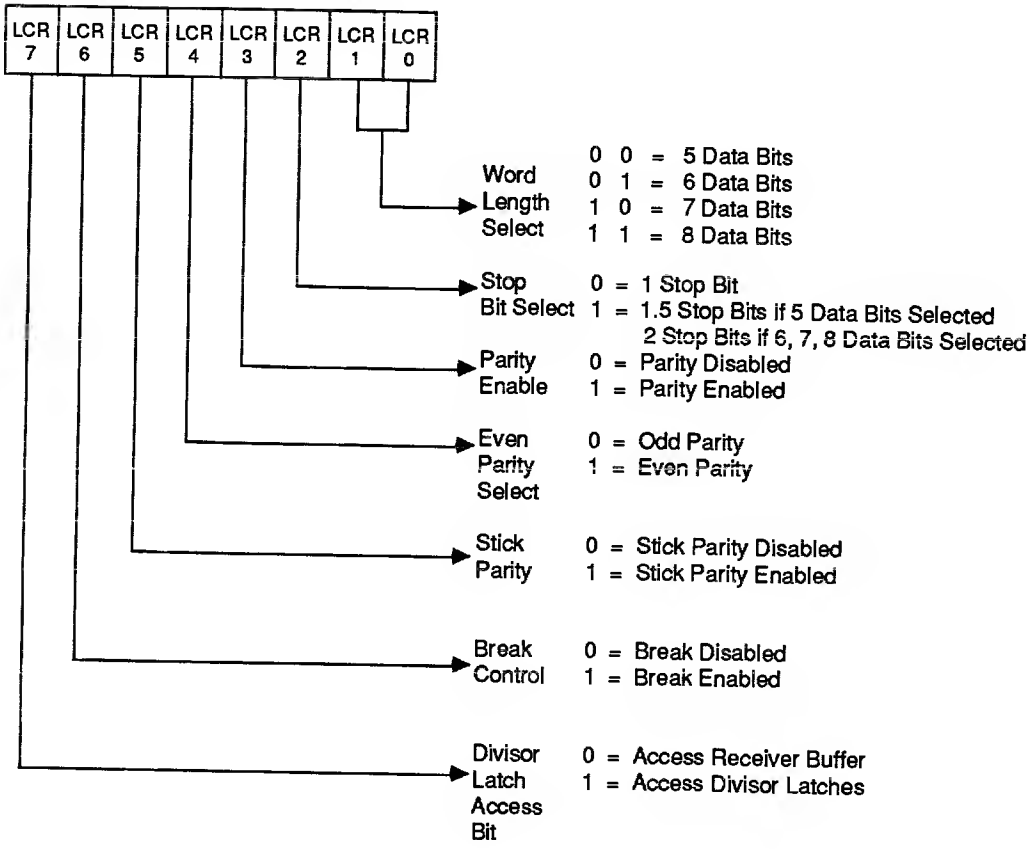
LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.

FIGURE 1. LINE CONTROL REGISTER



3. Wait for the transmitter to be idle (TEMT=1), and clear break when normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

LINE STATUS REGISTER

The Line Status Register (LSR) is a single register that provides status indications.

The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in transferred into the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE shows that the serial channel is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	1	0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled [IER(1)=1]. THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

MODEM CONTROL REGISTER

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 2. The MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the –DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the –RTS output is forced low. When MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (–CTS, –DSR, and –RI) are disconnected. The modem control outputs (–DTR and –RTS) are internally connected to –CTS and –DSR. –RI is connected to –MCR(2). The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Bits MCR(5) - MCR(7) are permanently set to logic 0.

MODEM STATUS REGISTER

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the VL16C451. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for the channel are –CTS, –DSR, –RI, and –RLSD. MSR(4) - MSR(7) are status indications of these lines. A status bit=1 indicates the associated signal is low, a bit=0 indicates a high. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], an interrupt is generated whenever MSR(0) is set to a one. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3.

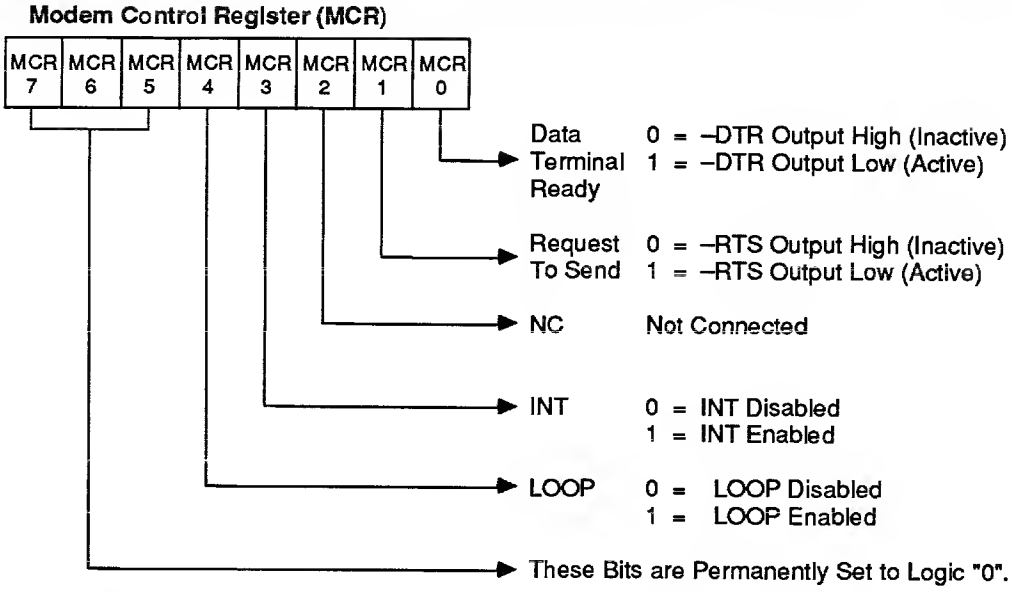
MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the –CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the –DSR input to the serial channel has changed state since the last time it was read by the CPU.

TABLE 3. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(0)	DCTS	Delta Clear to Send
MSR(3)	DRLSD	Delta Receive Line Signal Detect
MSR(4)	CTS	Clear To Send
MSR(5)	DSR	Data Set Ready
MSR(6)	RI	Ring Indicator
MSR(7)	RLSD	Receive Line Signal Detect

FIGURE 2. MODEM CONTROL REGISTER



MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on –RI do not activate TERI.

MSR(3) Delta Receive Line Signal Detect (DRLSD): DRLSD indicates that the –RLSD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the complement of the –CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in Loop Mode [MCR(4)=1], this bit reflects the value of –RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is the complement of the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the Loop Mode [MCR(4)=1], this bit reflects the value of –DTR in the MCR.

MSR(6) Ring Indicator: Is the complement of the RI input (pin 39). If the channel is in the Loop Mode [MCR(4)=1], this bit reflects the state of MCR(2).

MSR(7) Receive Line Signal Detect : Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (–RLSD) input . If the channel is in the Loop Mode [MCR(4)=1], this bit reflects the state of INT0 of the MCR.

The modem status inputs (–RI, –RLSD, –DSR, and –CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the other status bits.

For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read operation, the status bit is not set until the trailing edge of –IOR.

If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of –IOR instead of being set again.

DIVISOR LATCHES

The VL16C451 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

RECEIVE BUFFER REGISTER

The receiver circuitry in the serial channel of the VL16C451 is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits 0's.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in

the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

TRANSMIT HOLDING REGISTER
The Transmitter Holding Register (THR) holds the character until the Transmitter Shift Register is empty and ready to accept a new character. The transmitter and receiver word lengths are the same. If the character is less than eight bits, unused bits are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflect the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

SCRATCHPAD REGISTER
Scratchpad Register is an 8-bit Read/ Write register that has no effect on either channel in the VL16C451. It is intended to be used by the programmer to hold data termporarily.

INTERRUPT IDENTIFICATION REGISTER
In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). The IIR indicates the highest priority interrupt pending. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 4 and are described below.

IIR(0): IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

INTERRUPT ENABLE REGISTER
The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupt sources which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Figure 2 and below:

IER(0): When set to one, IER(0) enables Received Data Available interrupt.

IER(1): When set to one, IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When set to one, IER(2) enables the Receiver Line Status interrupt.

IER(3): When set to one, IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are Logic 0.

TRANSMITTER
The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. The microprocessor should perform a write to the THR only if THRE is one. This causes the THRE to be reset to 0. THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

TEMT remains low for at least the duration of the transmission of the data word. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word.

RECEIVER
Serial asynchronous data is input into the SIN pin. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character [LCR(0), LCR(1)], if parity is used LCR(3), and the polarity of parity LCR(4).

Status for the receiver is provided in the Line Status Register. When a full character is received including parity and stop bit, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register which resets LSR(0). If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). If there is a parity error, the parity error is set in LSR(2). If a stop bit is not detected, a framing error indication is set in LSR(3).

If the data into SIN is symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)
The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 5, 6 and 7 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the VL16C451 –RESET input should be held low for 500 ns to reset the VL16C451 circuits to an idle mode until initialization. A low on –RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the VL16C451 remains in the idle mode until programmed.

A hardware reset of the VL16C451 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the VL16C451 is given in Table 8.

PROGRAMMING

The serial channel of the VL16C451 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the VL16C451 serial channel is not transmitting or receiving data.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the VL16C451 is 3.1 MHz.

TABLE 4. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –DCD –RLSD	MSR Read

X = Not Defined.

FIGURE 3. INTERRUPT CONTROL LOGIC

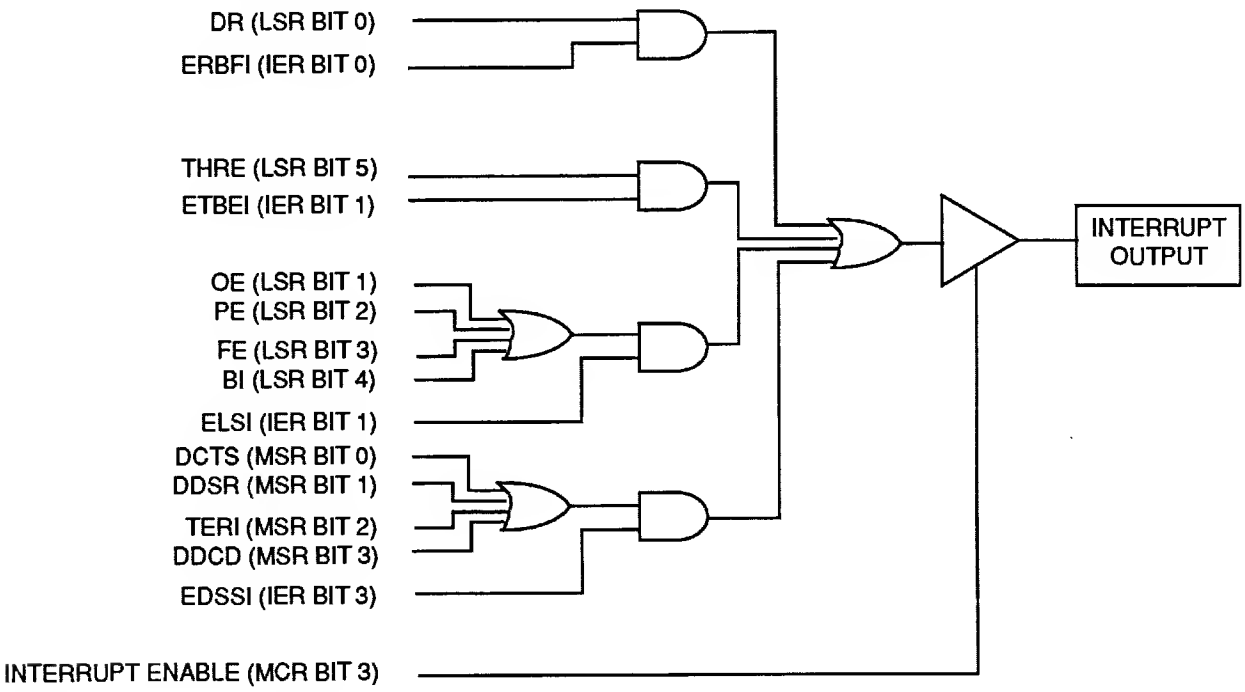


TABLE 5. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 6. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

TABLE 7. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 8. RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Are Permanently Low
Line Control Register	Reset	All Bits Low
Modem Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–OUT2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–OUT1	Reset	High

DEVICE APPLICATION

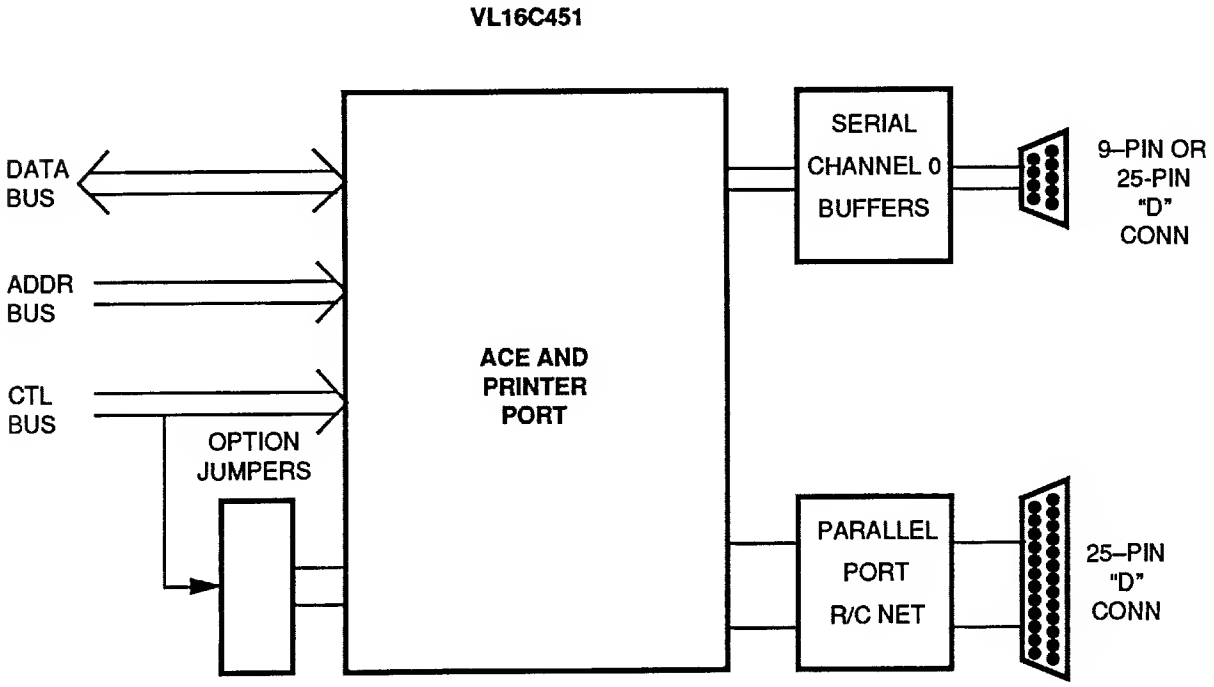


TABLE 9. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	INT	NC	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRLSD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

PARALLEL PORT REGISTERS

The VL16C451's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (–CS2) is low, the parallel port is selected. Table 10 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (–IOR) and write (–IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (BUSY), Acknowledge (–ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (–ERR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines. They are Interrupt Enable (IRQ ENB), Select In (–SLIN), Initialize the Printer (–INIT), Autofeed the Paper (–AFD) and Strobe (–STB). The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

Figure 4 describes the operation of the –LPTOE input. When –LPTOE goes Low, the internal data latch is enabled to the PD0-PD7 lines. PD0-PD7 will then contain the same information as the latch.

When –LPTOE goes high, the internal data latch is disabled from the PD0-PD7 lines. An external device can place data on the PD0-PD7 lines, and reading the data reads the PD0-PD7 lines.

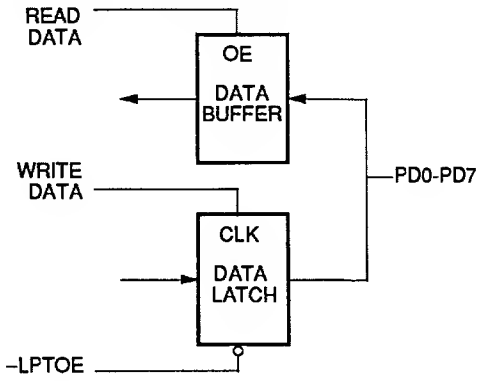
TABLE 10. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BUSY	–ACK	PE	SLCT	–ERR	1	1	1
Read Control	1	1	1	IRQ ENB	–SLIN	–INIT	–AFD	–STB
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	–SLIN	–INIT	–AFD	–STB

TABLE 11. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
–IOR	–IOW	–CS2	A1	A0	
0	1	0	0	0	Read Port
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Port
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

FIGURE 4. –LPTOE FUNCTION



AC CHARACTERISTICS: TA= 0°C to +70°C, VCC= 5 V ±5% (Note 4)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle	360		ns	
tDDD	Delay from –IOR to Data		125	ns	100 pF Load
tHZ	–IOR to Floating Data Delay	0	100	ns	100 pF Load, Note 3
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle	360		ns	
tDS	Data Setup Time	40		ns	
tDH	Data Hold Time	40		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 1
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 1
tAR	–IOR Delay from Address	60		ns	Note 1
tCSR	–IOR Delay from Chip Select	50		ns	Note 1
tWA	Address Hold Time from –IOW	20		ns	Note 1
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 1
tAW	–IOW Delay from Address	60		ns	Note 1
tCSW	–IOW Delay from Select	50		ns	Note 1
tRW	Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

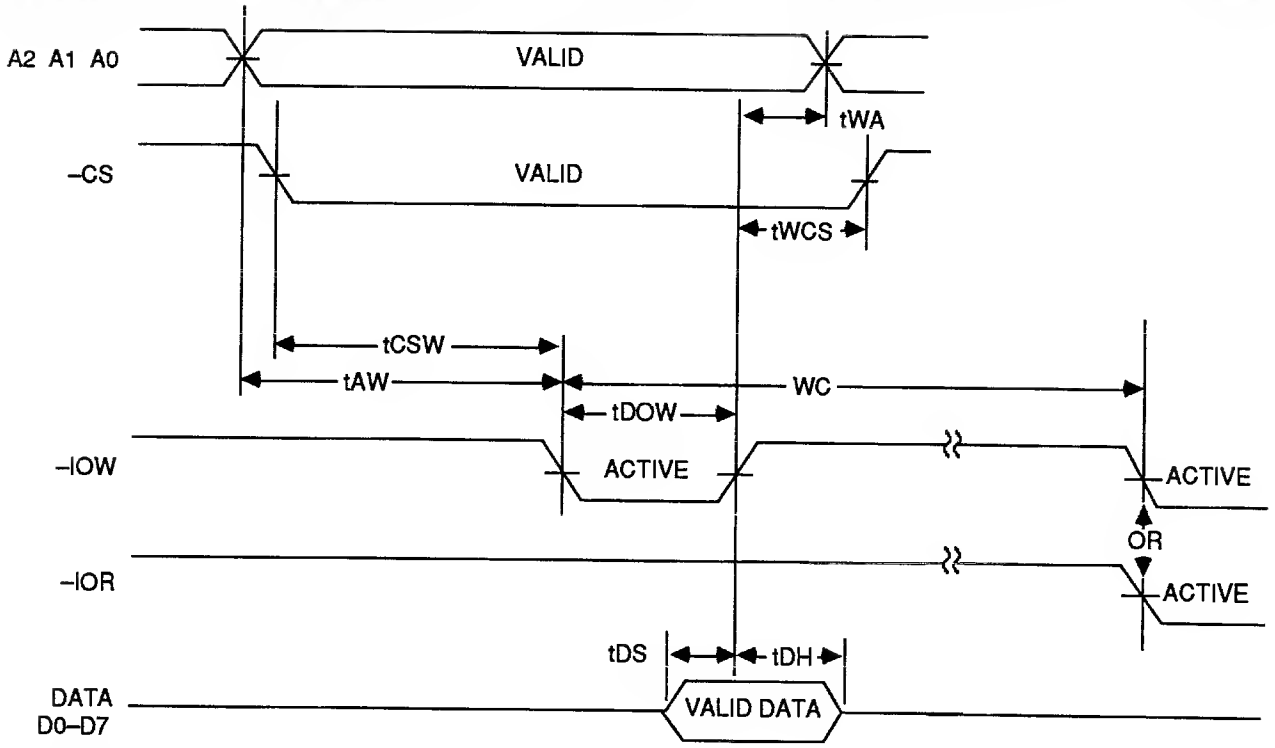
Notes:
1. The internal address strobe is always active.
2. RCLK = tXH and tXL.
3. Charge and discharge time is determined by VOL, VOH and the external loading.
4. All timings are referenced to valid 0 and valid 1. (See AC Test Points.)

AC CHARACTERISTICS (Cont.): TA= 0°C to +70°C, VCC= 5 V ±5% (Note 4)

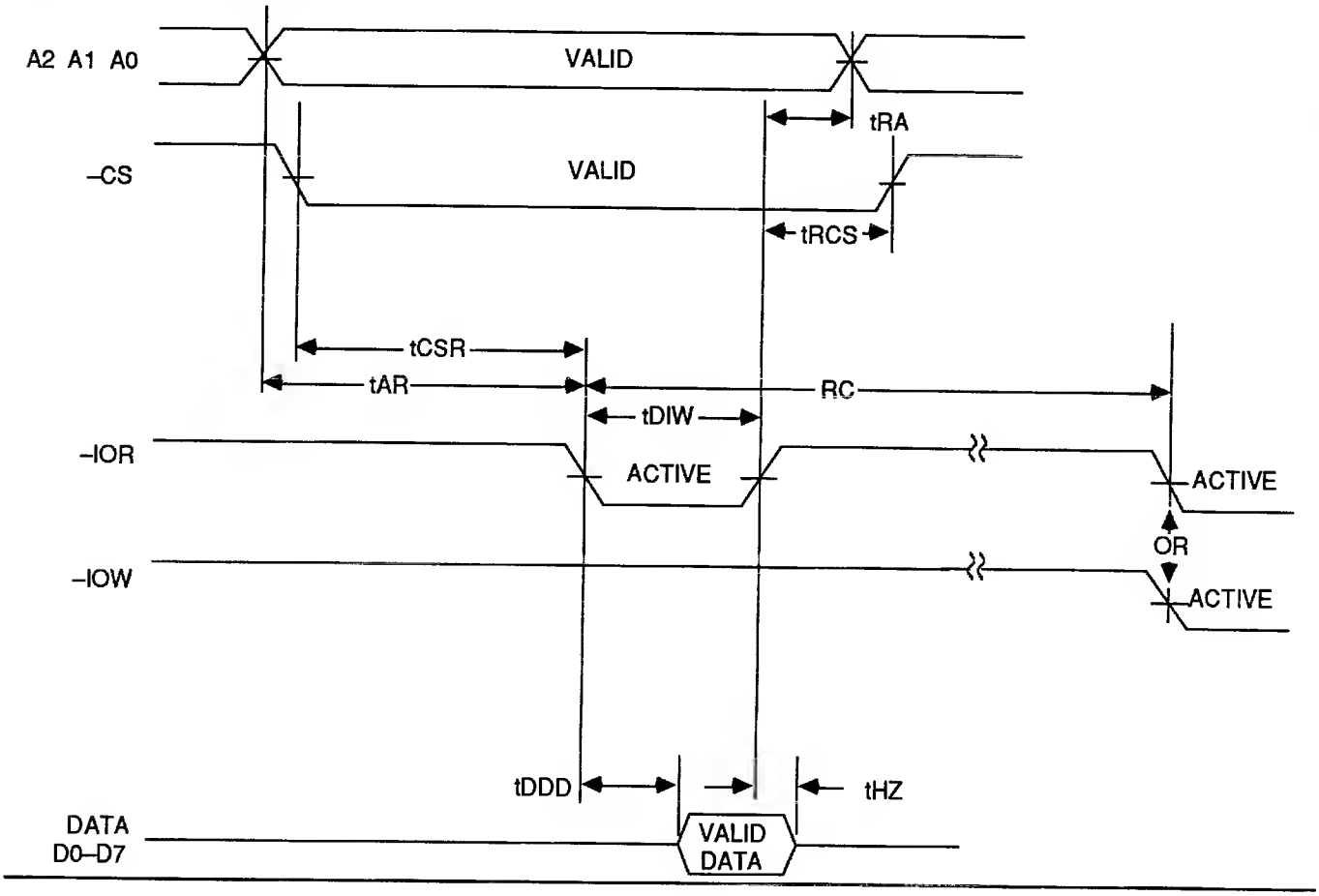
Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of –IOW (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INT0 Reset to Transmit Start		16	CLK Cycles	Note 2
tSI	Delay from Initial Write to Interrupt	8	24	CLK Cycles	Note 2
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 2
tIR	Delay from –IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
tMDO	Delay from –IOW (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from Modem Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –IOR (RS MSR)		250	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 2
tRINT	Delay from –IOR (RD RBR/RD LSR) to Reset Interrupt		1	µs	100 pF Load
Parallel Port					
tDT	Data Time	1		µs	
tSB	Strobe Time	1	500	µs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			µs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			µs	Defined by Printer
tAK	Acknowledge Duration Time			µs	Defined by Printer
tBSY	Busy Duration Time			µs	Defined by Printer
tBSD	Busy Delay Time			µs	Defined by Printer

Notes: 1. The internal address strobe is always active.
2. RCLK = tXH and tXL.
3. Charge and discharge time is determined by VOL, VOH and the external loading.
4. All timings are referenced to valid 0 and valid 1 (see AC Test Points).

WRITE CYCLE TIMING

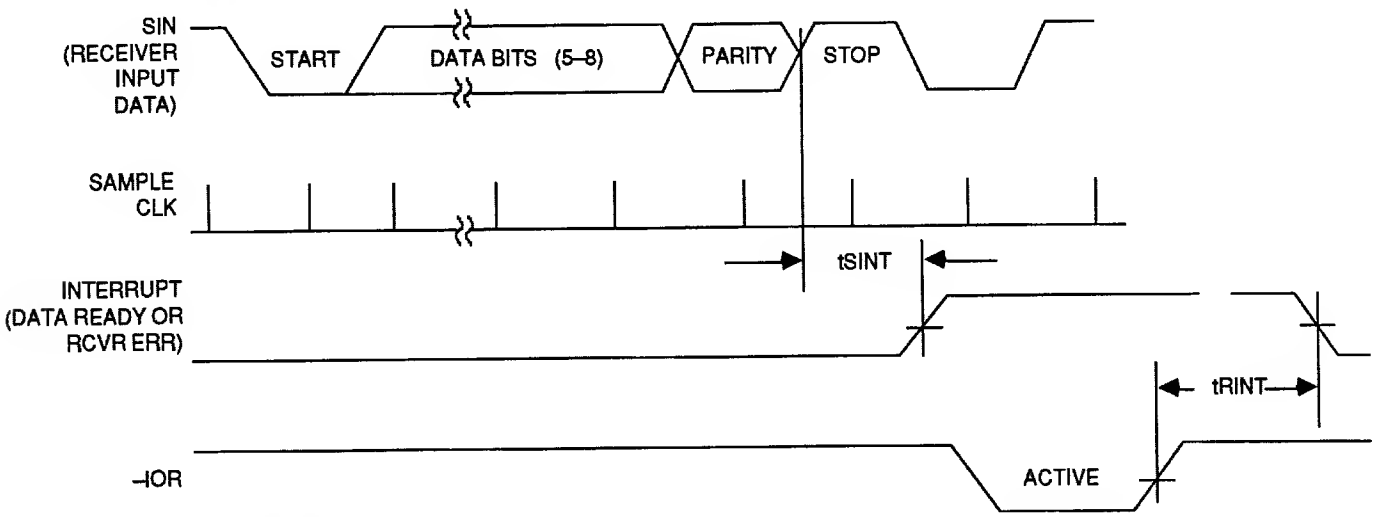


READ CYCLE TIMING

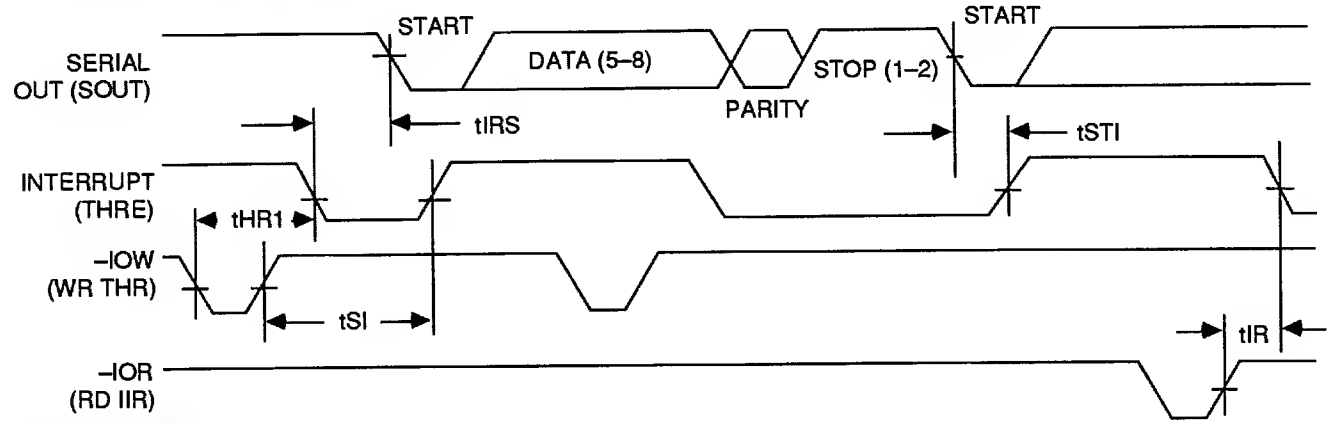


6

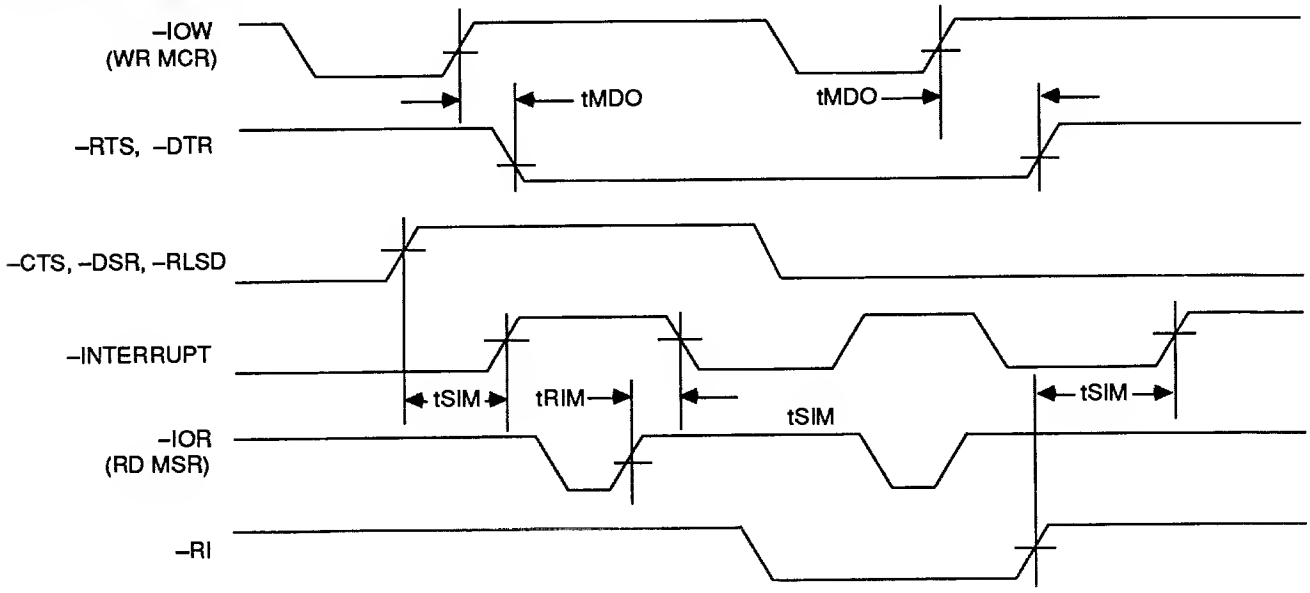
RECEIVER TIMING



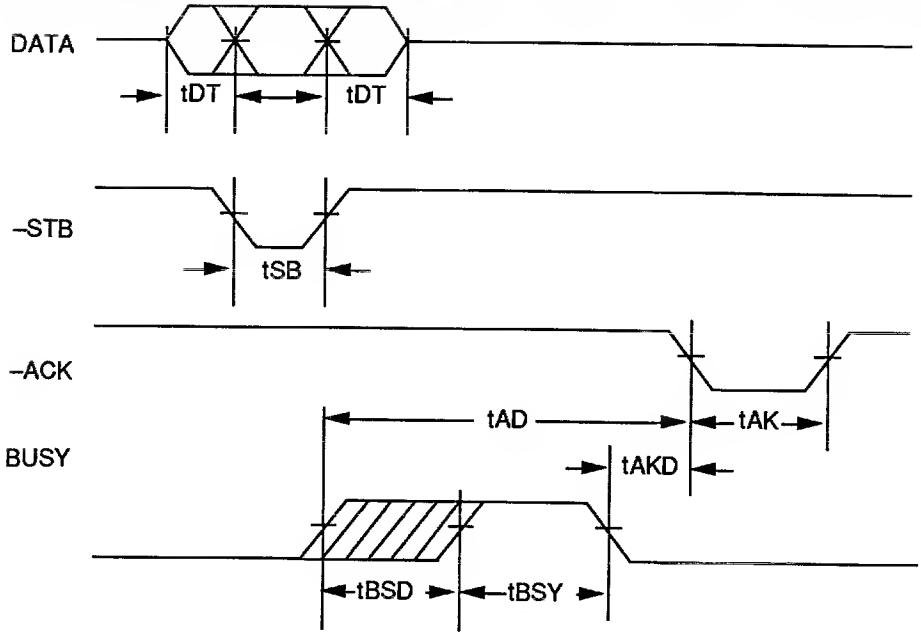
TRANSMITTER TIMING



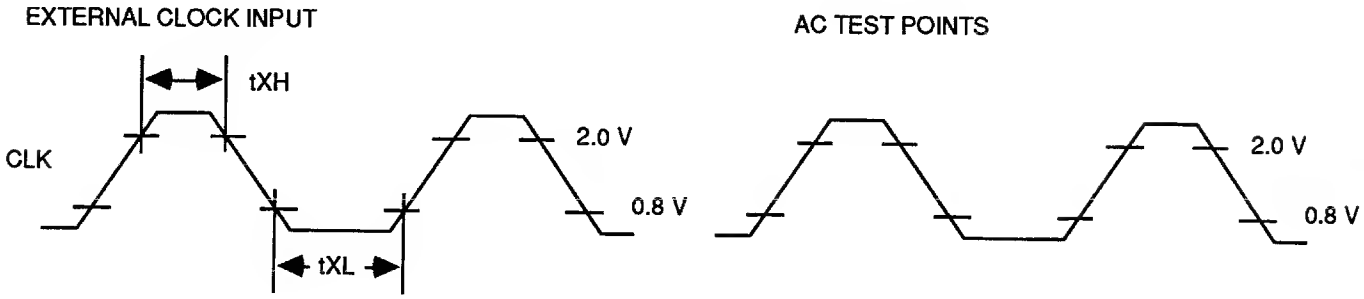
MODEM TIMING



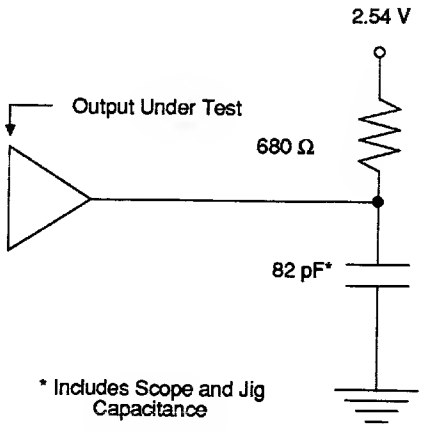
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



6

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VCC +0.3 V
Applied Output Voltage	–0.5 V to VCC +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	–0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0 mA on DB0-DB7 IOL = 12 mA on PD0-PD7 IOL = 10 mA on –INIT, –AFD, –STB, and –SLIN (see Note 1) IOL = 2.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = –0.4 mA on DB0-DB7 IOH = –2.0 mA on PD0-PD7 IOH = –0.2 mA on –INIT, –AFD, –STB, and –SLIN IOH = –0.2 mA on all other outputs
ICC	Power Supply Current		50	mA	VCC = 5.25 V, No loads on SIN, –DSR, –RLSD, –CTS. –RI = 2.0 V. Other inputs = 0.8 V. Baud rate generator = 4 MHz. Baud rate = 56K
IIL	Input Leakage		±10	µA	VCC = 5.25 V, GND = 0 V. All other pins floating.
ICL	Clock Leakage		±10	µA	VIN = 0 V, 5.25 V
IOZ	3-State Leakage		±20	µA	VCC = 5.25 V, GND = 0 V. VOUT = 0 V, 5.25 V 1) Chip deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Note 1. –INIT, –AFD, –STB, and –SLIN are open collector output pins that each have an internal pull-up resistor (2.5 kΩ-3.5 kΩ) to VCC. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V maximum.

VL16C452

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- Dual-channel version of VL16C450
- Centronix printer interface
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus on each channel

DESCRIPTION

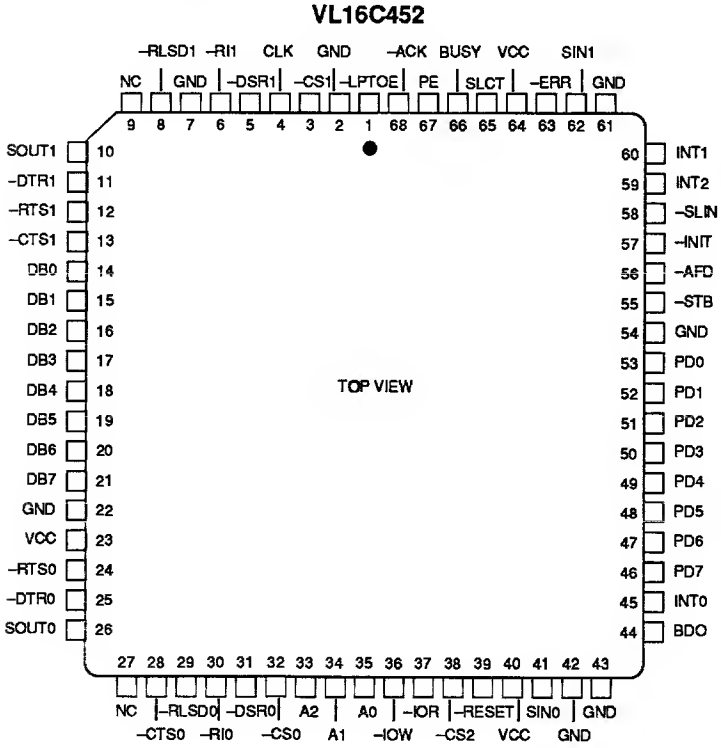
The VL16C452 is an enhanced dual-channel version of the popular VL16C450 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

In addition to its dual communications interface capabilities, the VL16C452 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. The parallel port, together with the two serial ports, provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

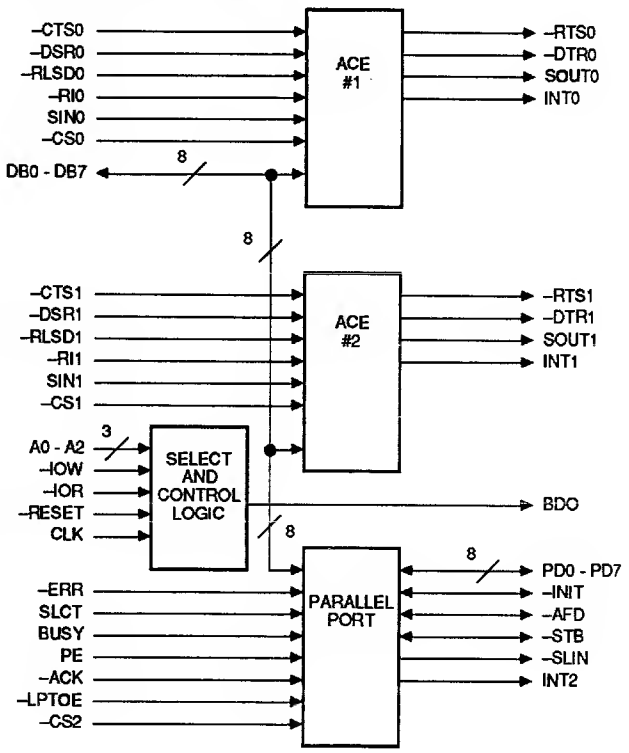
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16} –1).

The VL16C452 is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C452-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–IOR	37	I	Read Strobe - This is an active low input which enables the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2 and Chip Selects.
–IOW	36	I	Input/Output Write Strobe - This is an active low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends upon the register selected by the address inputs A0, A1, A2 and chip selects.
DB0-DB7	14-21	I/O	Data Bits DB0-DB7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL16C452 and the CPU. These lines are normally in a high-impedance state except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	35, 34, 33	I	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels, Table 10 for the decode of the parallel line printer port.
CLK	4	I	Clock Input - The external clock input to the baud rate divisor of each ACE.
SOUT0, SOUT1	26, 10	O	Serial Data Outputs - These lines are the serial data outputs from the ACEs' transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
–CTS0, –CTS1	28, 13	I	Clear to Send Inputs - The logical state of each –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of each ACE. A change of state in either –CTS pin since the previous reading of the associated MSR causes the setting of DCTS [MSR(0)] of each Modem Status Register.
–DSR0, –DSR1	31, 5	I	Data Set Ready Inputs - The logical state of the DSR pins is reflected in MSR(5) of its associated Modem Status Register. DDSR [MSR(1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR.
–DTR0, –DTR1	25, 11	O	Data Terminal Ready Lines - Each DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of its associated ACE. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR pin indicates that its ACE is ready to receive data.
–RTS0, –RTS1	24, 12	O	Request to Send Outputs - An –RTS pin is set low by writing a logic 1 to MCR(1) bit 1 of its UART's Modem Control Register. Both –RTS pins are reset high by Reset. A low on the –RTS pin indicates that its ACE has data ready to transmit. In half duplex operations, –RTS is used to control the direction of the line.
–RI0, –RI1	30, 6	I	Ring Indicator Inputs - The –RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each ACE. The Modem Status Register output TERI [MSR(2)] indicates whether the –RI input has changed from high to low since the previous reading of the MSR.
–LPTOE	1	I	Parallel Data Output Enable - When low, this signal enables the Write Data Register to the PD0-PD7 lines. A high puts the PD0-PD7 lines in the high-impedance state allowing them to be used as inputs. –LPTOE is usually tied low for printer operation.
VCC	23, 40, 64		Power Supply - The power supply requirement is 5 V ±5%.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
GND	2, 7, 22, 42, 43, 54, 61		Ground (0 V) - All pins must be tied to ground for proper operation.
–RLSD0, –RLSD1	29, 8	I	Receive Line Signal Detect - –RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Registers. MSR(3) (DRLSD) of the Modem Status Register indicates whether the –RLSD input has changed since the previous reading of the MSR. –RLSD has no effect on the receiver.
–RESET	39	I	Reset - When low, the reset input forces the VL16C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0, INT1	45, 60	O	Serial Channel Interrupts - Each three-state, serial channel interrupt output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service. Upon reset, the interrupt output will be in the high impedance state.
SIN0, SIN1	41, 62	I	Serial Data Inputs - The serial data inputs move information from the communication line or modem to the VL16C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the Loop Mode.
–CS0, –CS1, –CS2	32, 3, 38	I	Chip Selects - Each input acts as an enable for the write and read signals for the serial channels 0 (–CS0) and 1 (–CS1). –CS2 enables the the signals to the line printer port.
BDO	44	O	Bus Buffer Output - This active high output is asserted when either serial channel or the parallel port is read. This output can be used to control the system bus driver (74LS245).
PD0-PD7	53-46	I/O	Parallel Data Bits (0-7) - These eight lines provide a byte-wide input or output port to the system. They are held in a high-impedance state when –LPTOE is held in the high state.
–STB	55	O	Line Printer Strobe - This open-drain line provides communication between the VL16C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
–AFD	56	O	Line Printer Autofeed - This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
–INIT	57	O	Line Printer Initialize - This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
–SLIN	58	O	Line Printer Select - This open-drain line selects the printer when it is active low.
INT2	59	O	Printer Port Interrupt - This signal is an active high, three-state output, generated by the positive transition of –ACK. It is enabled by bit 4 of the Write Control Register. Upon a reset, the interrupt output will be in the high impedance state.
–ERR	63	I	Line Printer Error - This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
SLCT	65	I	Line Printer Selected - This is an input line from the line printer that goes high when the line printer has been selected.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUSY	66	I	Line Printer Busy - This is an input line from the line printer that goes high when the line printer is not ready to accept data.
PE	67	I	Line Printer Paper Empty - This is an input line from the line printer that goes high when the printer runs out of paper.
–ACK	68	I	Line Printer Acknowledge - This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
NC	9, 27		No Connection

FUNCTIONAL DESCRIPTION

SERIAL CHANNEL REGISTERS

Three types of internal registers are used in each serial channel of the VL16C452. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The VL16C452 data registers are double-buffered so that read and write operations can be performed at the same time the ACE is performing the parallel-to-serial and serial-to-parallel conversion.

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: Serial Channel 0 is accessed when –CS0 is low; Serial Channel 1 is accessed when –CS1 is low. Selecting both channels simultaneously is an invalid condition.

LINE CONTROL REGISTER

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described in Figure 1.

LCR (0) and LCR(1) word length select bits: (See Figure 1.)

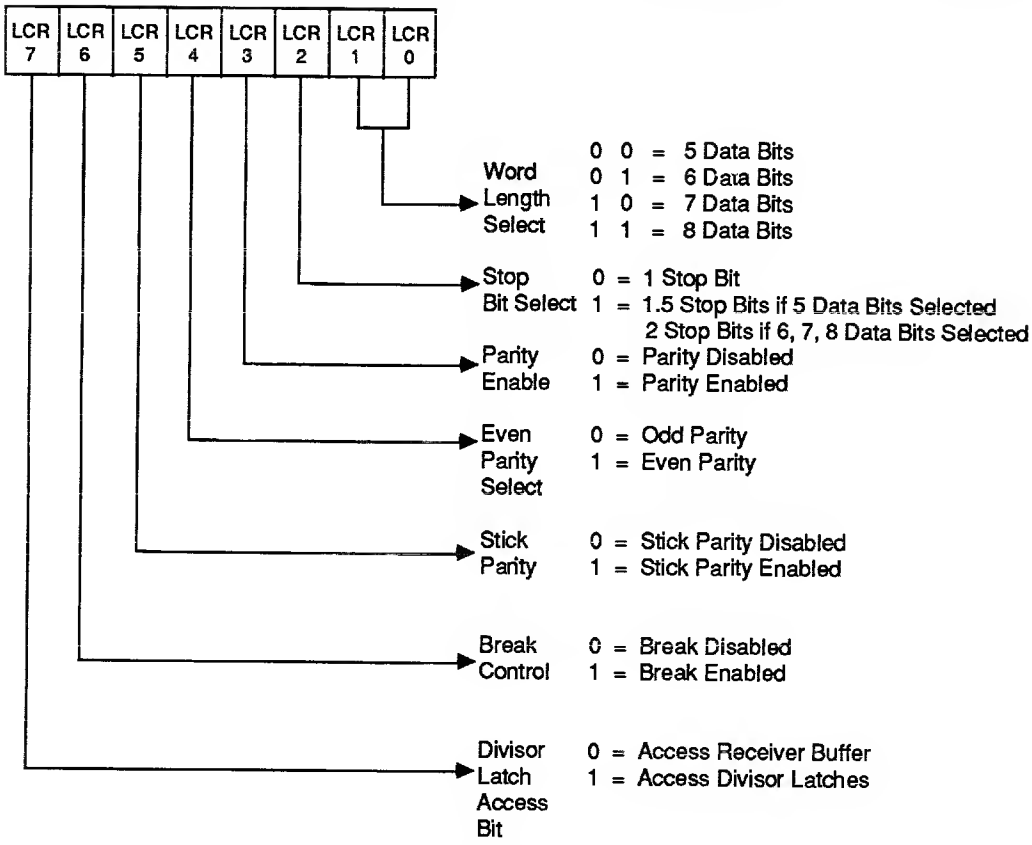
LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver always checks for one stop bit.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from

FIGURE 1. LINE CONTROL REGISTER



the value of LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), and clear break when normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

LINE STATUS REGISTER

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the VL16C452.

Four error flags OE, FE, PE and BI provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred.

The contents of the Line Status Register shown in Table 2 are described below.

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit [LCR(4)]. The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + pairty + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1)-LSR(4) are the error conditions that produce a Reciever Line Status interrupt [priority 1 interrupt in the Interrupt Identification Register (IIR)] when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE, and BI).

LSR(5) Transmitter Holding Register Empty (THRE): THRE shows that the serial channel is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled [IER(1)=1]. THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

MODEM CONTROL REGISTER

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 2. The MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins.

MCR(0): When MCR(0) is set high, the –DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs (–CTS, –DSR, –RLSD and –RI) are disconnected. The modem control inputs are internally connected to the first four bits of the modem control register. The modem control output pins are forced to their inactive state (high). In the Loop Mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Bits MCR(5)-MCR(7) are permanently set to logic 0.

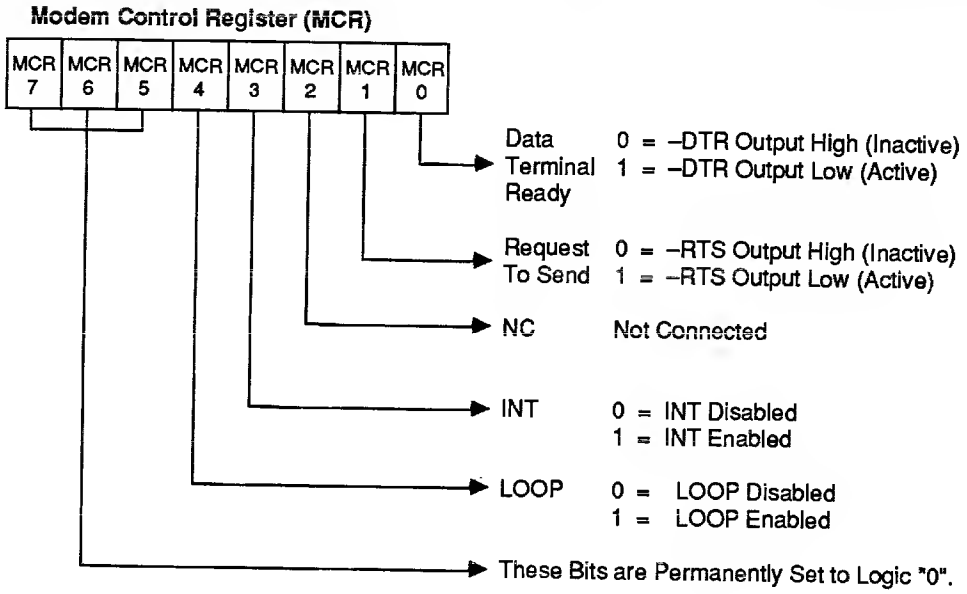
MODEM STATUS REGISTER

The MSR provides the CPU with status of the modem input lines from the

TABLE 3. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DRLSD	Delta Receive Line Signal Detect
MSR (4)	–CTS	Clear To Send
MSR (5)	–DSR	Data Set Ready
MSR (6)	–RI	Ring Indicator
MSR (7)	–RLSD	Receive Line Signal Detect

FIGURE 2. MODEM CONTROL REGISTER



modem or peripheral devices. The modem input lines for each channel are –CTS, –DSR, –RI, and –RLSD. MSR(4)-MSR(7) are status indications of these lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3. Note that the state (high or low) of the status bits are inversions of the input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on –RI do not activate TERI.

MSR(3) Delta Receive Line Signal Detect (DRLSD): DRLSD indicates that the –RLSD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the complement of the CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in Loop Mode [MCR(4)=1], MSR(4) is equivalent to MCR(1).

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is the complement of the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the Loop Mode [MCR(4)=1], MSR(5) is equivalent to MCR(0).

MSR(6) Ring Indicator: Is the complement of the RI input. If the channel is in the Loop Mode [MCR(4)=1], MSR(6) is equivalent to MCR(2).

MSR(7) Receive Line Signal Detect : Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (–RLSD) input . If the channel is in the Loop Mode [MCR(4)=1], MSR(4) is equivalent to MCR(3).

The modem status inputs (–RI, –RLSD, –DSR, and –CTS) reflect the modem input lines with any change of status.

Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD is true, and a state change occurs during a read operation (–IOR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD is false and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read –IOR operations. If a status condition is generated during a read –IOR operation, the status bit is not set until the trailing edge of the read –IOR.

If a status bit is set during a read –IOR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read –IOR instead of being set again.

DIVISOR LATCHES

Each VL16C452 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch

registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

SCRATCHPAD REGISTER

Scratchpad Register is an 8-bit Read/ Write register that has no effect on any channel in the VL16C452. It is intended to be used by the programmer to hold data temporarily.

INTERRUPT IDENTIFICATION REGISTER

The Interrupt Identification Register (IIR) of each serial channel of the VL16C452 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). The IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 4 and are described below.

IIR(0): IIR(0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

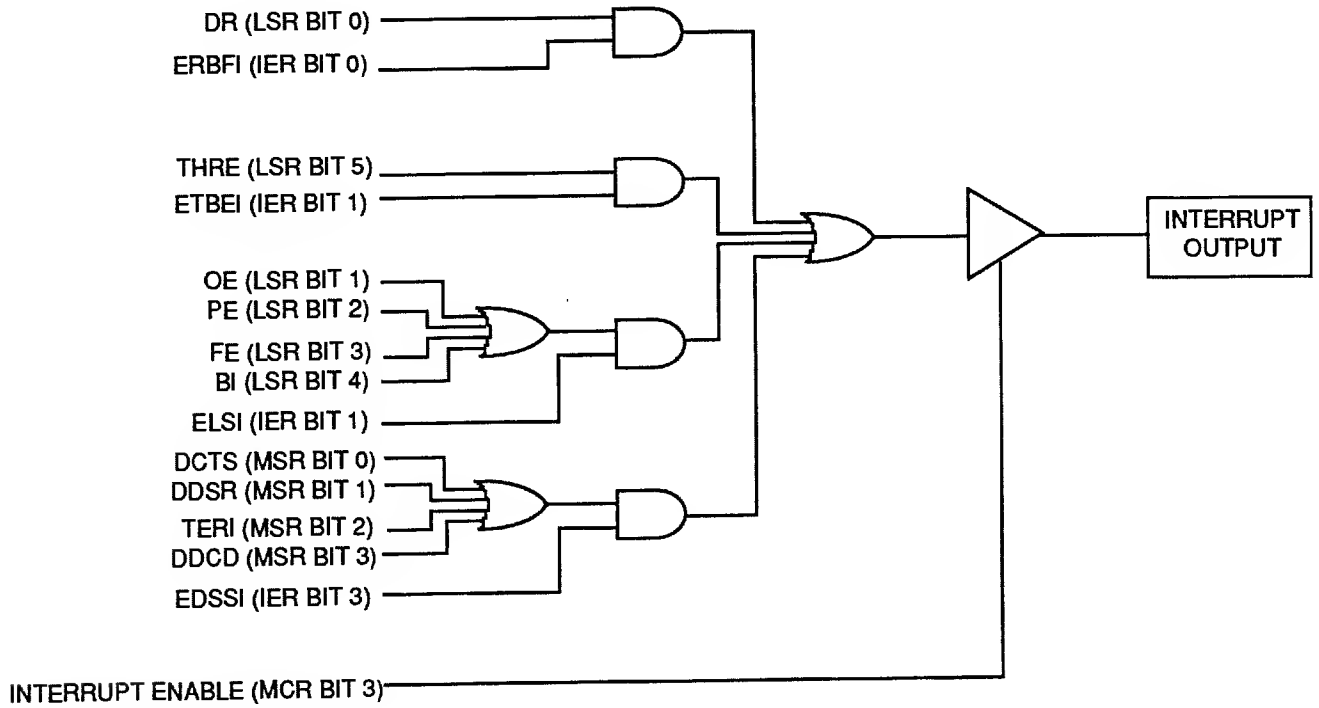
The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0)-IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Figure 3 and below:

IER(0): When programmed high [IER(0)=Logic 1], IER(0) enables Received Data Available interrupt.

IER(1): When programmed high [IER(1)=Logic 1], IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high [IER(2)=Logic 1], IER(2) enables the Receiver Line Status interrupt.

FIGURE 3. INTERRUPT CONTROL LOGIC



IER(3): When programmed high [IER(3)=Logic 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5K bps are available. Tables 5, 6 and 7 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the VL16C452 –RESET input should be held low for 500 ns to reset the VL16C452 circuits to an idle mode until initialization. A low on –RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (Reset high), the VL16C452 remains in the idle mode until programmed.

A hardware reset of the VL16C452 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the VL16C452 is given in Table 8.

PROGRAMMING

Each serial channel of the VL16C452 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the VL16C452 serial channel is not transmitting or receiving data.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the VL16C452 is 3.1 MHz.

6

TABLE 4. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	–CTS, –DSR –RI, –RLSD	MSR Read

X = Not Defined.

TABLE 5. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 6. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	–
75	2048	–
110	1396	0.026
134.5	1142	0.0007
150	1024	–
300	512	–
600	256	–
1200	128	–
1800	85	0.392
2000	77	0.260
2400	64	–
3600	43	0.775
4800	32	–
7200	21	1.587
9600	16	–
19200	8	–
38400	4	–

TABLE 7. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 8. RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Are Permanently Low
Line Control Register	Reset	All Bits Low
Modem Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–OUT2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–OUT1	Reset	High

DEVICE APPLICATION

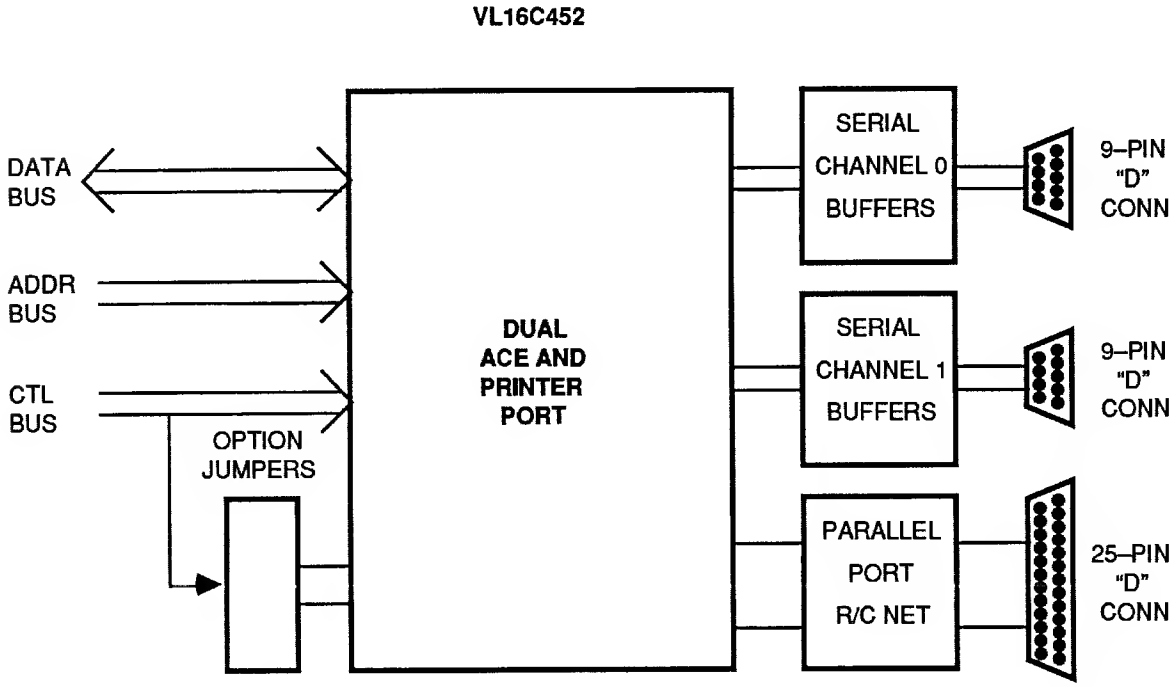


TABLE 9. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	INT	NC	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DRLSD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

PARALLEL PORT REGISTERS

The VL16C452's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (–CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (–IOR) and write (–IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (BUSY), Acknowledge (–ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (–ERR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In (–SLIN), Initialize the Printer (–INIT), Autofeed the Paper (–AFD), Strobe (–STB), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 10. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BUSY	–ACK	PE	SLCT	–ERR	1	1	1
Read Control	1	1	1	IRQ ENB	–SLIN	–INIT	–AFD	–STB
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	–SLIN	–INIT	–AFD	–STB

TABLE 11. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
–IOR	–IOW	–CS2	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

AC CHARACTERISTICS: TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle	360		ns	
tDDD	Delay from –IOR to Data		125	ns	100 pF Load
tHZ	–IOR to Floating Data Delay	0	100	ns	100 pF Load, Note 4
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle	360		ns	
tDS	Data Setup Time	40		ns	
tDH	Data Hold Time	40		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 2
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 2
tAR	–IOR Delay from Address	60		ns	Note 2
tCSR	–IOR Delay from Chip Select	50		ns	Note 2
tWA	Address Hold Time from–IOW	20		ns	Note 2
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 2
tAW	–IOW Delay from Address	60		ns	Note 2
tCSW	–IOW Delay from Select	50		ns	Note 2
tRW	Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

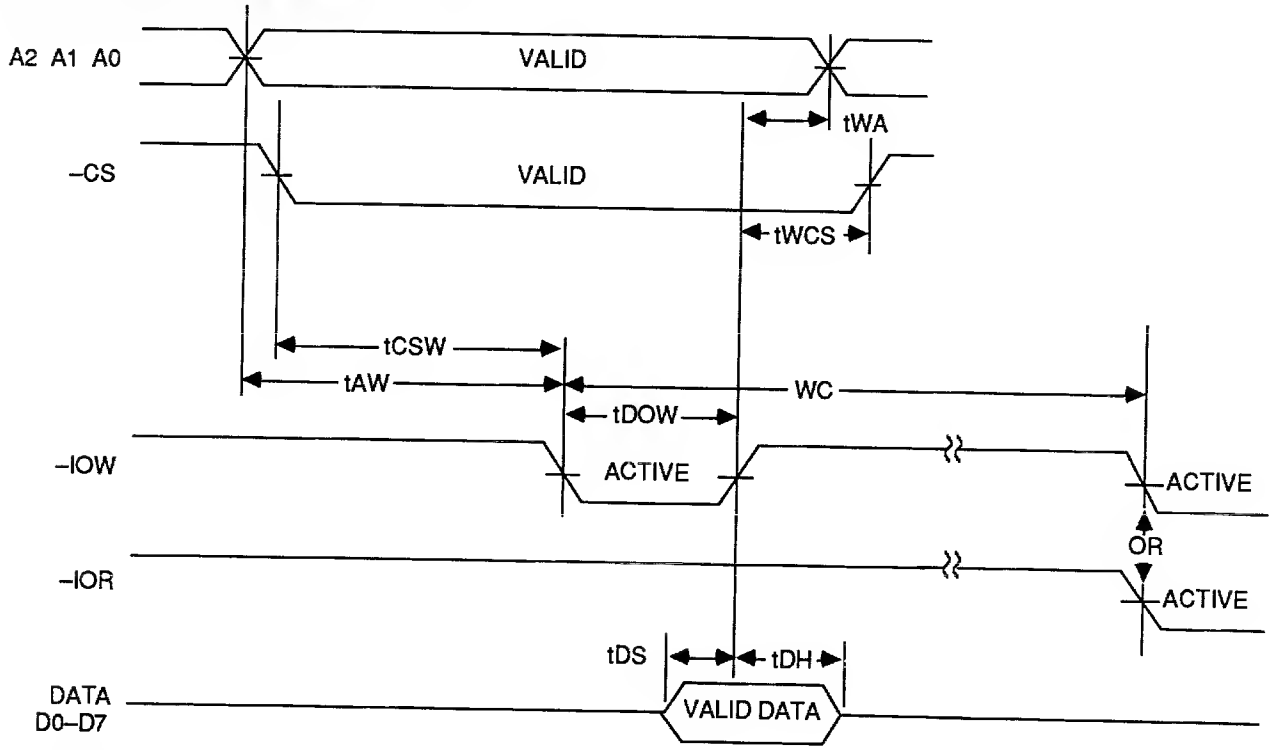
Notes:
1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1. (See AC Test Points.)
6. RCLK is internally derived from the internal –BAUDOUT signal.

AC CHARACTERISTICS (Cont.): TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

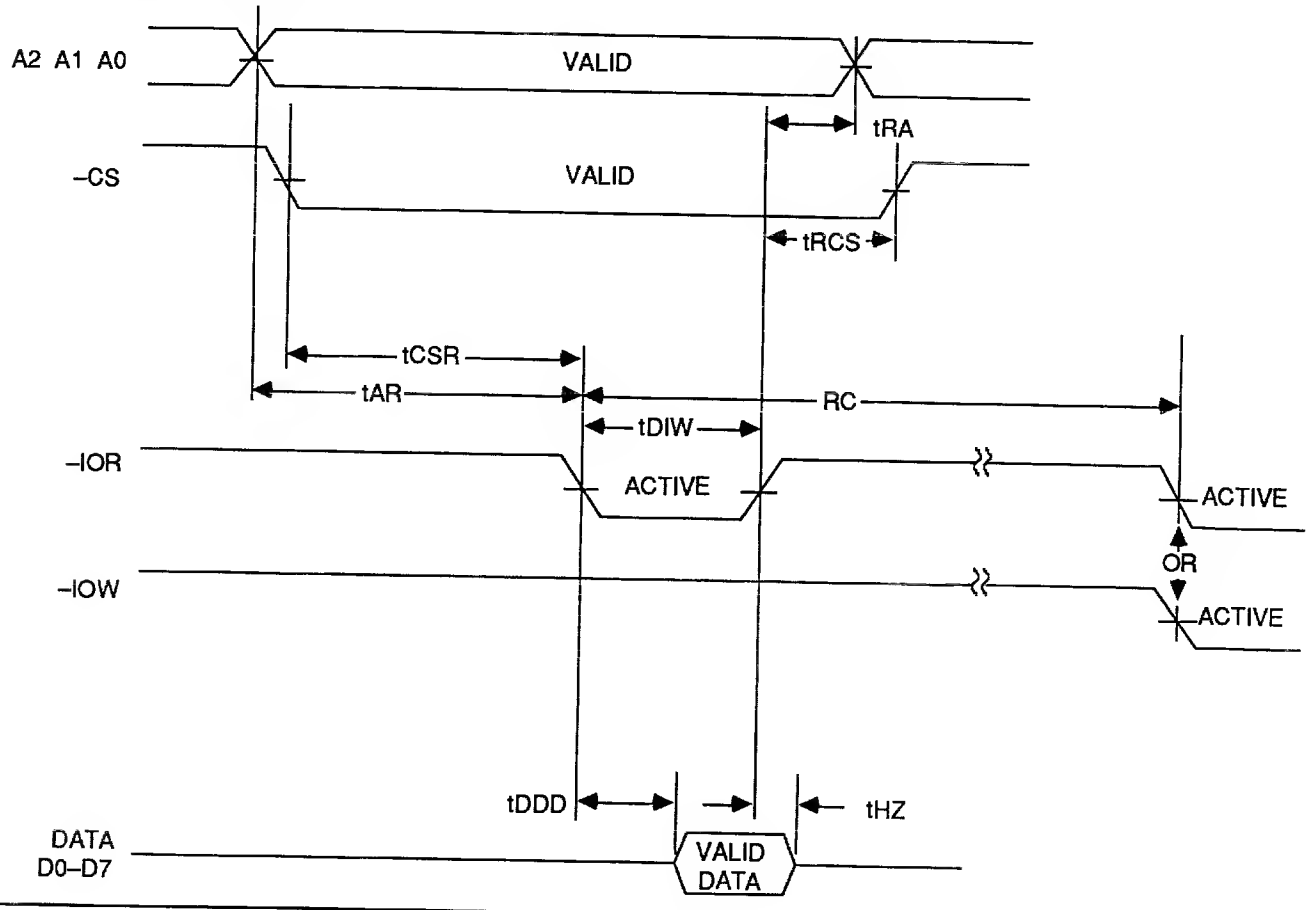
Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of –IOW (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		16	CLK Cycles	Note 3
tSI	Delay from Initial Write to Interrupt	8	24	CLK Cycles	Note 3
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 3
tIR	Delay from –IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
tMDO	Delay from –IOW (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –IOR (RS MSR)		250	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 3
tRINT	Delay from –IOR (RD RBR/RDLSR) to Reset Interrupt		1	µs	100 pF Load
Parallel Port					
tDT	Data Time	1		µs	
tSB	Strobe Time	1	500	µs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			µs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			µs	Defined by Printer
tAK	Acknowledge Duration Time			µs	Defined by Printer
tBSY	Busy Duration Time			µs	Defined by Printer
tBSD	Busy Delay Time			µs	Defined by Printer

Notes:
1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC Test Points).

WRITE CYCLE TIMING

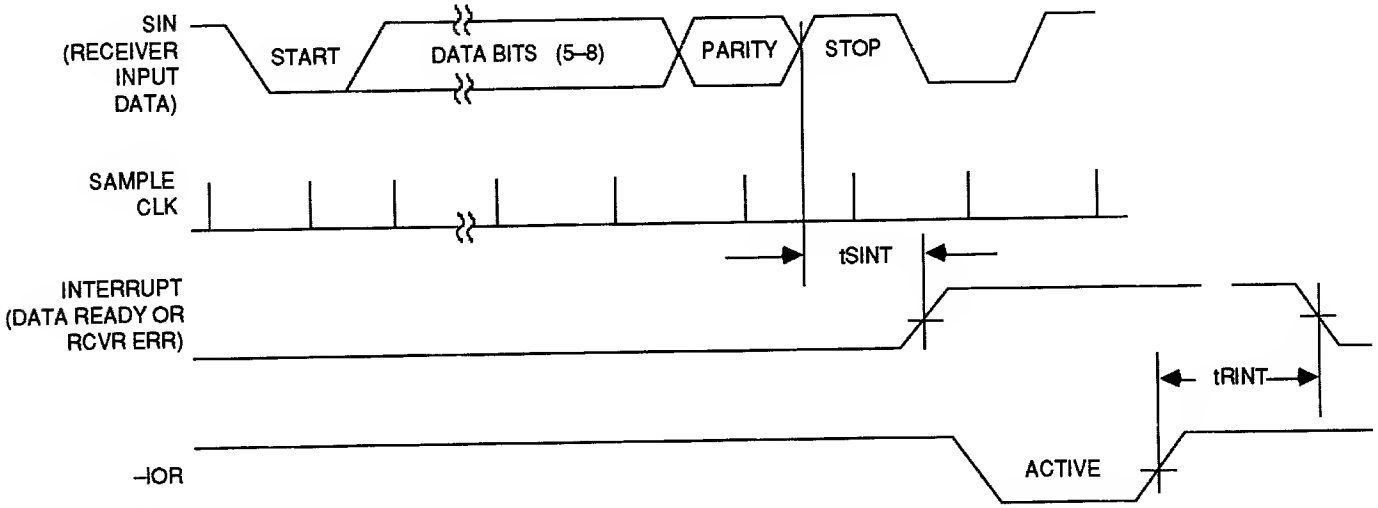


READ CYCLE TIMING

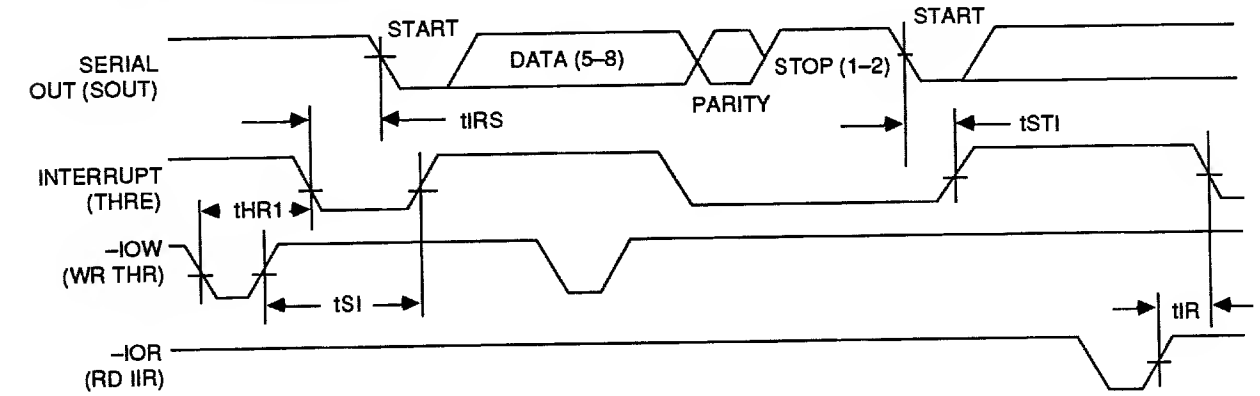


6

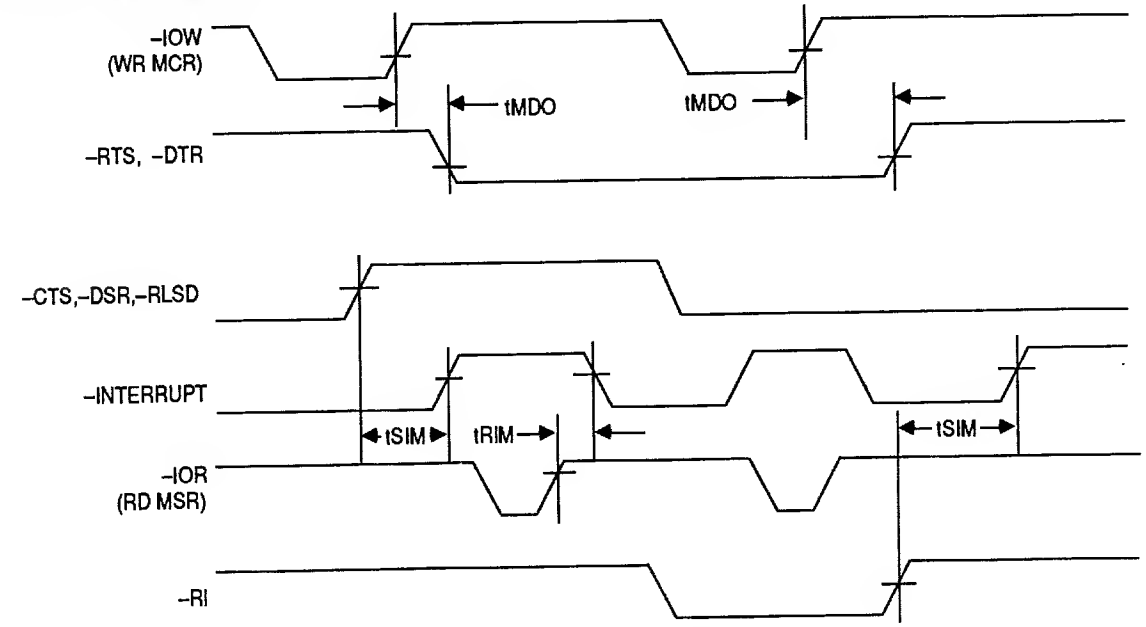
RECEIVER TIMING



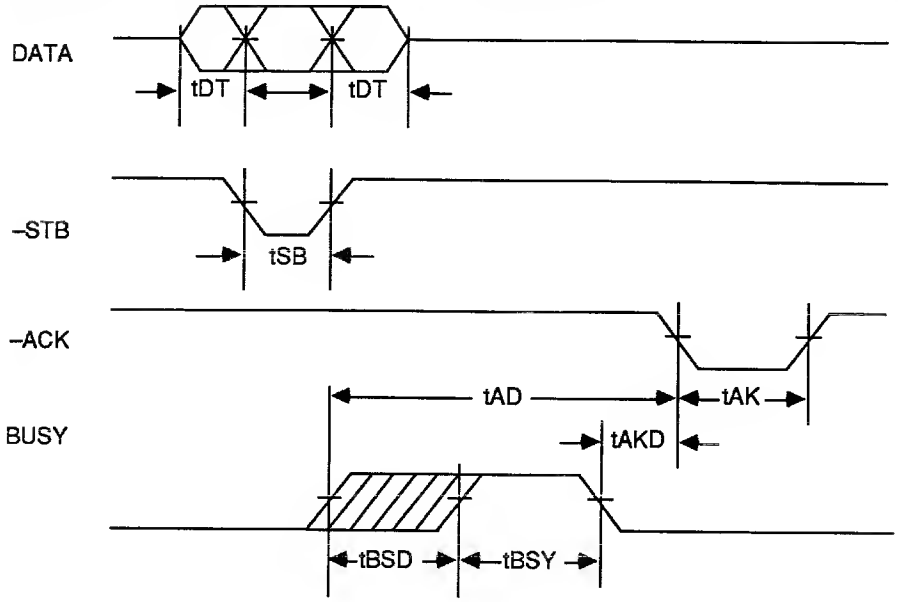
TRANSMITTER TIMING



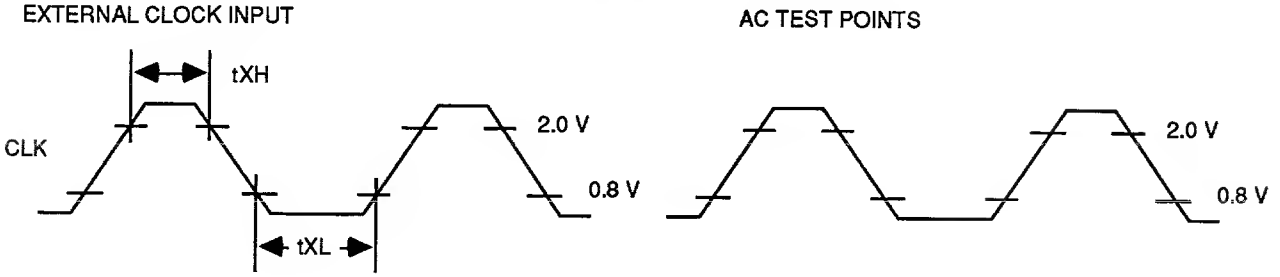
MODEM TIMING



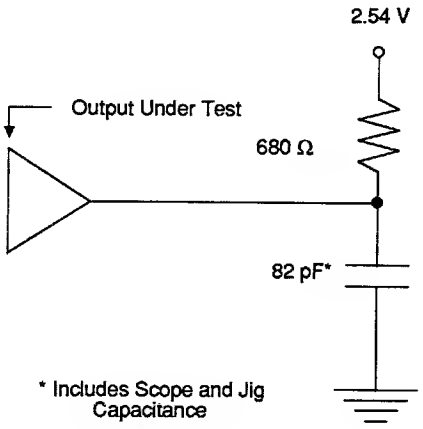
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to +70°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to VCC +0.3 V
Applied Output Voltage	–0.5 V to VCC +0.3 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70°C, VCC = 5 V ± 5%

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	–0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0 mA on DB0 - DB7 IOL = 12 mA on PD0 - PD7 IOL = 10 mA on –INIT, –AFD, –STB, and –SLIN (see Note 1) IOL = 2.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = –0.4 mA on DB0 - DB7 IOH = –2.0 mA on PD0 - PD7 IOH = –0.2 mA on –INIT, –AFD, –STB, and –SLIN IOH = –0.2 mA on all other outputs
ICC	Power Supply Current		50	mA	VCC = 5.25 V. No loads on SIN0,1; –DSR0,1; –RLSD0,1; –CTS0,1. –RI0, –RI1 = 2.0 V. Other inputs = 0.8 V. Baud rate generator = 4 MHz. Baud rate = 56K
IIL	Input Leakage		±10	µA	VCC = 5.25 V, GND = 0 V. All other pins floating.
ICL	Clock Leakage		±10	µA	VIN = 0 V, 5.25 V
IOZ	3-State Leakage		±20	µA	VCC = 5.25 V, GND = 0 V. VOUT = 0 V, 5.25 V 1) Chip deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Note 1. –INIT, –AFD, –STB, and –SLIN are open collector output pins that each have an internal pull-up resistor (2.5 kΩ-3.5 kΩ) to VCC. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V Max.

VL16C550

ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFOs

FEATURES

- Fully compatible with VL16C450 ACE
- 16 byte FIFO reduces CPU interrupts
- Full double buffering
- Modem control signals include –CTS, –RTS, –DSR, –DTR, –RI and –DCD
- Programmable serial characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd-, or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
  - Baud rate generation (DC to 256K baud)
- Independent control of transmit, receive, line status, data set interrupts, FIFOs
- Full status reporting capabilities
- Three-state, TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTIONS

The VL16C550 is an asynchronous communications element (ACE) that is functionally equivalent to the VL16C450, and additionally incorporates two 16 byte FIFOs. The FIFOs are available on both the transmitter and receiver, and can be activated by placing the device in the FIFO mode. After a reset, the registers of the VL16C550 are identical to those of the VL16C450.

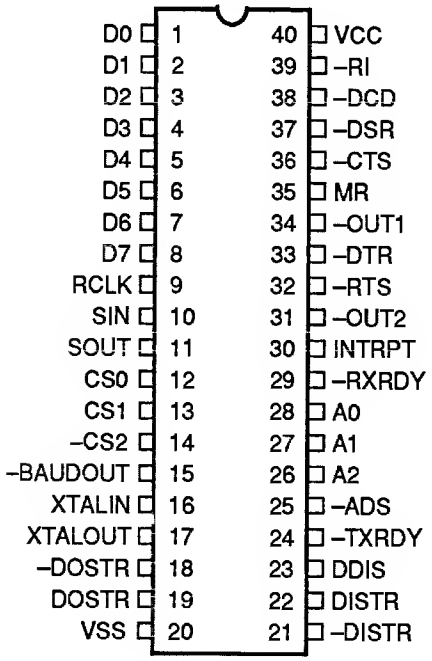
Improved VL16C550 specifications provide compatibility with most newer state-of-the-art CPUs. The VL16C550 serves as a serial data input/output interface in microcomputer systems. It performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. In the FIFO mode, FIFOs are enabled permitting 16 bytes to be stored in both transmit and receive mode. The receive FIFO also provides three bits per byte of error status. The complete status of the VL16C550 can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing, or break interrupt.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

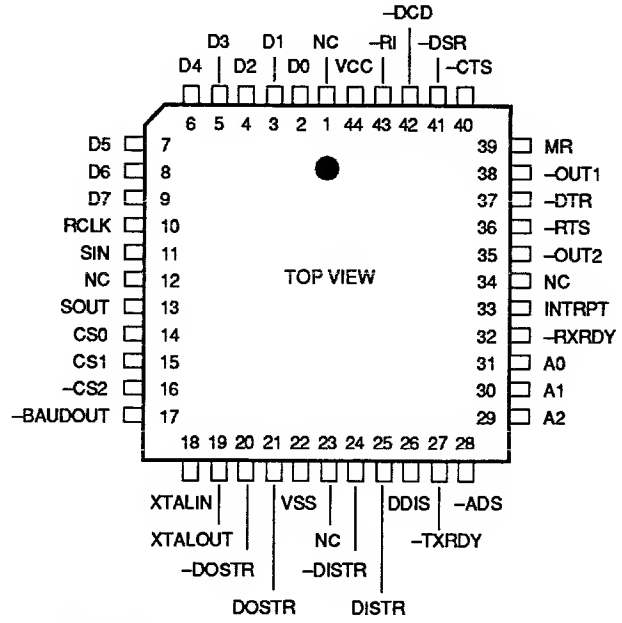
The VL16C550 ACE with FIFOs is available in plastic DIP as well as a PLCC.

PIN DIAGRAMS

VL16C550



VL16C550

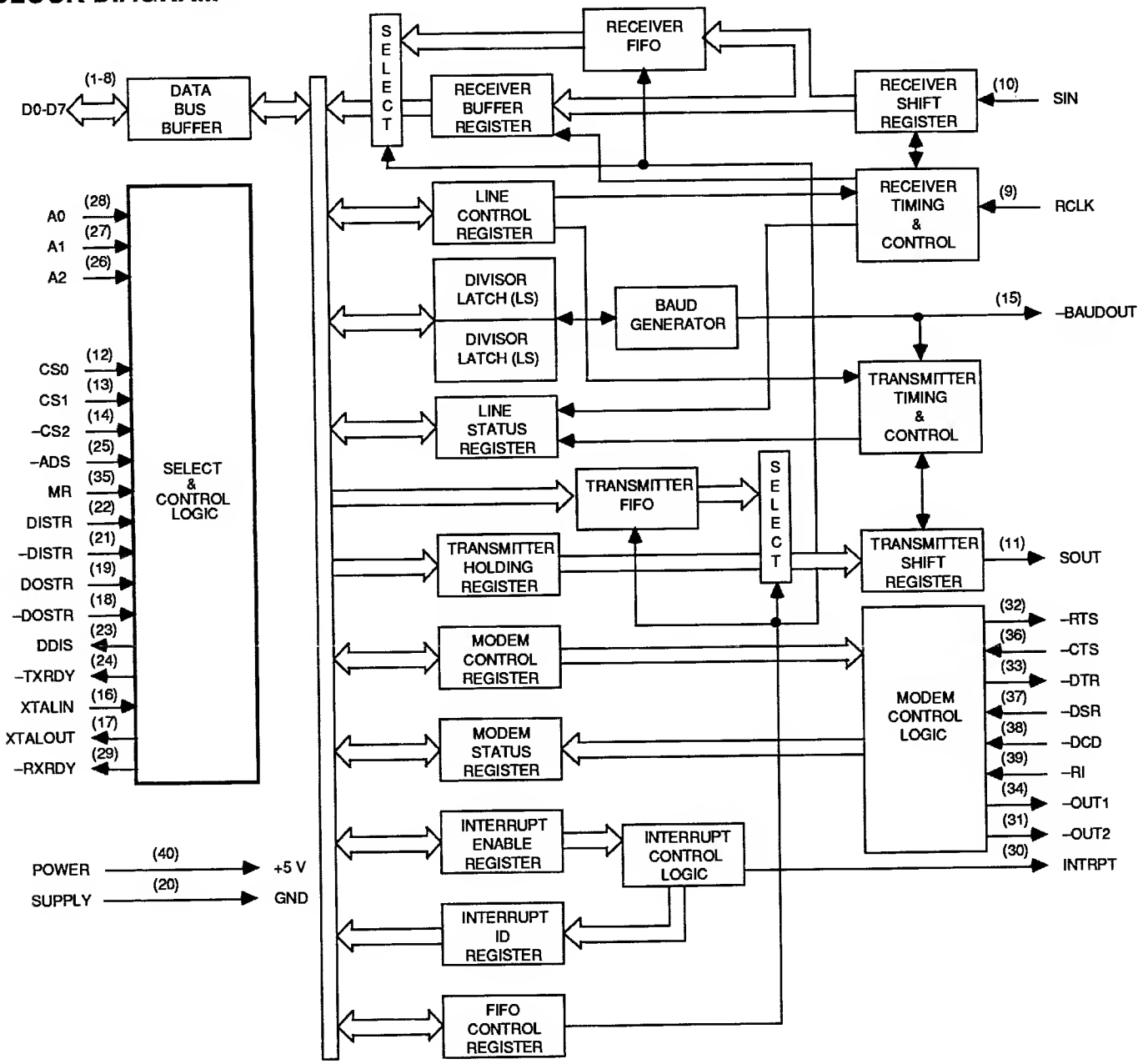


ORDER INFORMATION

Part Number	External Clock Frequency	Package
VL16C550-PC VL16C550-QC	8 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
D0-D7	1-8	I/O	Data Bits 0 through 7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the ACE and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
RCLK	9	I	Receive Clock Input - The external clock input to the ACE receiver logic (16X SIN data rate).
SIN	10	I	Serial Data Input - The serial data input moves information from the communication line or modem to the ACE receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data input is disabled when operating in the Loop Mode.
SOUT	11	O	Serial Data Output - This line is the serial data output from the ACE. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). SOUT is held in the mark condition when the transmitter is disabled, Master Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
CS0, CS1, –CS2	12-14	I	Chip Selects - The Chip Select inputs act as an enable for the device. When –CS2 is low and CS0 and CS1 are both high, the chip is selected.
–BAUDOUT	15	O	Baud Rate Output - This output signal is equal to the internal reference frequency, divided by the selected divisor.
XTALIN	16	I	Crystal Input - Input for external timing reference input or crystal (See Figure 3-Basic Configuration).
XTALOUT	17	O	Crystal Output - Output pin when using crystal circuit. (See Figure 3-Basic Configuration).
–DOSTR	18	I	Write Strobe - This is an active low input which causes data from the data bus (D0-D7) to be input to the ACE.
DOSTR	19	I	Write Strobe - Same as –DOSTR, but uses an active high input.
VSS	20		Ground (0 V).
–DISTR	21	I	Read Strobe - This is an active low input which causes the ACE to output data to the data bus (D0-D7).
DISTR	22	I	Read Strobe - Same as –DISTR, but uses an active high input.
DDIS	23	O	Driver Disable - This pin goes low whenever the microprocessor is reading data from the ACE. This signal may be used to control an external transceiver.
–TXRDY	24	O	Transmitter Ready - Two types of DMA signaling are available. Either can be selected via FCR3 when operating in the FIFO Mode. Only DMA Mode 0 is allowed when operating in the VL16C450 Mode. Single transfer DMA (a transfer is made between CPU bus cycles) is supported by Mode 0. Multiple transfers that are made continuously until the XMIT FIFO has been filled are supported by Mode 1. Mode 0 - Once –TXRDY is activated it will go inactive after the first character is loaded into the holding register or XMIT FIFO. In the FIFO Mode (FCR0=1, FCR3=0) [(FCR0=0) for VL16C450 Mode] with no characters in the XMIT holding register or XMIT FIFO, –TXRDY will be active low. Mode 1 - –TXRDY will go active low if in the FIFO Mode (FCR0=1) when FCR3=1 and there is a minimum of one unfilled position in the XMIT FIFO. When the XMIT FIFO is completely full, –TXRDY will go inactive.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–ADS	25	I	Address Strobe Input - When this pin is low, the state of the Register Select and Chip Select pins is latched internally.
A0-A2	28-26	I	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations.
–RXRDY	29	O	Receiver Ready - Receiver DMA signaling is also available through this pin (pin 24 also has DMA signaling capabilities). One of two types of DMA signaling can be selected via FCR3 when operating in the FIFO Mode. Only DMA Mode 0 is allowed when operating in the VL16C450 Mode. For single transfer DMA (a transfer is made between CPU bus cycles), Mode 0 is used. Multiple transfers that are made continuously until the RCVR FIFO has been emptied are supported by Mode 1. Mode 0 - The –RXRDY pin will be active low when in the FIFO Mode (FCR0=1, FCR3=0) or [(FCR0=0) when in the VL16C450 Mode] and the RCVR FIFO or RCVR holding register contain at least one character. When there are no more characters in the FIFO or holding register the –RXRDY pin will go inactive. Mode 1 - The –RXRDY will go low in the FIFO Mode (FCR0=1) when the FCR3=1 and the timeout or trigger levels have been reached. It will go inactive when the FIFO or holding register is empty.
INTRPT	30	O	Interrupt Output - This pin goes high (when enabled by the Interrupt Enable Register) whenever a Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty, Modem Status condition or timeout (FIFO Mode) is detected.
–OUT2	31	O	Output 2 - This output that can be set to an active low by programming bit 3 of the Modem Control Register to a high level. This signal is cleared (high) by writing a logic 0 to the OUT2 bit (MCR) or whenever a Master Reset occurs.
–RTS	32	O	Request to Send - The –RTS pin is set low by writing a logic 1 to MCR bit 1 of the ACE's Modem Control Register. The –RTS pin is reset high by writing a logic 0 to MCR bit 1 or by Master Reset. A low on the –RTS pin indicates that the ACE has data ready to transmit.
–DTR	33	O	Data Terminal Ready - The –DTR pin can be set (low) by writing a logic 1 to MCR, Modem Control Register bit 0 of the ACE. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR) or whenever a Master Reset occurs. When active (low), the –DTR pin indicates that the ACE is ready to receive data.
–OUT1	34	O	Output 1 - This output can be set to an active low by programming bit 2 of the Modem Control Register to a high level. This signal is cleared (high) by writing a logic 0 to the OUT1 bit (MCR) or whenever a Master Reset occurs.
MR	35	I	Master Reset - When high, the reset input forces the ACE into an idle mode in which all data activities are suspended. The Modem Control Register (MCR) along with its output, is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume activities.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–CTS	36	I	Clear to Send - The logical state of the –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of the ACE. A change of state of the –CTS pin, since the previous reading of the MSR, causes the setting of DCTS in the Modem Status Register.
–DSR	37	I	Data Set Ready - The logical state of the –DSR pin is reflected in MSR(5) of the Modem Status Register. DDSR MSR(1) indicates whether the –DSR pin has changed state since the previous reading of the MSR.
–DCD	38	I	Data Carrier Detect - –DCD is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the Modem Status Register. MSR(3) (DDCD) of the Modem Status Register indicates whether the –DCD input has changed since the previous reading of the MSR. –DCD has no effect on the receiver.
–RI	39	I	Ring Indicator Input - The –RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the ACE. The Modem Status Register output TERI MSR(2) indicates whether the –RI input has changed from high to low since the previous reading of the MSR.
VCC	40		Power Supply - The power supply requirement is 5 V ±5%.

REGISTERS

Three types of internal registers are used in the ACE (Control, Status and Data). The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control Register. The status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double-buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

LINE CONTROL REGISTER

The format of the data character is controlled by the Line Control Register. The LCR may be read. Its contents are described below and shown in Figure 1.

6

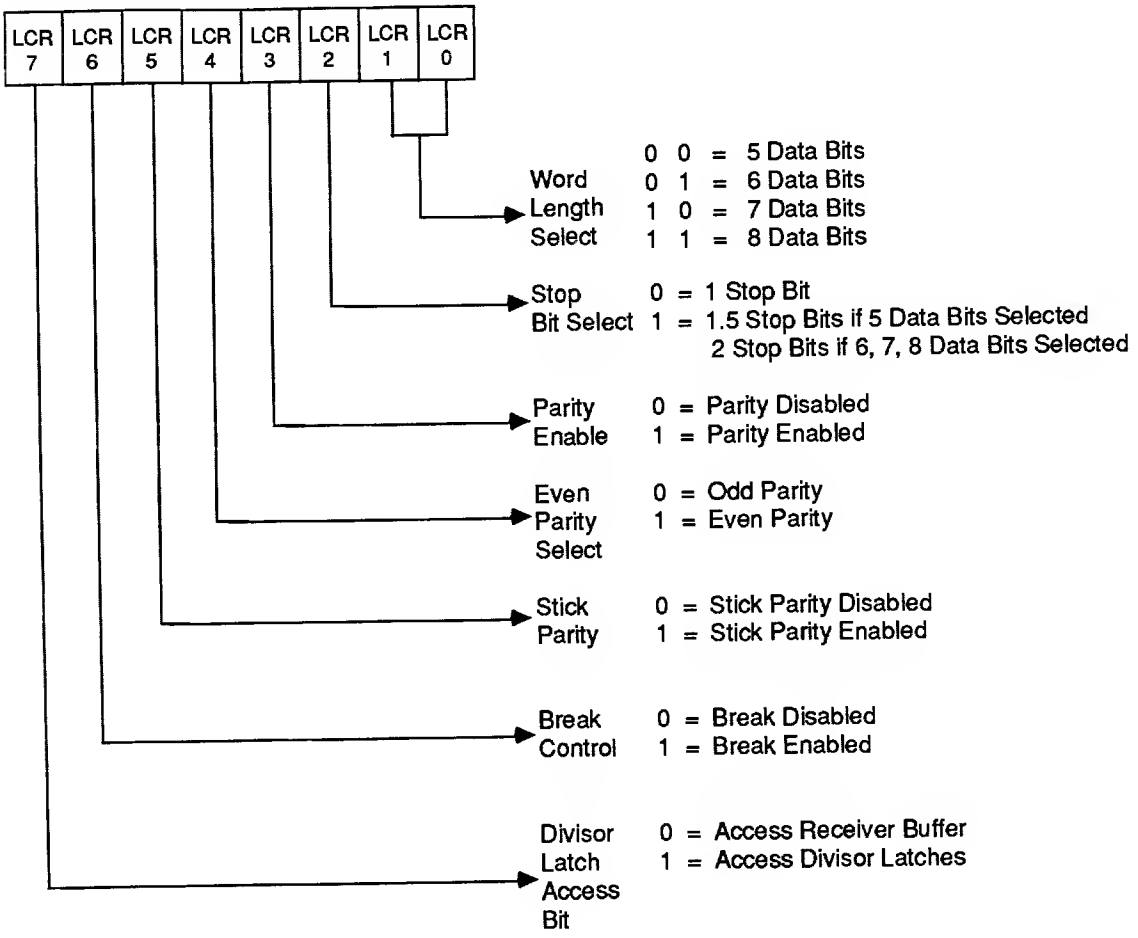
TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The serial channel is accessed when CS0 is low.

FIGURE 1. LINE CONTROL REGISTER



LCR(0) and LCR(1) Word Length Select bit 1: The number of bits in each serial character is programmed as shown in Figure 1.

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. See Figure 1. The receiver always checks for one stop bit.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When enabled a one selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This forces parity to a known state and allows the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The Break Control bit acts only on SOUT and does not effect the transmitter logic. If the following sequence is used, no invalid characters will be transmitted because of the break.

1. Load all "0"s pad character in response to THRE.
2. Set the break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), then clear the break when the normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB); LCR(7) must be set high (logic 1) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation.

LCR(7) must be input low (logic 0) to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

LINE STATUS REGISTER

The Line Status Register (LSR) is a single register that provides status indications.

The Line Status Register shown in Table 2 is described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register or the FIFO.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	1	0
LSR(0) Data Ready (DR)	Ready	Not Ready
LSR(1) Overrun Error (OE)	Error	No Error
LSR(2) Parity Error (PE)	Error	No Error
LSR(3) Framing Error (FE)	Error	No Error
LSR(4) Break Interrupt (BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR(6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR(7) RCVR FIFO Error	Error in FIFO	No Error in FIFO

Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

An overrun error will occur in the FIFO Mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO but it is overwritten.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct parity, as selected by LCR(3) and LCR(4). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

In the FIFO Mode, the Parity Error is associated with a particular character in the FIFO. LCR(2) reflects the error when the character is at the top of the FIFO

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR. In the FIFO Mode, the Framing Error is associated with a particular character in the FIFO. LCR(3) reflects the error when the character is at the top of the FIFO.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

In the FIFO Mode this is associated with a particular character in the FIFO. LCR(2) reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR(1)-LSR(4) are the error conditions that produce a Receiver Line Status interrupt [priority 1 interrupt in the Interrupt Identification Register (IIR)] when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR. In the FIFO Mode when the XMIT FIFO is empty this bit is set. It is cleared when one byte is written to the XMIT FIFO.

When the THRE interrupt is enabled IER(1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR. In the FIFO Mode, when both the transmitter FIFO and shift register are empty this bit is set to one.

LSR(7) This bit is always 0 in the VL16C450 Mode. In FIFO Mode, it is set when at least one of the following data errors is in the FIFO: Parity Error, Framing Error or Break Interrupt indication.

FIFO CONTROL REGISTER

This write only register is at the same location as the IIR. It is used to enable and clear the FIFOs, set the trigger level of the RCVR FIFO, and select the type of DMA signaling.

FCR(0=1) enables both the XMIT and RCVR FIFOs). All bytes in both FIFOs can be cleared by resetting FCR(0). Data is cleared automatically from the FIFOs when changing from FIFO Mode to VL16C450 Mode and vice versa. Programming of other FCR bits is enabled by setting FCR(0)=1.

FCR(1)=1 clears all bytes in the RCVR FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR(2)=1 clears all bytes in the XMIT FIFO and resets the counter logic to 0. This does not clear the shift register.

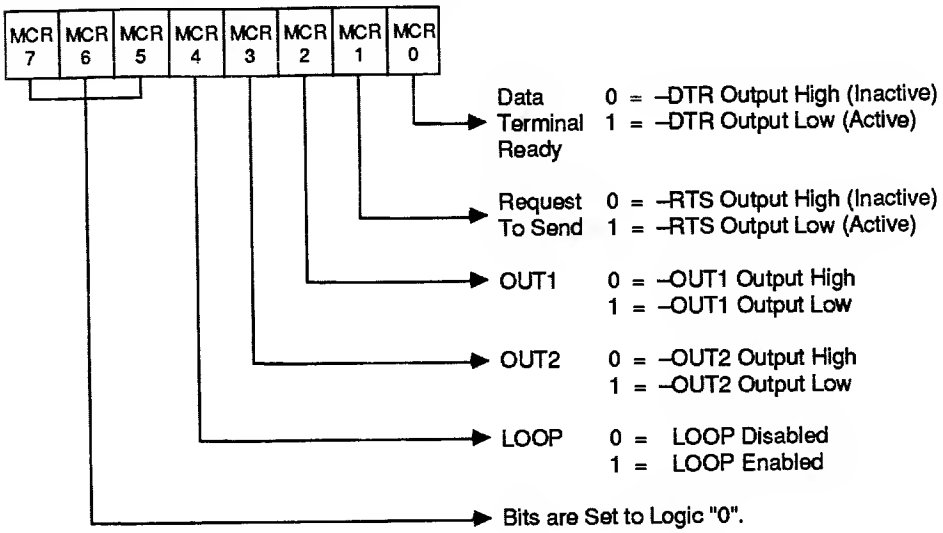
FCR(3)=1 will change the –RXRDY and –TXRDY pins from Mode 0 to Mode 1 if FCR(0)=1.

FCR(4)-FCR(5): These two bits are reserved for future use.

FCR(6)-FCR(7): These two bits are used for setting the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

FIGURE 2. MODEM CONTROL REGISTER



MODEM CONTROL REGISTER

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Figure 2. MCR can be written and read. The –RTS and –DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 2, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the –DTR output is forced low. When MCR(0) is reset low, the –DTR output is forced high. The –DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the –RTS output is forced low. When MCR(1) is reset low, the –RTS output is forced high. The –RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(2): When MCR (2) is set high –OUT1 is forced low.

MCR(3): When MCR(3) is set high, the –OUT2 output is forced low.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic 1) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs (–CTS, –DSR, –DCD, and –RI) are disconnected. The modem control outputs (–DTR, –RTS, –OUT1 and –OUT2) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high) on the VL16C450.

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel.

Bits MCR(5)-MCR(7) are permanently set to logic 0.

MODEM STATUS REGISTER

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are –CTS, –DSR, –RI, and –DCD. MSR(4)-MSR(7) are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], an interrupt is generated whenever MSR(0)-MSR(3) is set to a one. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 3.

MSR(0) Delta Clear to Send (DCTS): DCTS displays that the –CTS input to the serial channel has changed state since it was last read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the –DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the –RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on –RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DDCD): DDCD indicates that the –DCD input to the serial channel has changed state since the last time it was read by the CPU.

TABLE 3. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR(0)	DCTS	Delta Clear To Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DDCD	Delta Data Carrier Detect
MSR(4)	–CTS	Clear To Send
MSR(5)	–DSR	Data Set Ready
MSR(6)	–RI	Ring Indicator
MSR(7)	–DCD	Data Carrier Detect

MSR(4) Clear to Send (CTS): CTS is the complement of the –CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in Loop Mode [(MCR(4)=1], MSR(4) reflects the value of RTS in the MCR.

MSR(5) Data Set Ready (DSR): DSR is the complement of the –DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the Loop Mode [MCR(4)=1], MSR(5) reflects the value of DTR in the MCR.

MSR(6) Ring Indicator (RI): RI is the complement of the –RI input (pin 39). If the channel is in the Loop Mode (MCR(4)=1), MSR(6) reflects the value of –OUT1 in the MCR.

MSR(7) Data Carrier Detect (DCD): Data Carrier Detect indicates the status of the Data Carrier Detect (–DCD) input. If the channel is in the Loop Mode (MCR(4)=1), MSR(2) reflects the value of –OUT2 in the MCR.

Reading the MSR register will clear the delta modem status indications but has no effect on the other status bits.

For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read –DISTR operation, the status bit is not set until the trailing edge of the read.

If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read instead of being set again.

DIVISOR LATCHES

The ACE serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 8 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 38.5K bps are available. Tables 5, 6 and 7 illustrate the divisors needed to obtain standard rates using these three frequencies.

SCRATCHPAD REGISTER

Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

INTERRUPT IDENTIFICATION REGISTER

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2) or character timeout
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 4 and are described below:

IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 4.

IIR(3): This bit is always logic 0 when in the VL16C450 Mode. This bit is set along with bit 2 when in the FIFO Mode and a timeout interrupt is pending.

IIR(4)-IIR(5): These two bits are always logic 0.

IIR(6)-IIR(7): FCR(0)=1 sets these two bits.

INTERRUPT ENABLE REGISTER

The Interrupt Enable Register (IER) is used to independently enable the four serial channel interrupt sources which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0)-IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 9 and below:

IER(0): When set to one, IER(0) enables the Received Data Available interrupt and the timeout interrupts in the FIFO Mode.

IER(1): When set to one, IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When set to one IER(2) enables the Receiver Line Status interrupt.

IER(3): When set to one, IER(3) enables the Modem Status Interrupt.

IER(4)-IER(7): These four bits of the IER are logic 0.

RECEIVER

Serial asynchronous data is input into the SIN pin. The ACE continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register when a full character is received, including parity and stop bits, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register which resets LSR(0). If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). If there is a parity error, the parity error is set in LSR(2). If a stop bit is not detected, a framing error indication is set in LSR(3).

If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

MASTER RESET

After power up, the ACE MR input should be held high for one microsecond to reset the ACE circuits to an idle mode until initialization. A high on MR causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following the removal of the reset condition (reset low), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the ACE is given in Table 8.

PROGRAMMING

The serial channel of the ACE is programmed by the control registers LCR, IER, DLL and DLM, MCR and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

FIFO INTERRUPT MODE OPERATION

The following RCVR interrupts will occur when the RCVR FIFO and receiver interrupts are enabled.

1. LSR(0) is set when a character is transferred from the shift register to th RCVR FIFO. When the FIFO is empty, it is reset.
2. IIR=06 (receiver line status interrupt) has higher priority than IIR=04 (received data available interrupt).

TABLE 4. INTERRUPT IDENTIFICATION REGISTER

FIFO Mode Only	Interrupt identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	—
0	1	1	0	First	Receiver Line Status	OE, PE, FE or BI	LSR Read
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	RBR Read or FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	Minimum of One Character in the RCVR FIFO and No Character Input or Removed During the Last Four Character Times	RBR Read
0	0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	0	Fourth	Modem Status	–CTS, –DSR, –RI or –DCD	MSR Read

3. Receive data available interrupt will be issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level it will be cleared.
4. IIR=04 (receive data available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following RCVR FIFO timeout interrupts will occur when RCVR FIFO and receiver interrupts are enabled.

1. If the following conditions exist, a FIFO timeout interrupt will occur.
   - Minimum of one character in FIFO
   - Last received serial character was longer than four continuous previous character times (if two stop bits are programed, the second one is included in the time delay)
   - The last CPU read of the FIFO was more than four continuous character times ago

   At 300 baud and 12-bit characters, the FIFO timeout interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal the character times can be calculated. (The delay is proportional to the baud rate.)
3. The timeout timer is reset after the CPU reads the RCVR FIFO or after a new character is received when there has been no timeout interrupt.
4. A timeout interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

XMIT interrupts will occur as follows when the transmitter and XMIT FIFO interrupts are enabled (FCR0=1, IER1=1).

1. The XMIT FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been a minimum of two bytes at the same time in XMIT FIFO, since the last THRE=1. If FCR0 is enabled, the first transmitter interrupt will occur immediately after changing FCR0.
2. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR=02) occurs. The interrupt is cleared as soon as the transmitter holding register is written toor the IIR is read.

RCVR FIFO trigger level and character timeout interrupts have the same priority as the current received data available interrupt. The current transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty.

FIFO POLLED MODE OPERATION

Resetting IER0, IER1, IER2, IER3 or all to zero, with FCR0=1, puts the ACE into the FIFO Polled Mode. RCVR and XMITTER are controlled separately. Therefore, either or both can be in the Polled Mode.

In the FIFO Polled Mode, there is no timeout condition indicated or trigger level reached. The RCVR and XMIT FIFOs still have the capability of holding characters, however.

6

TABLE 5. BAUD RATES (1.8432 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

TABLE 6. BAUD RATES (3.072 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

TABLE 7. BAUD RATES (8 MHz CLOCK)

Baud Rate Desired	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	1000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

TABLE 8. MASTER RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 Forced and 4-7 Permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Are Permanently Low
Line Control Register	Reset	All Bits Low
Modem Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–OUT2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–OUT1	Reset	High

TABLE 9. SERIAL CHANNEL ACCESSIBLE REGISTERS

Address	Register Mnemonic	Register Bit Number							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0*	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1*	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
2	FCR (Write Only)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	0	Reserved	DMA Mode Select	SMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
2	IIR (Read Only)	FIFOs Enabled**	FIFOs Enabled**	0	0	Interupt ID Bit (2)**	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" If Interrupt Pending
3	LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
4	MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
5	LSR	Error in RCVR Trigger**	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
6	MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

* DLAB = 1
**These bits are always 0 in the VL16C450 Mode.

6

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
tADS	Address Strobe Width	60		ns	
tAS	Address Setup Time	60		ns	
tAH	Address Hold Time	0		ns	
tCS	Chip Select Setup Time	60		ns	
tCH	Chip Select Hold Time	0		ns	
tDIW	–DISTR/DISTR Strobe Width	125		ns	
tRC	Read Cycle Delay	125		ns	
RC	Read Cycle = tAR(1) + tDIW + tRC	280		ns	Note 3
tDD	–DISTR/DISTR to Drive Disable Delay		060	ns	
tDDD	Delay from –DISTR/DISTR to Data		125	ns	100 pF Load (Note 2)
tHz	–DISTR/DISTR to Floating Data Delay	0	100	ns	100 pF Load (Note 2)
tDOW	–DOSTR/DOSTR Strobe Width		100	ns	
tWC	Write Cycle Delay	150		ns	
WC	Write Cycle = tAW + tDOW + tWC	280		ns	
tDS	Data Setup Time	30		ns	
tDH	Data Hold Time	30		ns	
tCSC	Chip Select Output Delay from Select			ns	
tRA	Address Hold Time from –DISTR/DISTR	20		ns	Note 1
tRCS	Chip Select Hold Time from –DISTR/DISTR	20		ns	Note 1
tAR	–DISTR/DISTR Delay from Address	30		ns	Note 1
tCSR	–DISTR/DISTR Delay from Chip Select	30		ns	Note 1
tWA	Address Hold Time from –DOSTR/DOSTR	20		ns	Note 1
tWCS	Chip Select Hold Time from –DOSTR/DOSTR	20		ns	Note 1
tAW	–DOSTR/DOSTR Delay from Address	30		ns	Note 1
tCSW	–DOSTR/DOSTR Delay from Select	30		ns	Note 1
tMRW	Master Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	55		ns	External Clock (8 MHz Max.)
tXL	Duration of Clock Low Pulse	55		ns	External Clock (8 MHz Max.)

Notes: 1. Only applies when –ADS is tied low.
2. VOL, VOH and the external loading determine the charge and discharge time.
3. In FIFO Mode RC=425 ns (min.) between reads of the receiver FIFO and the status registers (IIR or LSR).

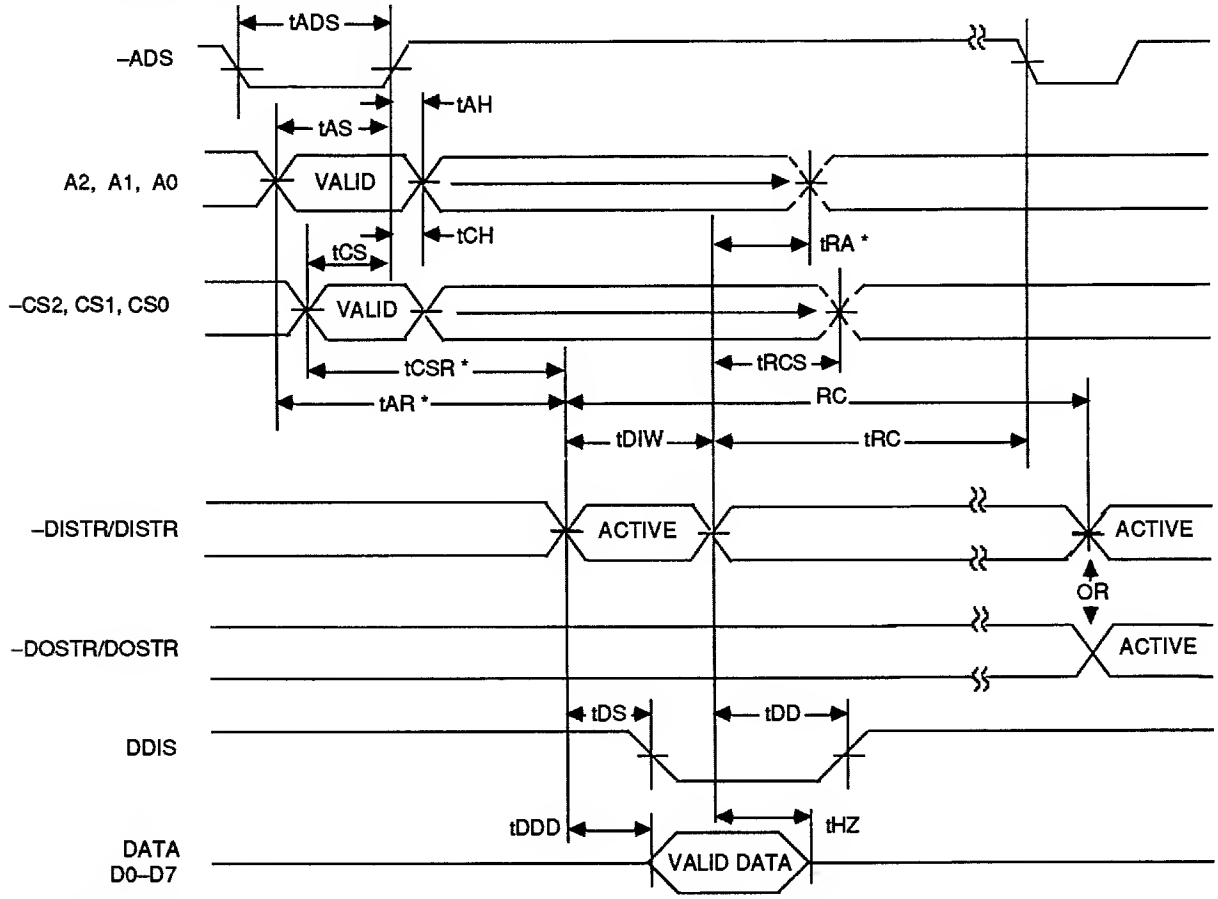
AC CHARACTERISTICS (Cont.): TA = 0°C to + 70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of –DOSTR/DOSTR (WR THR) to Reset Interrupt		175	ns	100 pF Load
tHR2	Delay from Falling Edge of –DOSTR/DOSTR (WR THR) to Reset Interrupt		250	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	–BAUDOUT CYCLES	
tSI	Delay from Initial Write to Interrupt	16	24	–BAUDOUT CYCLES	Note 1
tSS	Delay from Stop to Next Start		100	ns	
tSTI	Delay from Start Bit Low to Interrupt (THRE) High	8	8	–BAUDOUT CYCLES	Note 1
tIR	Delay from –DISTR/DISTR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
tSXA	Delay from Start to –TXRDY Active		8	–BAUDOUT CYCLES	100 pF Load
tWXI	Delay from Write to –TXRDY Inactive		195	ns	100 pF Load
Modem Control					
tMDO	Delay from –DOSTR/DOSTR (WR MCR) to Output		200	ns	100 pF Load
tSIM	Delay to Set Interrupt from Modem Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –DISTR/DISTR (RD MSR)		250	ns	100 pF Load
Baud Generator					
N	Baud Divisor	1	$2^{16}-1$		
tBLD	Baud Output Negative Edge Delay		175	ns	100 pF Load
tBHD	Baud Output Positive Edge Delay		175	ns	100 pF Load
tLW	Baud Output Down Time	100		ns	fX = 8 MHz, ÷2, 100 pF Load
tHW	Baud Output Up Time	75		ns	fX = 8 MHz, ÷2, 100 pF Load
Receiver					
tSCD	Delay from RCLK to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrupt		1	RCLK	Note 2
tRINT	Delay from –DISTR/DISTR (RD RBR/RD LSR) to Reset Interrupt		1	µs	100 pF Load

Notes: 1. If the Transmitter Interrupt Delay is active, this delay will be lengthened by one character time, minus the last stop bit time.

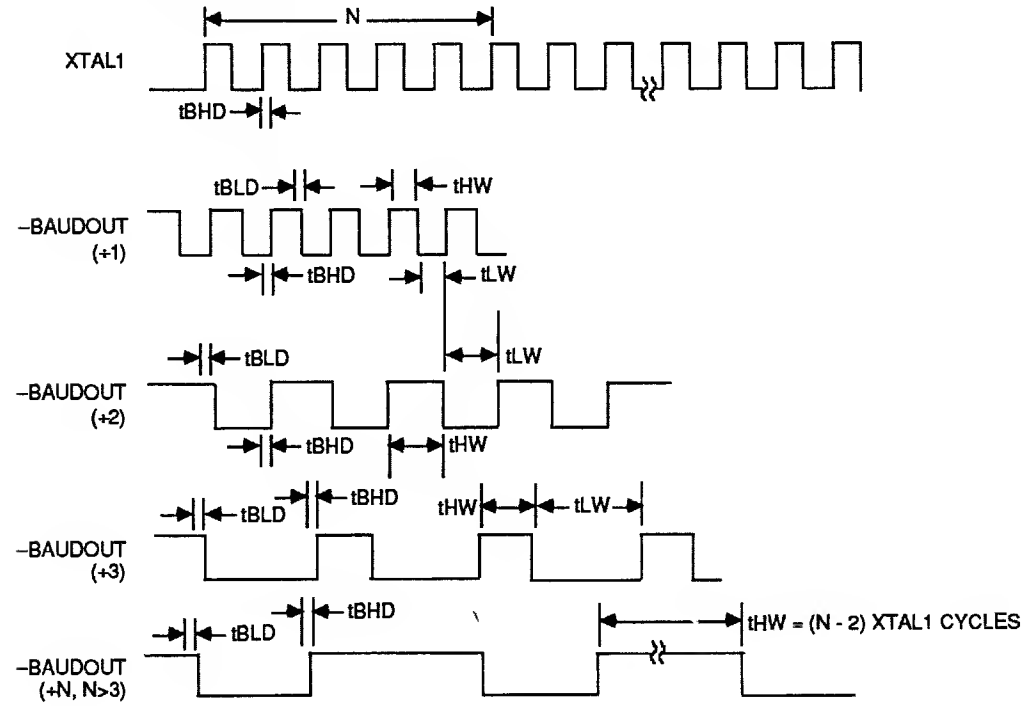
2. The receiver data available indication, the overrun error indication, the trigger level interrupts and the active –RXRDY indication will be delayed three RCLKs in the FIFO Mode (FCR0=1). After the first byte has been received status indicators (PE, FE, BI) will be delayed three RCLKs. These indicators will be updated immediately for any further bytes received after RDRBR goes inactive. There are eight RCLK delays for timeout interrupts.

READ CYCLE TIMING

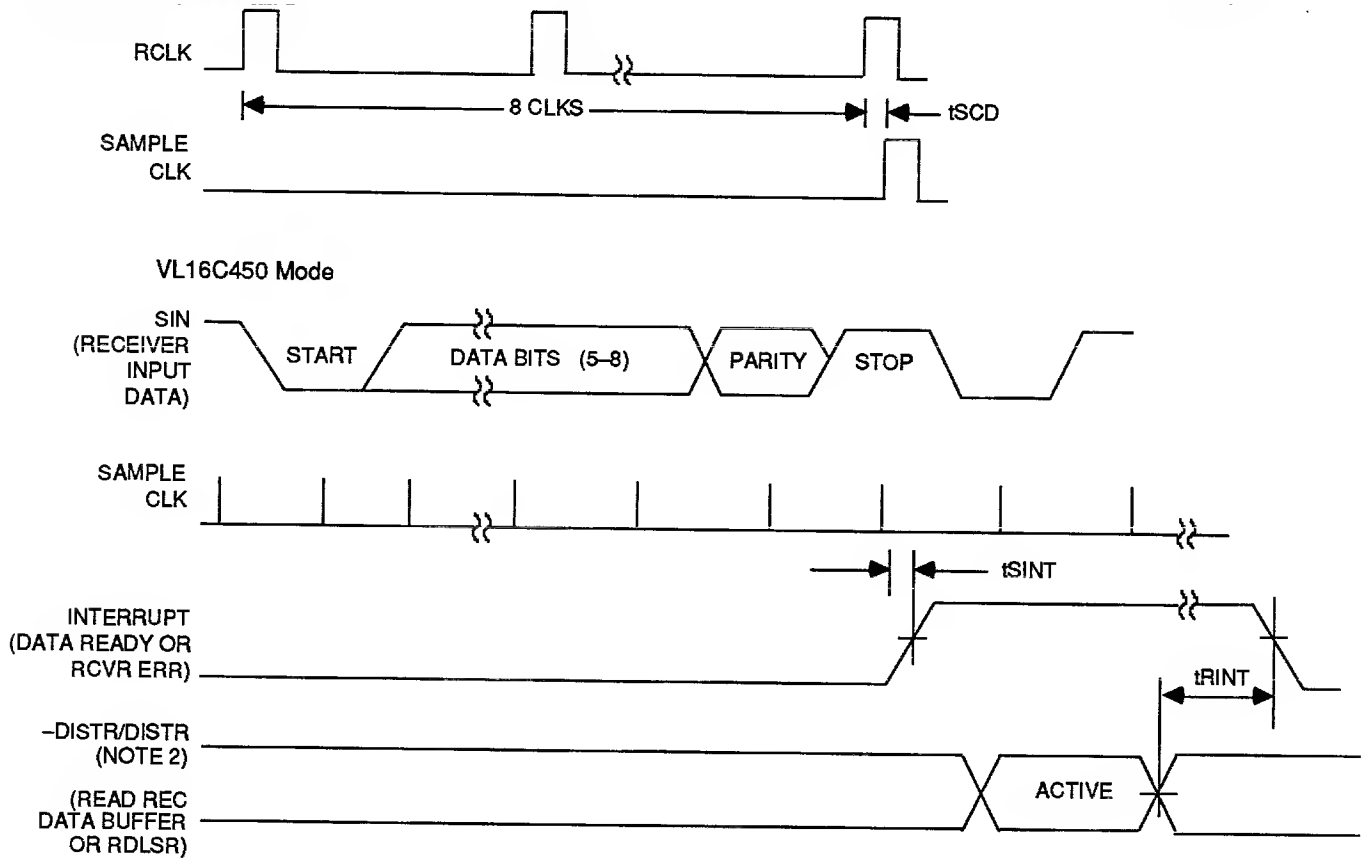


* Applicable only when -ADS is tied low.

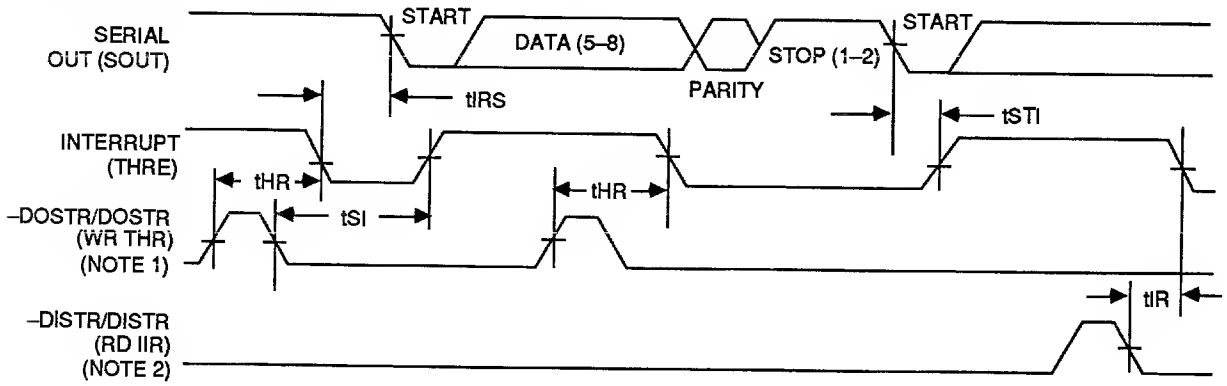
BAUDOUT TIMING



RECEIVER TIMING

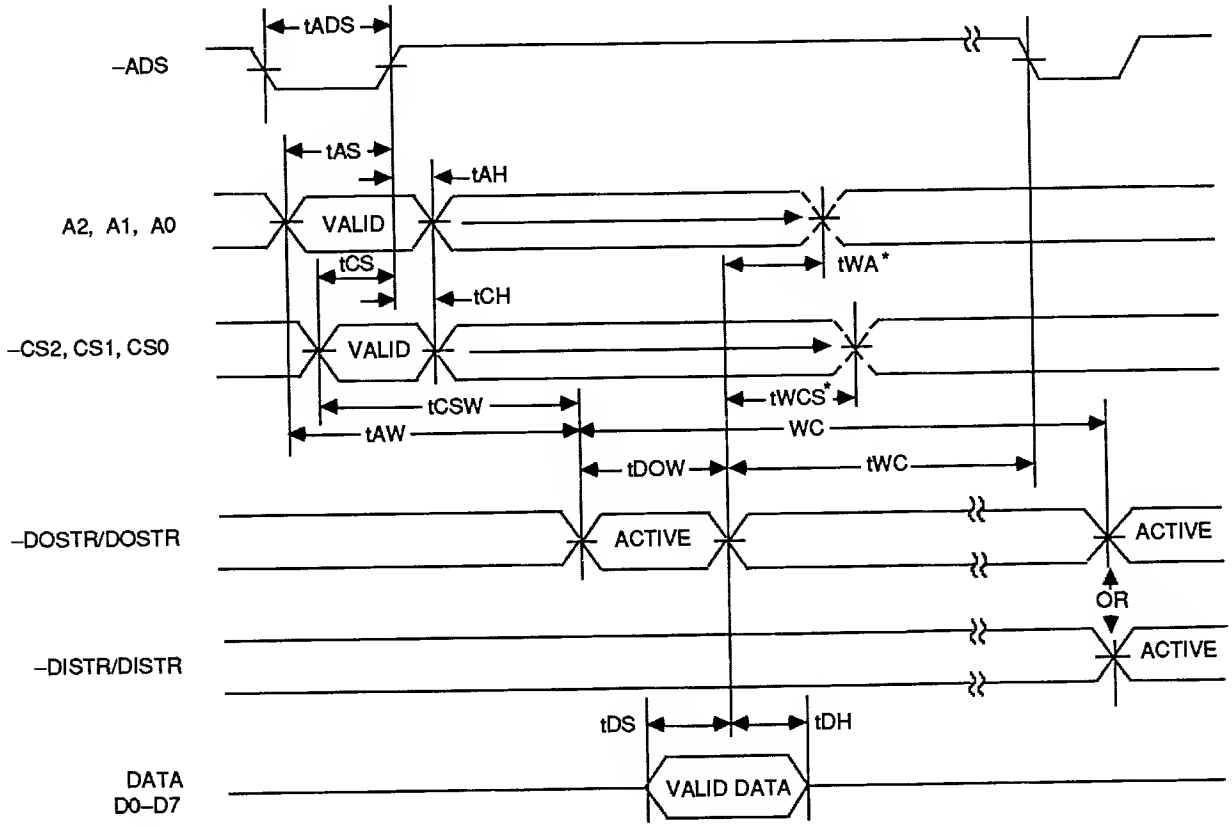


TRANSMITTER TIMING



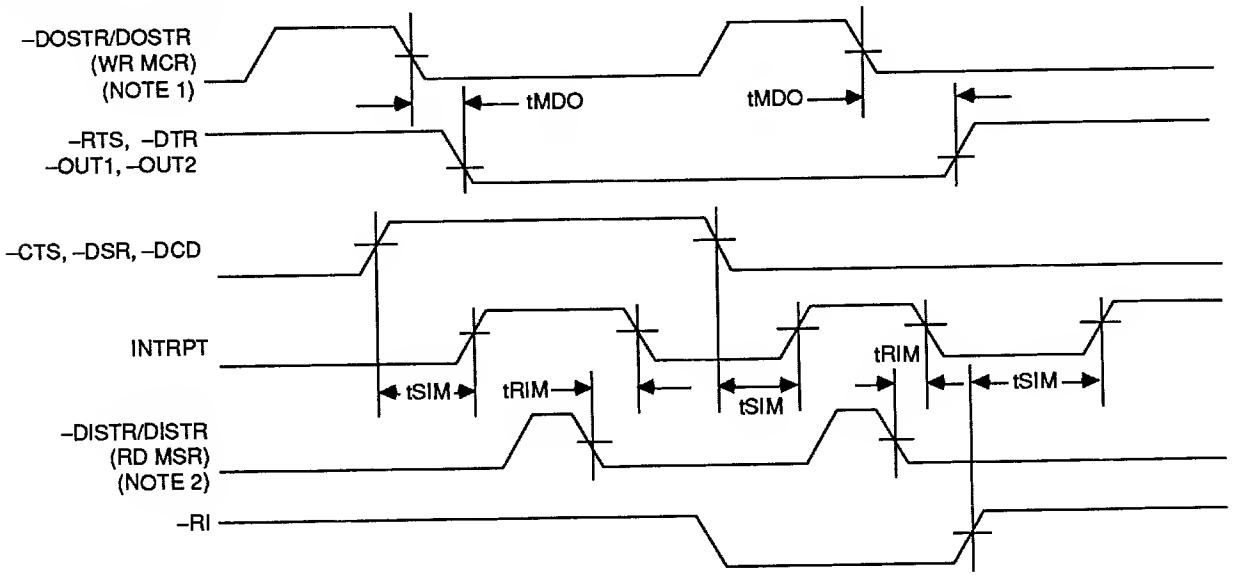
Notes: 1. See Write Timing.
2. See Read Timing.

WRITE TIMING



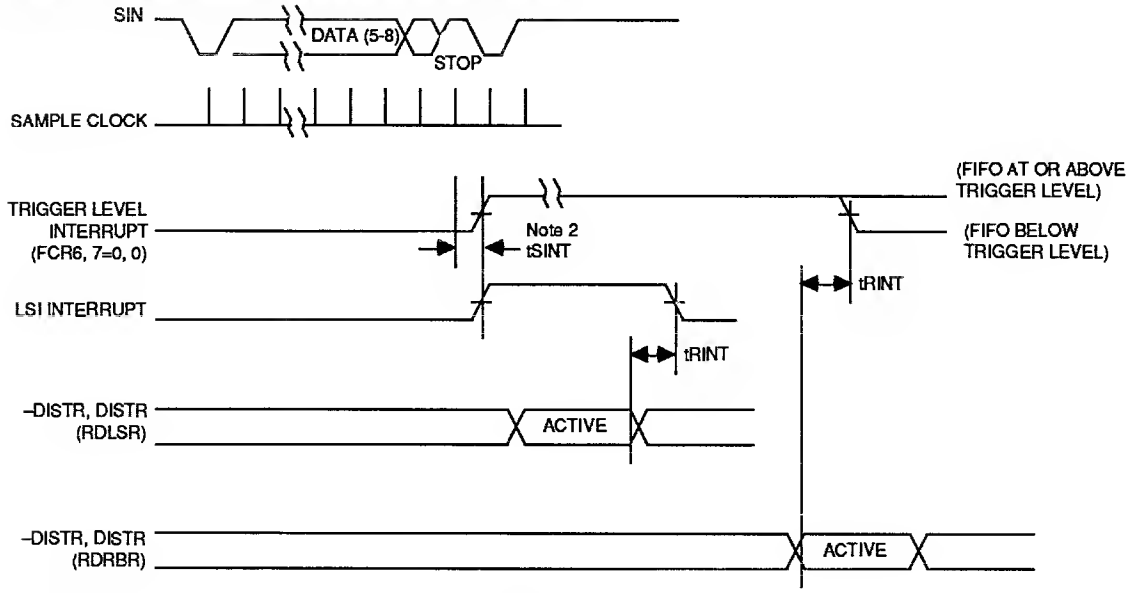
*Applicable only when –ADS is tied low.

MODEM TIMING

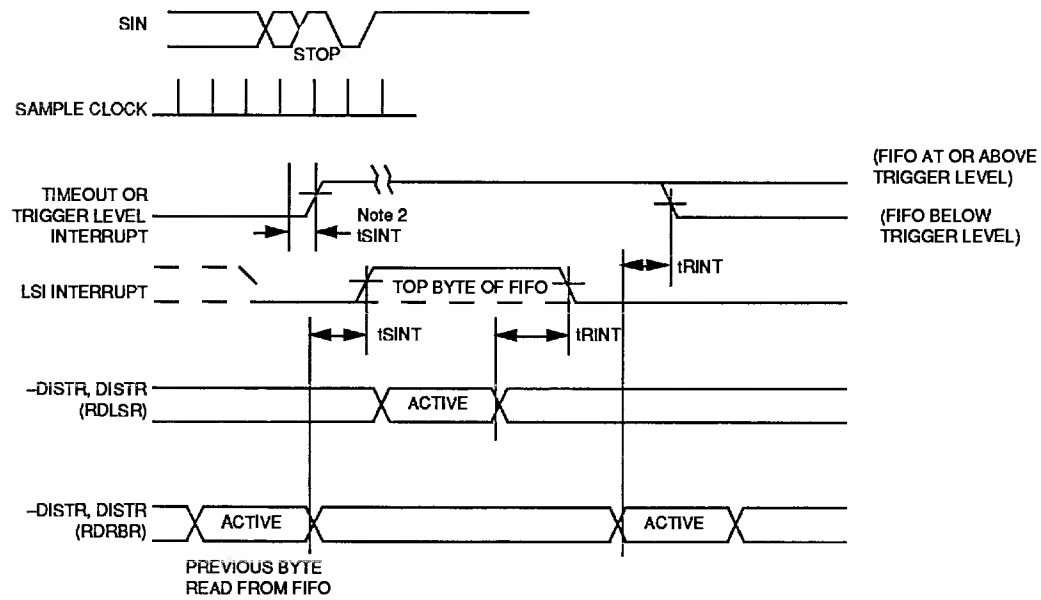


Notes: 1. See Write Timing.
2. See Read Timing.

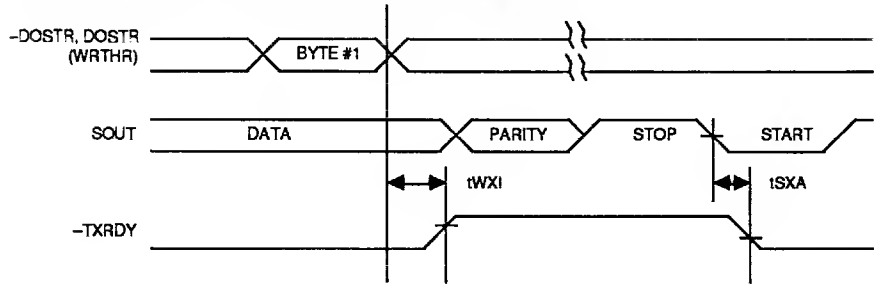
RCVR FIFO FIRST BYTE (This sets RDR.)



RCVR FIFO FIRST BYTE (RDR is already set.)



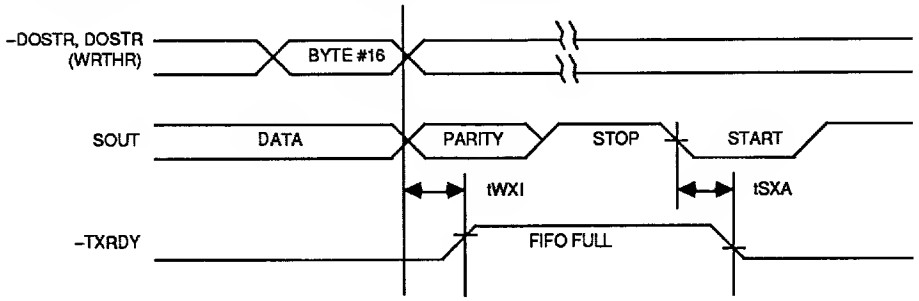
TRANSMITTER READY (PIN 24)-MODE 0



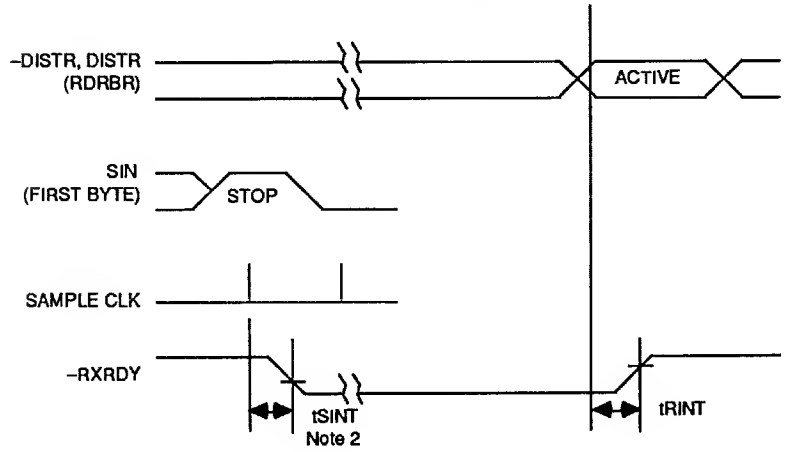
Notes: 1. This is the reading of the last byte in the FIFO.
2. If FCR0=1, then tSINT=3 RCLKs. For a timeout interrupt, tSINT=8 RCLKs.

6

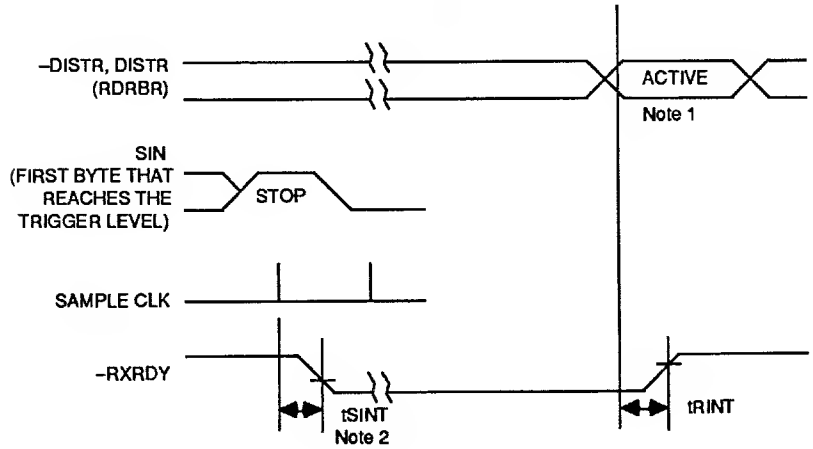
TRANSMITTER READY (PIN 24)-MODE 1



RECEIVER READY (PIN 29)-MODE 0



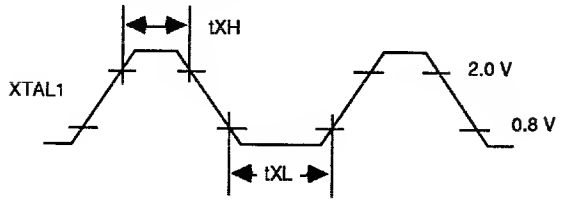
RECEIVER READY (PIN 29)-MODE 1



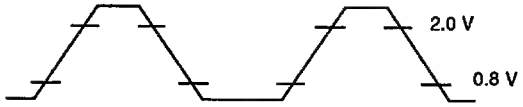
Notes: 1. This is the reading of the last byte in the FIFO.
2. If FCR0=1, then tSINT=3 RCLKs. For a timeout interrupt, tSINT=8 RCLKs.

AC TESTING INPUT/OUTPUT WAVEFORMS

EXTERNAL CLOCK INPUT (3.1 MHz MAXIMUM)



AC TEST POINTS



Note: All timings are referenced to valid 0 and valid 1.

TEST CIRCUIT

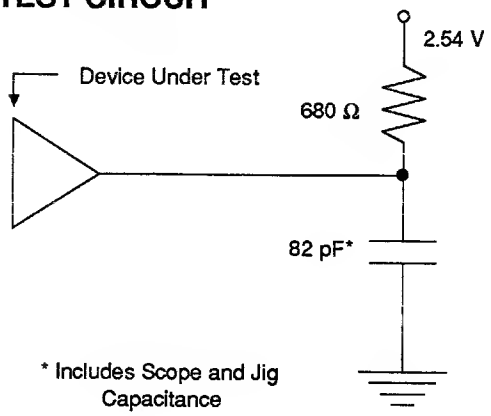
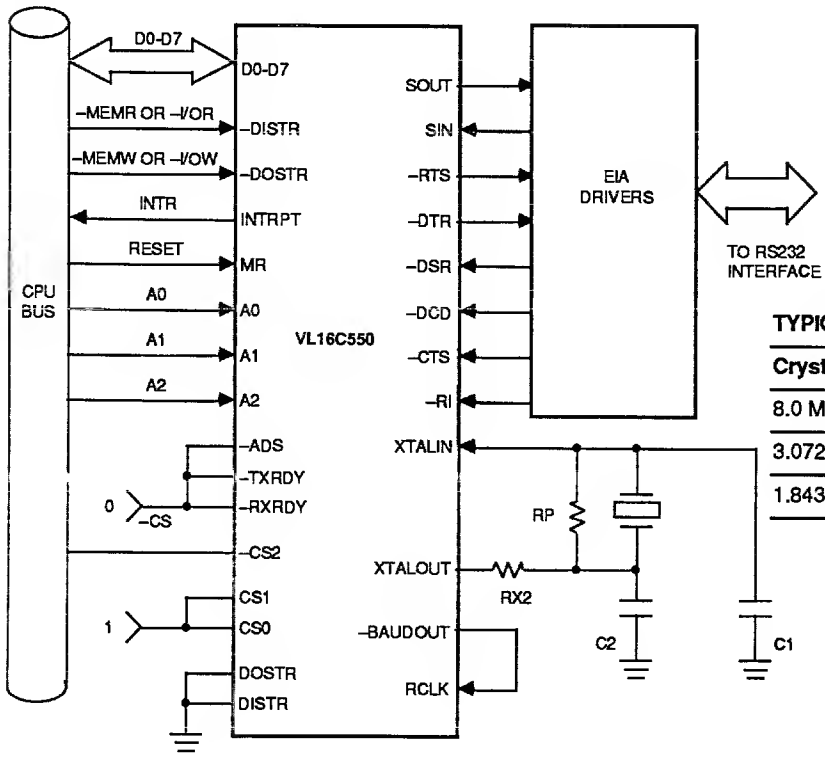


FIGURE 3. BASIC CONFIGURATION



TYPICAL COMPONENT VALUES

Crystal	RP	RX2	C1	C2
8.0 MHz	1 MΩ	1.5 KΩ	10 - 30 pF	40 - 90 pF
3.072 MHz	1 MΩ	1.5 KΩ	10 - 30 pF	40 - 90 pF
1.843 MHz	1 MΩ	1.5 KΩ	10 - 15 pF	65 - 100 pF

6

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to VCC +0.3 V
Applied Output Voltage	−0.5 V to VCC +0.3 V
Applied Input Voltage	−0.5 V to +7.0 V
Power Dissipation	500 mV

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	−0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	V	
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage		0.4	V	IOL 1.6 mA on All
VOH	Output High Voltage	2.4		V	IOH = −1.0 mA
ICC (Ave)	Average Power Supply Current (VCC)		10	mA	VCC = 5.25 V, No Loads on SIN, −DSR, −CTS, −DCD. −RI = 2.0 V. All Other Inputs = 0.8 V. Baud Rate Generator at 8 MHz. Baud Rate at 256K.
IIL	Input Leakage		±10	µA	VCC = 5.25 V VSS = 0 V All Other Pins Floating
ICL	Clock Leakage		±10	µA	VIN = 0 V, 5.25 V
IOZ	Three-State Leakage		± 20	µA	VCC = 5.25 V VSS = 0 V VOUT = 0 V, 5.25 V 1) Chip Deselected 2) Chip and Write Mode Selected.
VILMR	MR Schmitt VIL		0.8	V	
VIHMR	MR Schmitt VIH	2.0		V	

CAPACITANCE: TA = 25°C, VCC = VSS = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CXTAL2	Clock Input Capacitance		15	20	pF	fc = 1 MHz Unmeasured pins returned to VSS
CXTAL1	Clock Output Capacitance		20	30	pF	
CI	Input Capacitance		6	10	pF	
CO	Output Capacitance		10	20	pF	

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFO

FEATURES

- IBM PC/AT-compatible
- Two VL16C550 ACEs
- Centronix printer interface
- 16 byte FIFO reduces CPU interrupts
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
  - 5-, 6-, 7- or 8-bit characters
  - Even-, odd- or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus on each channel

DESCRIPTION

The VL16C552 is an enhanced dual-channel version of the popular VL16C550 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

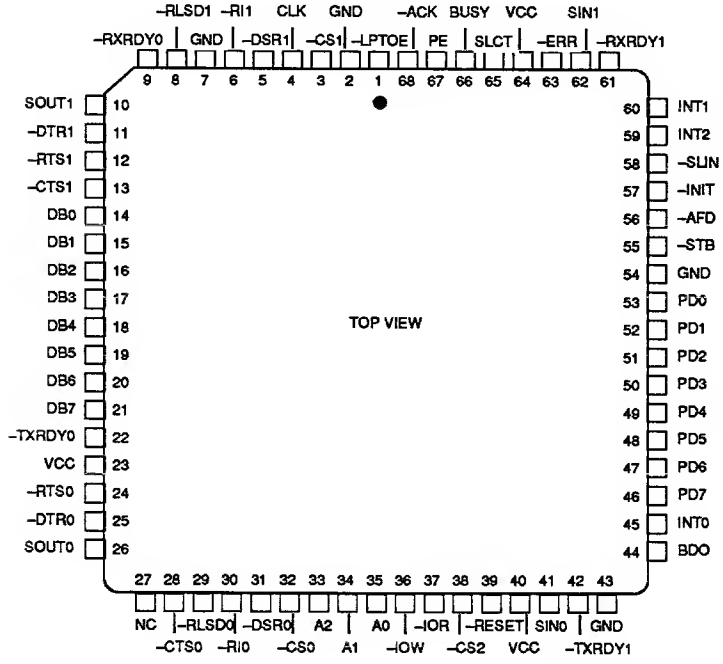
In addition to its dual communications interface capabilities, the VL16C552 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. The parallel port, together with the two serial ports, provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

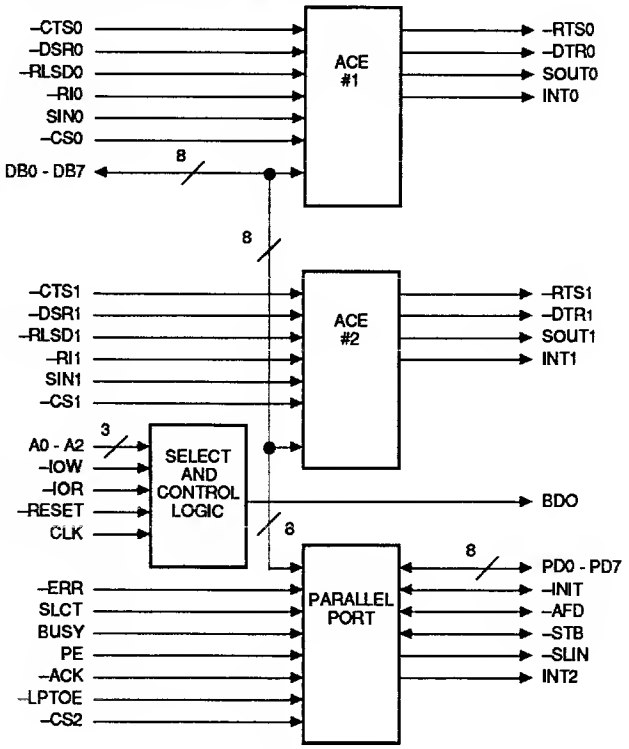
The VL16C552 is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM

VL16C552



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C552-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

NOTES:

VL82C018

REAL TIME CLOCK WITH RAM

FEATURES

- Direct replacement for IBM PC/AT-compatible clock
- Calculates year (with leap year compensation), month, date, day of the week, days, hours, minutes, and seconds
- Calendar, time and alarm are represented as binary or BCD
- 24- or 12-hour clock (AM and PM in 12-hour mode)
- Programmable daylight savings time feature
- Compatible with Motorola and Intel bus timing
- Multiplex bus for lower pin count
- Appears as 64 RAM locations to microprocessor
  - 14 bytes of RAM for control and clock registers
  - 50 bytes of general purpose RAM
- CMOS technology for low power dissipation
- On chip oscillator
- Power sense input sets register bit in case of power failure
- Square wave output signal is programmable
- (–IRQ) bus compatible interrupt signals
- Three software-maskable and testable interrupts
  - Once/second to once/day time-of-day alarm
  - End of clock update cycle
- In-circuit test mode

DESCRIPTION

The VL82C018 is a CMOS Real Time Clock with RAM that directly replaces the MC146818 and DS1287A in the IBM AT computer clock/calendar application and elsewhere. Components required to maintain time-of-day and memory status in the absence of power are an external crystal and battery.

Connections are for a standard 32.768 KHz quartz crystal or equivalent. For extremely high precision timekeeping applications, a variable timing capacitor may be required. The internal oscillator circuitry is operated with a crystal having a specified load capacitance of 6 pF.

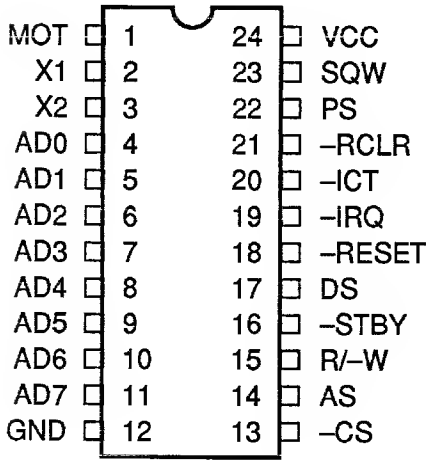
The battery that is required is any standard three volt lithium cell or other energy source. For proper operation, the voltage must be held between two and four volts.

The –RCLR function is designed so that it can be shorted to ground manually or by switch and is not driven with external buffers. By setting the –RCLR pin to logic 1, the 50 bytes of general purpose RAM can be cleared without effecting the RAM associated with the Real Time Clock. –RCLR must be forced to an input logic 0 during battery back up mode when VCC is not applied in order to clear the RAM.

6

PIN DIAGRAM

VL82C018



ORDER INFORMATION

Part Number	Package
VL82C018-PC	Plastic DIP

Note: Operating temperature range is 0°C to +70°C.

NOTES:

VL82C106

PC/AT COMBO I/O CHIP

FEATURES

- Combines the following PC/AT® Peripheral Chips:
  - VL16C450 UART - COM1:
  - VL16C450 UART - COM2:
  - Parallel Printer Port - LPT1:
  - Keyboard/Mouse Ctrl. - KBD
  - Real Time Clock
- Serial ports fully 16C450 compatible
- Bidirectional line printer port
- Software control of PS/2®-compatible enhancements (LPT Port, Mouse)
- CMOS direct drive of Centronics-type parallel interface
- PC/AT- or PS/2-compatible keyboard and mouse controller
- 146818A-compatible Real Time Clock (RTC)
- 16 bytes of additional standby RAM (66 bytes total)
- IDE bus control signals included (two external 74LS245 and one 74ALS244 - or equivalent - buffers are required)
- Seven battery-backed programmable chip select registers for auto configuration
- Preprogrammed default chip selects
- Programmable wait state generation
- 5 µA standby current for RTC, RAM, and chip select registers
- Single 128-pin plastic quad flatpack

DESCRIPTION

The VL82C106 Combo chip replaces with a single 128-pin chip, several of the commonly used peripherals found in PC/AT-compatible computers. This chip when used with the VLSI PC/AT-compatible chip set allows designers to implement a very cost effective, minimum chip count motherboard containing functions that are common to virtually all PCs.

The on-chip UARTs are completely software compatible with the VL16C450 ACE.

The bidirectional parallel port provides a PS/2 software compatible interface between a Centronics-type printer and the VL82C106. Direct drive is provided so that all that is necessary to interface to the line printer port is a resistor - capacitor network. The bidirectional feature (option) is software programmable for backwards PC/AT-compatibility.

The keyboard/mouse controller is selectable as PC/AT- or PS/2-compatible.

The Real Time Clock is 146818A-compatible and offers a standby current drain of 5 µA at 3.0 V.

Included is the control logic necessary for the support of the Integrated Drive Electronics (IDE) hard disk bus interface.

The Combo I/O chip also includes seven programmable chip selects, three internal and four external. Each chip select has a programmable 16-bit base address and a mask register that allows the number of bytes corresponding to each chip select to be programmed (e.g. 3F8H-3FFH has a base address of 3F8H and a range of 8 bytes). Each chip select can be programmed for number of wait states (1-8) and 8- or 16-bit operation. 16-bit decoding is used for all I/O addresses. A default fixed decode is provided on reset for the on-chip serial ports, printer port, and off-chip floppy and hard disk controllers, which may be changed to battery-backed programmable chip selects via a control bit.

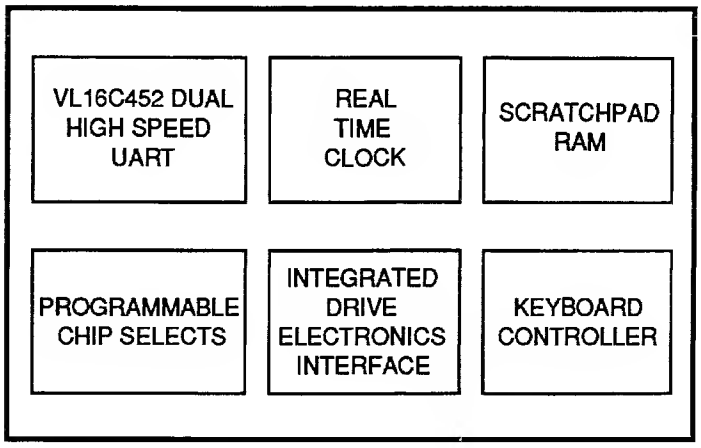
6

ORDER INFORMATION

Part Number	Package
VL82C106-QFPC	Plastic Quad Flatpack

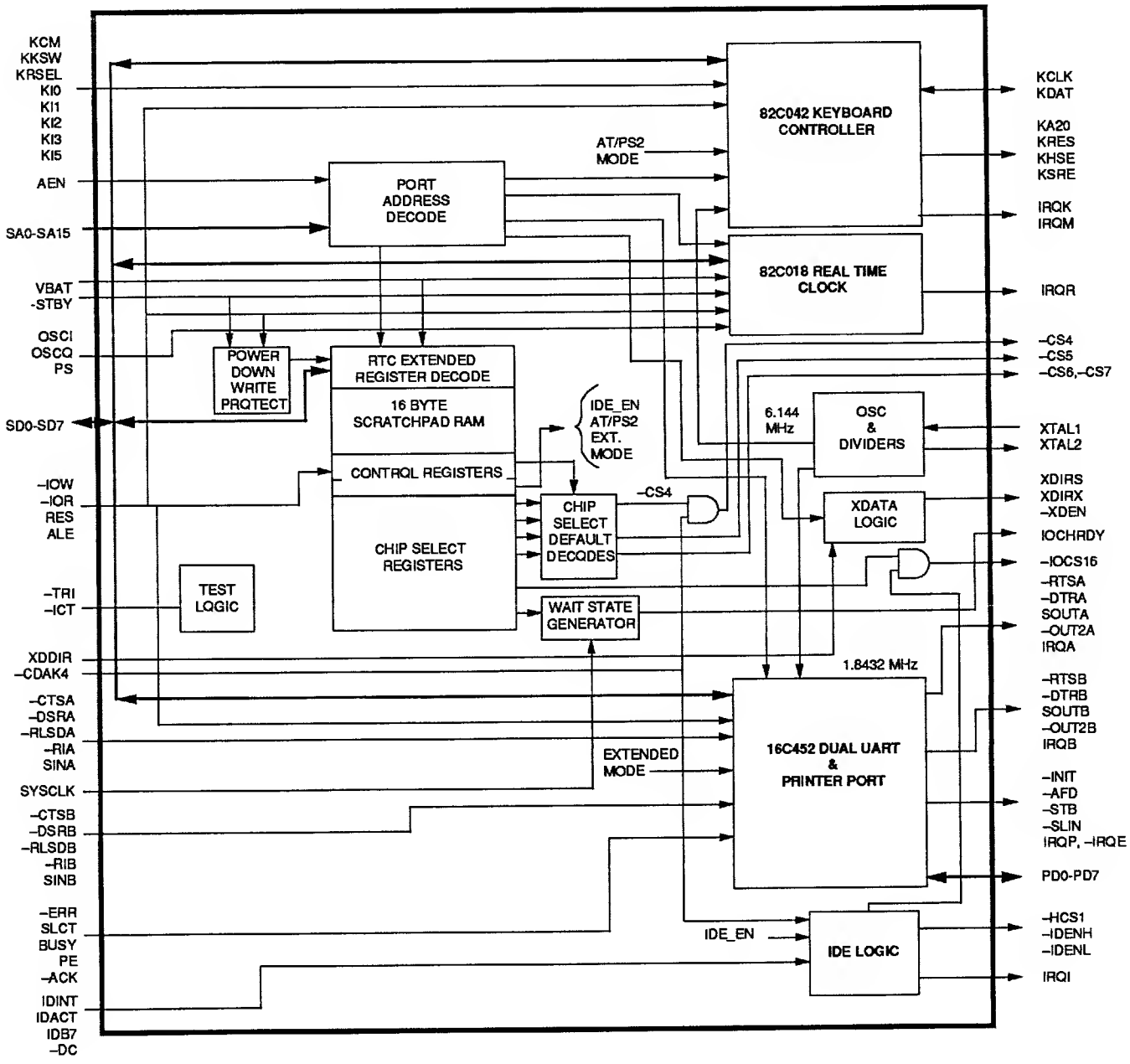
Note: Operating temperature range is 0°C to +70°C.

INTERNAL FUNCTIONAL DIAGRAM



PC/AT® and PS/2® is the registered trademark of IBM Corporation.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Below is a detailed explanation of each of the major building blocks of the VL82C106 Combo chip. The following functional blocks are covered:

- 16C450 Serial Ports
- Parallel Printer Port
- 146818A-Compatible Real Time Clock
- Keyboard Controller
- Control and Chip Selects
- IDE Interface

SERIAL COMMUNICATIONS PORTS

The chip contains two UARTs, based on the VL16C450 Megacell core. Each of these UARTs share a common baud-rate clock, which is the XTAL1 input (18.432 MHz) divided by ten . The 18.432 MHz signal is shared with the keyboard controller, which divides it by three to get an approximate 6 MHz reference clock. Please refer to the VL16C450 data sheet for the register descriptions for the UARTs.

COMA is accessed via internally generated CS1, while COMB uses internally generated CS2.

LINE PRINTER PORT

The Line Printer Port contains the functionality of the port included in the VL16C452, but offers a software programmable Extended Mode. This enhancement is the addition of a Direction Control Bit, an Interrupt Status Bit, and modification of the –LPTOE signal to an Extended Mode control signal. These features are disabled on initial power-up, but may be turned on by setting the EMODE bit of Control Register 0 (RTC Register 50H in AT or PS/2 mode or I/O PORT 102H in PS/2 mode). When the EMODE bit is not enabled, the part functions exactly as a PC/AT-compatible printer port.

The Line Printer Port is accessed via internally generated programmable chip select CS3.

Register 0 - Line Printer Port Data

The Line Printer (LPT) Port is either uni- or bidirectional, depending on the state of the Extended Mode and Data Direction Control bits.

Compatibility Mode (EMODE bit = 0) - Read operations differ according to the state of the EMODE Control bit. When in compatibility mode (EMODE = 0), reads to this register return the last data that was written to the LPT Port. Write operations immediately output data to the LPT Port.

(EMODE bit = 1) - Read operations return either the data last written to the LPT Data Register if the Direction Bit is set to write ("0") or the data that is present on the pins of the LPT Port if the direction is set to read ("1"). Write operations latch data into the output register, but only drive the LPT Port when the Direction Bit is set to write.

In either case, the bits of the LPT Data Register are defined as follows:

Bit	Description
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

Register 1 - LPT Port Status

The LPT Status Register is a read-only register that contains interrupt status and real time status of the LPT connector pins. The bits are described as follows:

Bit	Description
0	Reserved
1	Reserved
2	–IRQ
3	–ERROR
4	SLCT
5	PE
6	–ACK
7	–BUSY

Bits 0 and 1 - Reserved, read as "1's".

Bit 2 - Interrupt Status bit, a "0" indicates that the printer has acknowledged the previous transfer with a ACK handshake (bit 4 of the control register must be set to "1"). The bit is changed to "0" on the active to inactive transition of the –ACK signal. This bit is changed to a "1" after a read from the status port. The default value for this bit is "1".

Bit 3 - Error Status bit, a "0" indicates that the printer has had an error. A "1" indicates normal operation. This bit follows the state of the –ERR pin.

Bit 4 - Select Status bit, indicates the current status of the SLCT signal from the printer. A "0" indicates the printer is currently not selected (off-line). A "1" means the printer is currently selected.

Bit 5 - Paper Empty Status bit, a "0" indicates normal operation. A "1" indicates that the printer is currently out of paper. This bit follows the state of the PE pin.

Bit 6 - Acknowledge Status bit, a "0" indicates that the printer has received a character and is ready to accept another. A "1" indicates that the last operation to the printer has not been completed yet. This bit follows the state of the –ACK pin.

Bit 7 - Busy Status bit, a "0 indicates that the printer is busy and cannot receive data. A "1" indicates that the printer is ready to accept data. This bit is the inversion of the BUSY pin.

Register 2 - LPT Port Control

This port is a read/write port that is used to control the LPT direction as well as the Printer Control lines driven from the port. Write operations set or reset these bits, while read operations return the status of the last write operation to this register (except for bit 5 which is write only and is always read back as a "1"). The bits in this register are defined as follows:

Bit	Description
0	STROBE
1	AUTO FD XT
2	–INIT
3	SLCT IN
4	IRQ EN
5	DIR (Write Only)
6	Reserved
7	Reserved

Bit 0 - Printer Strobe Control bit, when set ("1") the STROBE signal is asserted on the LPT interface, causing the printer to latch the current data. When reset ("0") the signal is negated.

Bit 1 - Auto Feed Control bit, when set ("1") the AUTO FD XT signal will be asserted on the LPT interface, causing the printer to automatically generate a line feed at the end of each line. When reset ("0") the signal is negated.

Bit 2 - Initialize Printer Control bit, when set ("1") the INIT signal is negated. When reset ("0") the INIT signal is asserted to the printer, forcing a reset.

Bit 3 - Select Input Control bit, when set ("1") the SLCT IN signal is asserted, causing the printer to go "on-line". When reset ("0") the signal is negated.

Bit 4 - Interrupt Request Enable Control bit, when set ("1") enables interrupts from the LPT Port whenever the –ACK signal is asserted by the printer. When reset ("0") interrupts are disabled.

Bit 5 - When EMODE = 1, Direction (DIR) Control bit, when set ("1") the output buffers in the LPT Port are disabled, allowing data driven from external sources to be read from the LPT Port. When reset ("0"), the output buffers are enabled, forcing the LPT pins to drive the LPT pins. The power-on-reset value of this is set ("1"). When EMODE = 0, this bit has no effect.

Bits 6 and 7 - Reserved, read as "1's".

REAL TIME CLOCK

The Real Time Clock (RTC) is a direct replacement for the Motorola MC146818A Real Time Clock component. It is also compatible with the Dallas Semiconductor DS1287A RTC when an external battery and crystal are provided. Clock functions include the following:

- Time of Day Clock
- Alarm Function
- 100 Year Calendar Function
- Programmable Periodic Interrupt Output
- Programmable Square Wave Output
- 50 Bytes of User RAM
- User RAM Preset Feature

RTC PROGRAMMERS MODEL

The RTC memory consists of ten RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 50 general purpose RAM bytes. The address map of the real time clock is shown below.

Add.	Function	Range
0	Seconds (Time)	0-59
1	Seconds (Alarm)	0-59
2	Minutes (Time)	0-59
3	Minutes (Alarm)	0-59
4	Hours (Time)	1-12, 12 Hr Mode
4	Hours (Time)	0-23, 24 Hr Mode
5	Hours (Alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R O)
13	RTC Register D	(R O)
14-63	User RAM (Standby)	

All 64 bytes are directly readable and writable by the processor program except for the following:

1) Registers C and D are read only.
2) Bit 7 of Register A is read only.
3) Bit 7 of the seconds byte is read only.

The RTC is accessed via internally decoded PORT 070H (RTC register address) and PORT 071H (RTC data read/write).

The RTC address map also includes additional standby RAM, plus control registers for Combo chip configuration and chip select control. The RAM and Chip Select control registers are powered via the VBAT power supply for battery-backed operation.

The bottom 64 bytes of the address space are devoted to the RTC function, the next 16 bytes are used for the additional standby RAM, the next 25 bytes for future RAM expansion, and the next 23 bytes are used for programmable chip select base registers and peripheral configurations. The total address map is shown below:

Add.	Function
0-13	Time Portion of RTC
14-63	RAM Portion of RTC
64-79	Additional Standby RAM
80-104	Reserved
105-127	Chip Select Control Registers
128-255	Reserved for NMI Enable Control

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Time of Day Register

The contents of the Time of Day registers can be either in Binary or BCD format. They are relatively straightforward, but are detailed here for completeness. The address map of these registers is shown next:

Add.	Function	Range
0	Seconds (Time)	0-59
1	Seconds (Alarm)	0-59
2	Minutes (Time)	0-59
3	Minutes (Alarm)	0-59
4	Hours (Time)	1-12, 12 Hr Mode
4	Hours (Time)	0-23, 24 Hr Mode
5	Hours (Alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99

Address 0 - Seconds (Time): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 1 - Seconds (Alarm): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 2 - Minutes (Time): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 3 - Minutes (Alarm): The range of this register is 0-59 in BCD mode, and 0-3BH in Binary mode.

Address 4 - Hours (Time): The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01H-0CH	Binary	AM
81H-8CH	Binary	PM

Address 5 - Hours (Alarm): The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01H-0CH	Binary	AM
81H-8CH	Binary	PM

Address 6 - Day of Week: The range of this register is 1-7 in BCD mode, and 1-7H in Binary mode.

Address 7 - Date: The range of this register is 1-31 in BCD mode, and 1-1FH in Binary mode.

Address 8 - Month: The range of this register is 1-12 in BCD mode, and 1-0CH in Binary mode.

Address 9 - Year: The range of this register is 0-99 in BCD mode, and 0-63H in Binary mode.

RTC CONTROL REGISTER

The RTC has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Add.	Function	Type
10	RTC Register A	R/W
11	RTC Register B	R/W
12	RTC Register C	R O
13	RTC Register D	R O
14-63	User RAM (Standby)	R/W

Register A

This register contains control bits for the selection of Periodic Interrupt, Input Divisor, and the Update In Progress Status bit. The bits in the register are defined as follows:

Bit	Description	Abbr.
0	Rate Select Bit 0	RS0
1	Rate Select Bit 1	RS1
2	Rate Select Bit 2	RS2
3	Rate Select Bit 3	RS3
4	Divisor Bit 0	DV0
5	Divisor Bit 1	DV1
6	Divisor Bit 2	DV2
7	Update In Progress	UIP

Bits 0 to 3 - The four rate selection bits (RS0 to RS3) select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by RESET. The Periodic Interrupt Rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate	
0	None	
1	3.90625	ms
2	7.8125	ms
3	122.070	µs
4	244.141	µs
5	488.281	µs
6	976.562	µs
7	1.953125	ms
8	3.90625	ms
9	7.8125	ms
0AH	15.625	ms
0BH	31.25	ms
0CH	62.5	ms
0DH	125	ms
0EH	250	ms
0FH	500	ms

Bits 4 to 6 - The three Divisor Selection bits (DV0 to DV2) are fixed to provide for only a five-state divider chain, which would be used with a 32 kHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, Divider Running
6	Reset Mode, Divider in Reset State

Bit 7 - The Update In Progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP

6

bit is "0". The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in Register B to a "1" will inhibit any update cycle and then clear the UIP status bit.

Register B

Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr.
0	Daylight Savings Enable	DSE
1	24/12 Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Not Used	
4	Update End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 - The Daylight Savings Enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

The elimination of this feature will be considered, since the start date of daylight savings time is currently being changed.

Bit 1 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode ("1") or the 12-hour mode ("0"). This is a read/write bit, which is affected only by software.

Bit 2 - The Data Mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

Bit 3 - This bit is unused in this version of the RTC, but is used for Square Wave Enable in the Motorola MC146818.

Bit 4 - The UIE (Update End Interrupt Enable) bit is a read/write bit which enables the Update End Interrupt Flag (UF) bit in Register C to assert an IRQ. The reset pin being asserted or the SET bit going high clears the UIE bit.

Bit 5 - The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a "1" permits the Alarm Interrupt Flag (AF) bit in Register C to assert an IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of 11XXXXXXb). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal. The reset pin clears AIE to "0". The internal functions do not affect the AIE bit.

Bit 6 - The Periodic Interrupt Enable (PIE) bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the IRQ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A "0" in PIE blocks IRQ from being initiated by a periodic interrupt, but the Periodic Interrupt Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal functions, but is cleared to "0" by a reset.

Bit 7 - When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

Register C

Register C contains status information about interrupts and internal operation of the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr.
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Update End Interrupt Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	IRQ Pending Flag	IRQF

Bits 0 to 3 - The unused bits of Status Register 1 are read as "0's", and cannot be written.

Bit 4 - The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting IRQ. UF is cleared by a Register C read or a reset.

Bit 5 - A "1" in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the IRQ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A reset or a read of Register C clears AF.

Bit 6 - The Periodic Interrupt Flag (PF) is a read only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an IRQ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a reset or a software read of Register C.

Bit 7 - The Interrupt Request Pending Flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a "1", the IRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the reset pin is asserted.

Register D
This register contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr.
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Vaild RAM Data and Time	VRT

Bits 0 to 6 - The remaining bits of Register D are unused. They cannot be written, but are always read as "0's".

Bit 7 - The Valid RAM Data and Time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the reset pin. The VRT bit can only be set by reading Register D.

CMOS STANDBY RAM
The 66 general purpose RAM bytes are not dedicated within the RTC. They can be used by the processor program, and are fully available during the update cycle.

GENERAL RTC NOTES
Set Operation
Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the Data Mode (DM) bit of Register B. All ten time, calendar, and alarm bytes must use the same Data Mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the RTC makes all updates in the selected Data Mode. The Data Mode cannot be changed without reinitializing the ten data bytes.

BCD vs Binary Format
The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

Update Operation
The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the Update Cycle in the processor program.

Alarm Operation
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the Alarm Interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any byte from 0C0H to 0FFH. An Alarm Interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts
The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The Alarm Interrupt may be programmed to occur at rates from one-per-second to one-a-day. The Periodic Interrupt may be selected for rates from half-a-second to 30.517 µs. The Update Ended Interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control
The Divider Control bits are fixed for only 32.768 kHz operation. The divider chain may be held in reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half a second later. The Divider Control bits are also used to facilitate testing the RTC.

Periodic Interrupt Selection
The Periodic Interrupt allows the IRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The Periodic Interrupt is separate from the Alarm Interrupt which may be output from once-per-second to once-per-day.

KEYBOARD CONTROLLER

The keyboard controller on-chip ROM contains the code that is required to support the PC/AT and PS/2 command sets and 136 bytes of conversion code.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simplify error handling in software. This logic is duplicated for the mouse interface.

User RAM support is provided. The program writes the 5-bit address (32-byte range) to a register, and then reads or writes the data through accesses to another register, PORT 60H DBB.

Parallel Ports 1 and 2 are provided, but are restricted to inputs only for P1 and outputs only to P2.

Support for PORT 60H DBB (reads and writes) and Status Register (reads and writes) is provided in hardware for interface to the PC host.

KEYBOARD CONTROLLER INTERFACE TO PC/AT

The interface to the PC/AT consists of one register pair (PORT 60H/64H) for the keyboard and mouse. Accesses to the registers are determined by the state of A2 and the chip select. For host control signals involved, the Command, Status and Data Registers are accessed as follows:

IOR	IOW	A2	Register
0	1	0	Read - Data DBB Output Buffer
0	1	1	Read - Status
1	0	0	Write - Data DBB Input Buffer
1	0	1	Write - Command

The PORT 60H DBB read operations output the contents of the Output Buffer to D0-D7 (host data bus - bidirectional or can be a three-state), and clears the status of the Output Buffer Full (OBF/ Status Register bit 0) bit.

Status read operations output the contents of the Status Register to D0-D7. No status is changed as a result of the read operation.

The PORT 60H DBB write operations cause the Input Buffer DBB to be changed. The state of the C/D bit is cleared (Status Register bit 3, "0" indicates data) and the Input Buffer Full (IBF/Status Register bit 1) bit is set ("1").

Command write operations are the same as DBB writes, except that the address is PORT 64H. The C/D bit will be set to ("1") when a valid command has been written to PORT 64H.

KEYBOARD PORT INTERFACE PROTOCOL

Data transmission between the controller, the keyboard, and mouse consist of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start Bit (Always 0)
2	Data Bit 0 (LSB)
3-8	Data Bits 1-6
9	Data Bit 7 (MSB)
10	Parity Bit (Odd)
11	Stop Bit (Always 1)

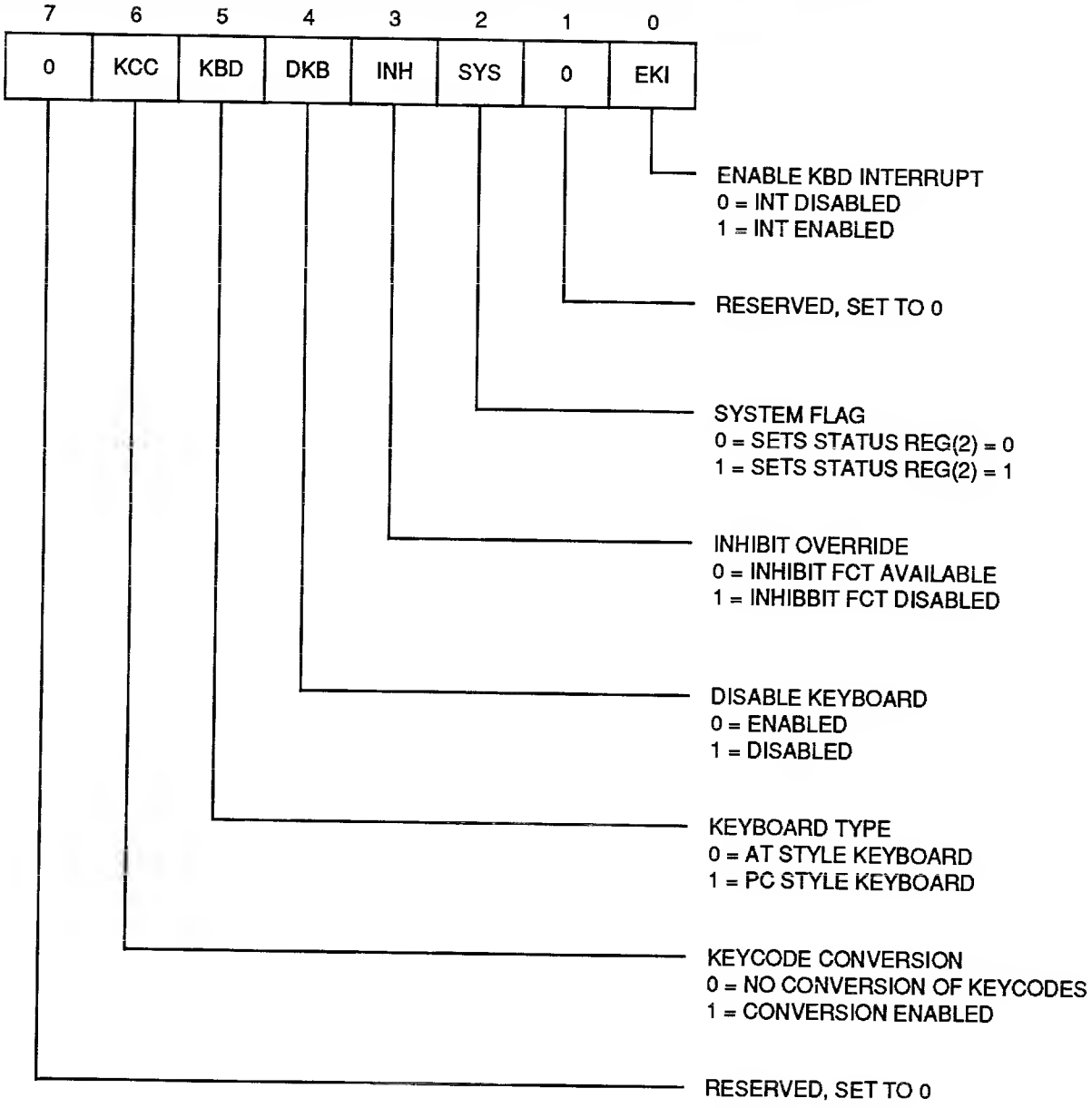
PROGRAMMER INTERFACE

The programmer interface to the keyboard controller is quite simple, consisting of four registers:

Register	R/W	I/O
Status	R	64H
Command	W	64H
Output Buffer	R	60H
Input Buffer	W	60H

The behavior of these registers differ according to the mode of operation (PC/AT or PS/2). There exists only one mode register and one Status Register with different bit definitions for PC/AT mode and PS/2 mode. The bit definitions for each register in each mode follows.

FIGURE 1. PC/AT MODE REGISTER (READ PORT 60H AFTER WRITE COMMAND 20H TO PORT 64H)



PC/AT MODE REGISTER

Bit 0 - Enable Keyboard Interrupt (EKI), when set ("1") causes the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Bit 1 - Reserved, should be written as "0".

Bit 2 - System Flag (SYS), when set ("1") writes the System Flag bit of the Status Register to "1". This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Inhibit Override (INH), when set ("1") disables the keyboard inhibit function (AD command).

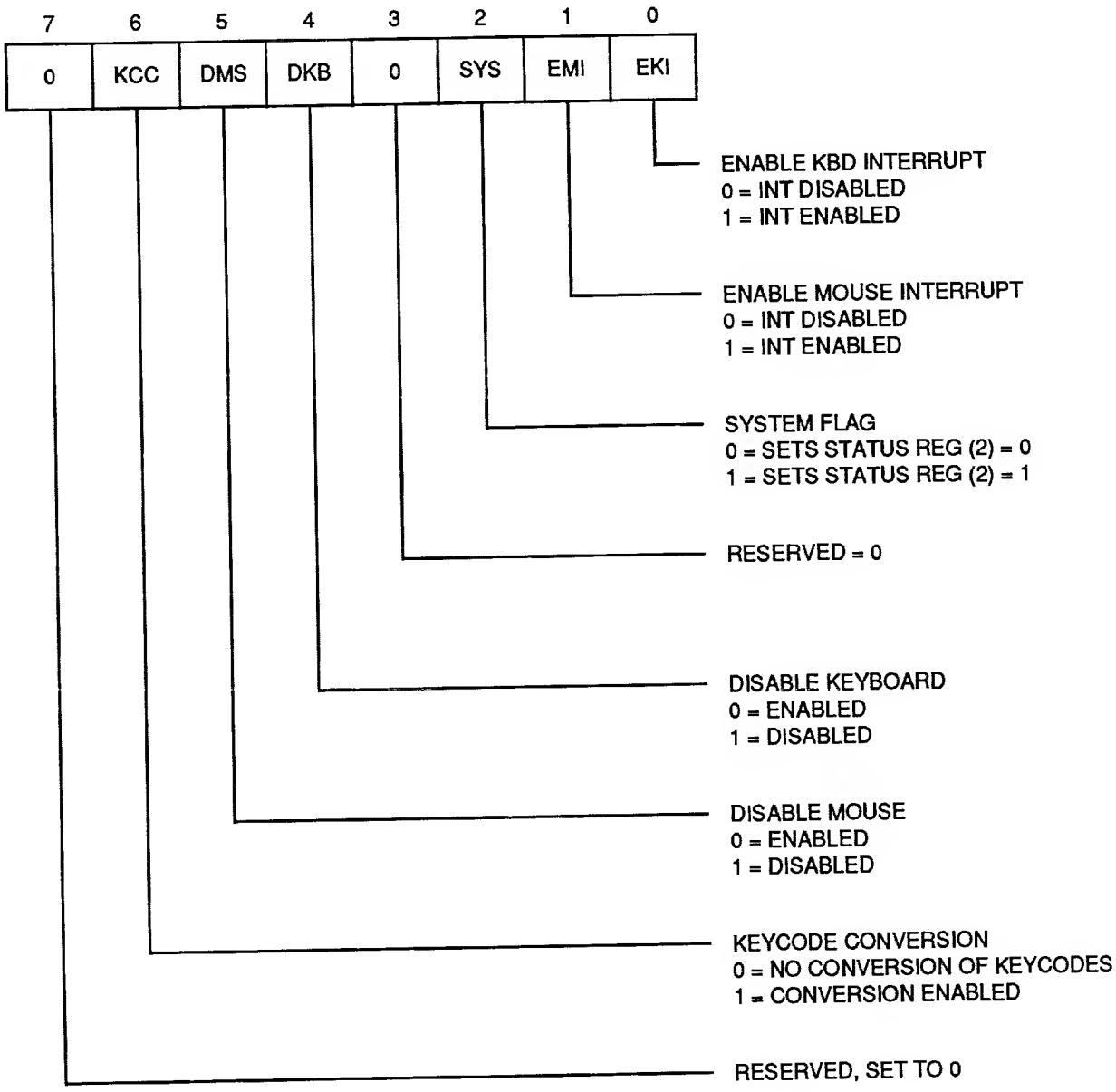
Bit 4 - Disable Keyboard (DKB), when set ("1") disables the keyboard by holding the –KCKOUT line high.

Bit 5 - Keyboard Type (KBD), when set ("1") allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.

Bit 6 - Keycode Conversion (KCC), when set ("1") causes the controller to convert the scan codes to PC format. When reset, the codes (AT keyboard) are passed along unconverted.

Bit 7 - Reserved, should be written as "0".

FIGURE 2. PS/2 MODE REGISTER (READ PORT 60H AFTER WRITE COMMAND 20H TO PORT 64H)



PS/2 MODE REGISTER

Bit 0 - Enable Keyboard Interrupt (EKI), when set ("1") causes the controller to generate a keyboard interrupt whenever data (keyboard or command) is written into the output buffer.

Bit 1 - Enable Mouse Interrupt (EMI), when set ("1") allows the controller to generate a mouse interrupt when mouse data is available in the output register.

Bit 2 - System Flag (SYS), when set ("1") writes the System Flag bit of the Status Register to "1". This bit is used to indicate a switch from virtual to real mode when set.

Bit 3 - Reserved, "0".

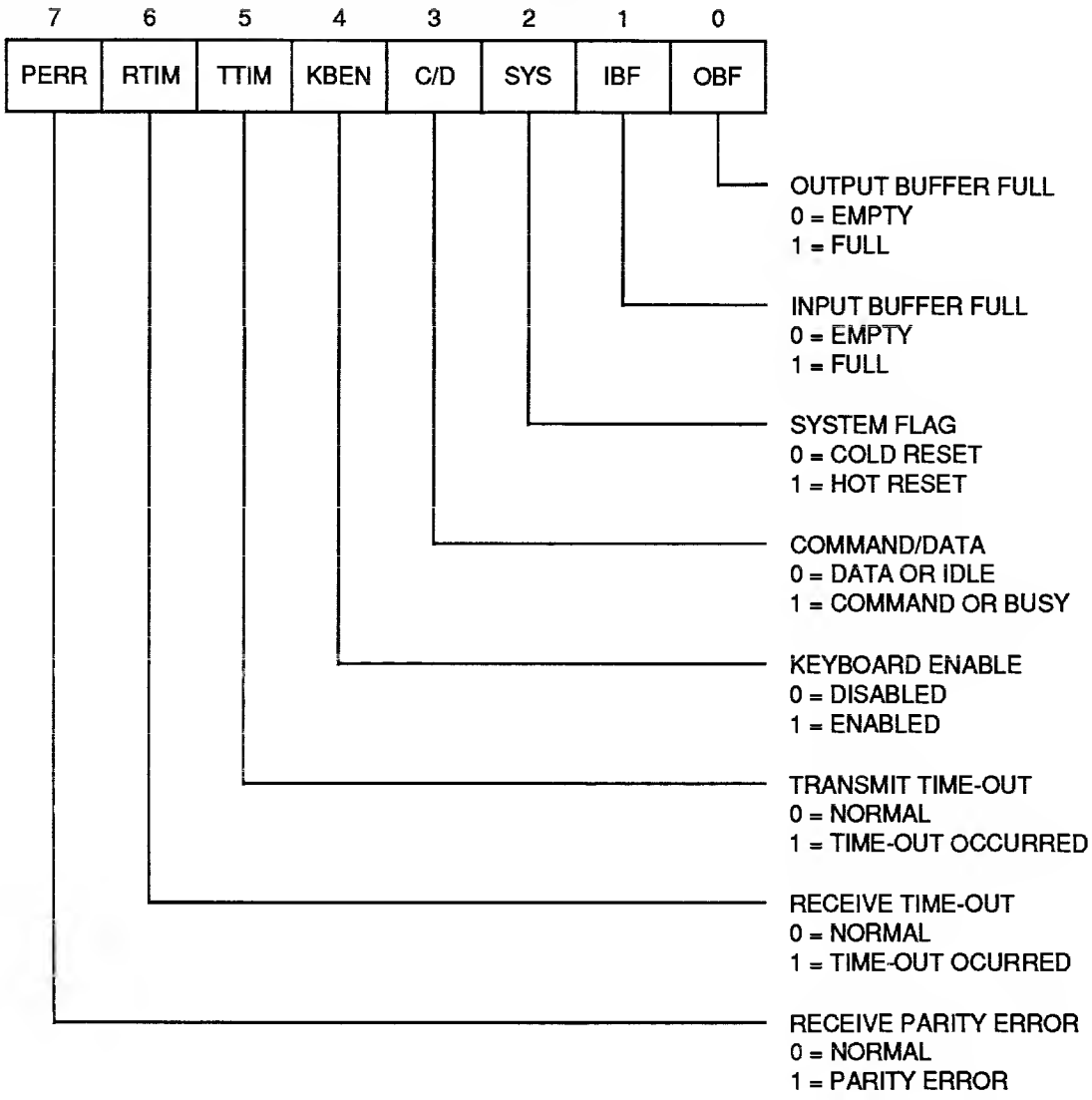
Bit 4 - Disable Keyboard (DKB), when set ("1") disables the keyboard by holding the –KCKOUT high.

Bit 5 - Disable Mouse (DMS), when set ("1") disables the mouse by holding the –MCKOUT high.

Bit 6 - Keycode Conversion (KCC), when set ("1") causes the controller to convert the scan codes to PC format. When reset, the codes (AT keyboard) are passed along unconverted.

Bit 7 - Reserved, "0".

FIGURE 3. PC/AT STATUS REGISTER (READ ONLY - PORT 64H)



PC/AT Status Register

Bit 0 - Output Buffer Full (OBF), when set ("1") indicates that data is available in the controller Data Bus Buffer, and that the CPU has not read the data yet. CPU reads to PORT 60H to reset the state of this bit.

Bit 1 - Input Buffer Full (IBF), when set ("1") indicates that there is a command in Status Register at PORT 64H or data in PORT 60H DBB register and that the controller has not yet performed the command or "processed" the data. It is also set when the controller is executing a command.

Bit 2 - System Flag (SYS), when set ("1") indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (CD), when set ("1") indicates that a command has been placed into the Input Data Buffer of the controller. The controller uses this bit to determine if the byte written is a command to be executed. This bit is not reset until the command has completed its operation.

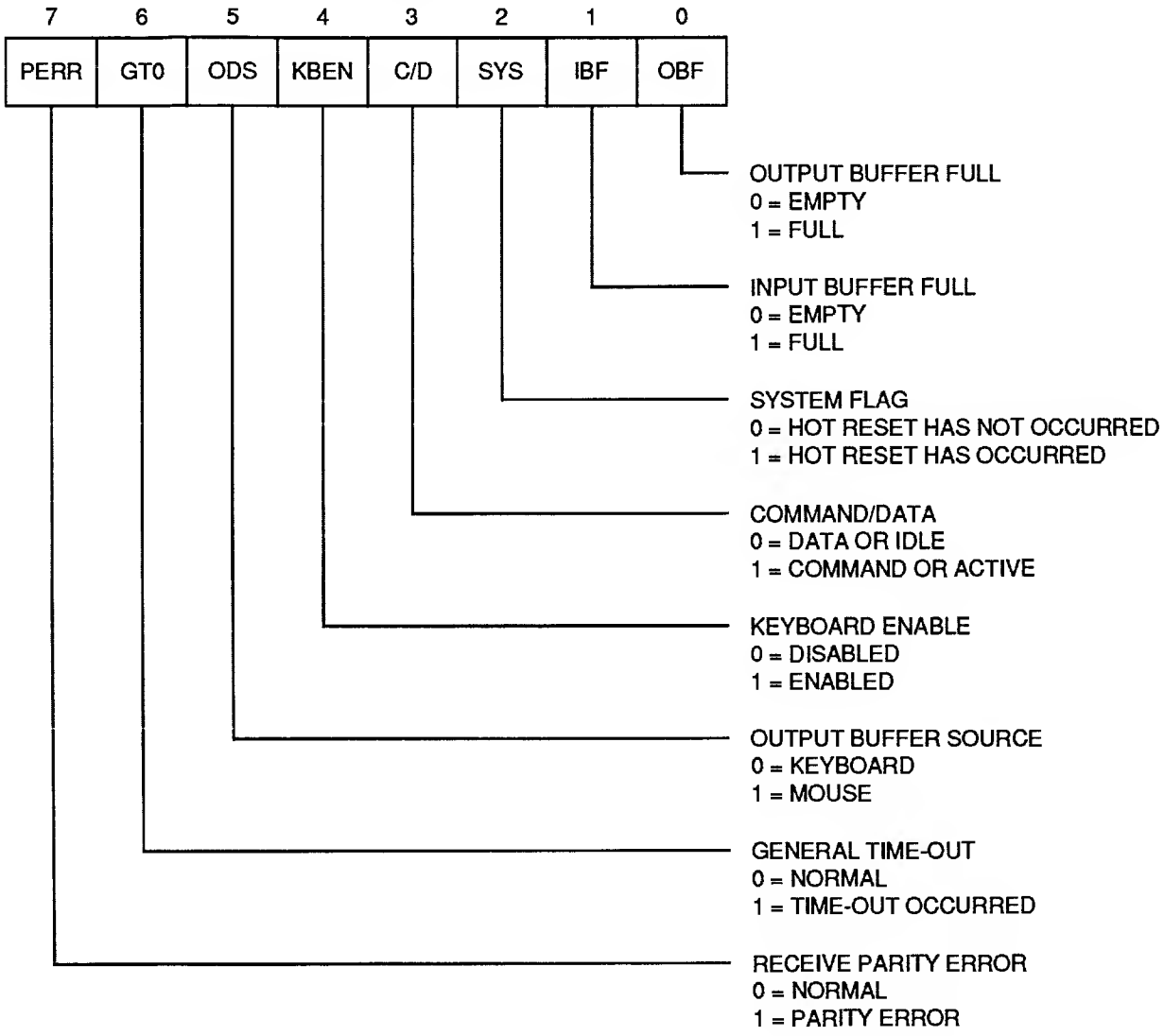
Bit 4 - Keyboard Enable (KBEN), when set ("1") indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.

Bit 5 - Transmit Time-out (TTIM), when set ("1") indicates that a transmission to the keyboard was not completed before the controller's internal timer timed-out.

Bit 6 - Receive Time-out (RTIM), when set ("1") indicates that a transmission from the keyboard was not completed before the controller's internal timer timed-out.

Bit 7 - Parity Error (PERR), when set ("1") indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the KIRQ pin is set ["1" if the EKI bit/ Mode Register bit 0 is set ("1")].

FIGURE 4. PS/2 STATUS REGISTER (READ ONLY - PORT 64H)



PS/2 Status Register

Bit 0 - Output Buffer Full (OBF), when set ("1") indicates that data is available in the controller Data Bus Buffer, and that the CPU has not read the data yet. The CPU reads to PORT 60H reset the state of this bit.

Bit 1 - Input Buffer Full (IBF), when set ("1") indicates that there is a command in Status Register at PORT 64H or data in PORT 60H DBB register and that the controller has not yet performed the command or "processed" the data. It is also set when the controller is executing a command.

Bit 2 - System Flag (SYS), when set ("1") indicates that the CPU has changed from virtual to real mode.

Bit 3 - Command/Data (CD), when set ("1") indicates that a command has been placed into the Input Data Buffer of the controller. The controller uses this bit to determine if the byte written is a command to be executed. This bit is not reset until the command has completed its operation.

Bit 4 - Keyboard Enable (KBEN), when set ("1") indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.

Bit 5 - Output Buffer Data Source (ODS), when set ("1") indicates that the data in the output buffer is mouse data. When reset, it indicates the data is from the keyboard.

Bit 6 - Time-out Error (TERR), when set ("1") indicates that a transmission was started and that it did not complete within the normal time taken (approximately 11 KCKIN cycles). If the transmission originated from the controller a FEH is placed in the output buffer. If the transmission originated from the keyboard a FFH is placed in the output buffer.

Bit 7 - Parity Error (PERR), when set ("1") indicates that a parity error (even parity = error) occurred during the last transmission from the keyboard. When a parity error is detected, the output buffer is loaded with FFH, the OBF Status bit is set and the KIRQ pin is set ["1" if the EKI bit/Mode Register bit 0 is set ("1")].

COMMAND SET

The command set supported by the keyboard controller supports two modes of operation, and a set of extensions to the AT command set for the PS/2. In both modes, the command is implemented by writing the command byte to PORT 64H. Any subsequent data is read from PORT 60H (see description of command 20) or written to PORT 60H (see description of command PORT 60H). The commands for each mode are shown in the table below:

PC/AT Mode:

Comm.	Description
20	Read Mode Register
21-3F	Read Keyboard Controller RAM (Byte 1-31)
60	Write Mode Register
61-7F	Write Keyboard Controller RAM (Byte 1-31)
AA	Self Test
AB	KBD Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port (P10-P17)
D0	Read Output Port (P20-P27)
D1	Write Output Port (P20-P27
E0	Read Test Inputs (T0, T1)
F0-FF	Pulse Output Port (P20-P27)

Added PS/2 Commands:

Comm.	Description
A4	Test Password
A5	Load Password
A6	Enable Password
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
C1	Poll in Port Low (P10-P13 -> S4-S7)
C2	Poll in Port High (P14-P17 -> S4-S7)
D1	Write Output Port B1 (P21)
D2	Write Keyboard Output Buffer
D3	Write Mouse Output Buffer
D4	Write to Mouse

The keyboard controller will support the following command set, which is described as the hex command code, followed by a description:

20 Read the keyboard controller's Mode Register (PC/AT and PS/2) - The keyboard controller sends its current mode byte to the output buffer (accessed by a read of PORT 60H).

21-3F Read the keyboard controller's RAM (PC/AT and PS/2) - Bits D4-D0 specify the address.

60 Write the keyboard controller's Mode Register (PC/AT and PS/2) - The next byte of data written to the keyboard data port (PORT 60H) is placed in the controller's mode register.

61-7F Write the keyboard controller's RAM (PC/AT and PS/2) - This command writes to the internal keyboard controller RAM with the address specified in bits D4-D0.

A4 Test Password Installed (PS/2 only) - This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and KIRQ is asserted (if the EKI bit is set). Test result - FAH means that the password is installed, and F1H means that it is not.

A5 Load Password (PS/2 only) - This command initiates the password load procedure. Following this command the controller will take data from the input buffer port (PORT 60H) until a 00H is detected or a full eight byte password including a delimiter (e.g. <cr>) is loaded into the password latches. Note: this means that during password validation the password can be a maximum of seven bytes with a delimiter such as <cr>.

A6 Enable Password (PS/2 only) - This command enables the security feature. The command is valid only when a password pattern is written into the controller (see A5 command). No other commands will be "honored" until the security sequence is completed and command A6 is cleared.

A7 Disable Mouse (PS/2 only) - This command sets bit 5 of the Mode Register which disables the mouse by driving the –MCKOUT line high.

A8 Enable Mouse (PS/2 only) - This command resets bit 5 of the Mode Register, thus enabling the mouse again.

A9 Mouse Interface Test (PS/2 only) - This command causes the controller to test the mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Mouse Clock Line Stuck Low
02	Mouse Clock Line Stuck High
03	Mouse Data Line Stuck Low
04	Mouse Data Line Stuck High

AA Self Test command (PC/AT and PS/2) - This commands the controller to perform internal diagnostic tests. A 55H is placed in the output buffer if no errors were detected. The OBF bit is set and KIRQ is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT and PS/ 2) - This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Keyboard Clock Line Stuck Low
02	Keyboard Clock Line Stuck High
03	Keyboard Data Line Stuck Low
04	Keyboard Data Line Stuck High

AC Diagnostic Dump (PC/AT only, Reserved on PS/2) - Sends 16 bytes of the controller's RAM, the current state of the input port, the current state of the output port and the controller's status word to the system. All outputs are in scan code format.

AD Keyboard Disable (PC/AT and PS/2) - This command sets bit 4 of the Mode Register to a "1". This disables the keyboard by driving the clock line (–KCKOUT) high. Data will not be sent or received.

AE Keyboard Enable (PC/AT and PS/2) - This command resets bit 4 of the mode byte to a "0". This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT and PS/2) - This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port low (PS/2 only) - P1 bits 0-3 are written into Status Register bits 4-7 until a new command is issued to the keyboard controller.

C2 Poll Input Port high (PS/2 only) - P1 bits 4-7 are written into Status Register bits 4-7 until a new command is issued to the keyboard controller.

D0 Read Output Port (PC/AT and PS/2) - This command causes the controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
0	P20	–RC	–RC
1	P21	A20 Gate	A20 Gate
2	P22	Speed Sel (ENMOD)	–MDOUT
3	P23	Shadow Enable	–MCKOUT
4	P24	Output Buffer Full	KIRQ
5	—	Input Buffer Empty	MIRQ
6	P26	–KCKOUT	–KCKOUT
7	P27	KDOUT	–KDOUT

Note: P22 (bit 2) is the speed control pin used by Award BIOS, and this is different from what is used by Phoenix and AMI.

D1 Write Output Port (PC/AT and PS/2) - The next byte of data written to the keyboard data port (PORT 60H) will be written to the controller's output port. The definitions of the bits are as defined above. For PS/2 mode, this command only affects P21. The next byte of data written to PORT 60H will be written to P21. All other bits will be unaffected.

D2 Write Keyboard Output Buffer (PS/2 only) - The next byte written to the data buffer (PORT 60H) is written to the output buffer (60H) as if initiated by the keyboard [the OBF bit is set ("1") and KIRQ will be set if the EKI bit is set ("1")].

D3 Write Mouse Output Buffer (PS/2 only) - The next byte written to the data buffer (PORT 60H) is written to the output buffer as if initiated by the mouse [the OBF bit is set ("1") and MIRQ will be set if the EMI bit is set ("1")].

D4 Write to Mouse (PS/2 only) - The next byte written to the data buffer (PORT 60H) is transmitted to the mouse.

Note: If data is written to the data buffer (PORT 60H) and the command preceding it did not expect data from the port (PORT 60H) the data will be transmitted to the keyboard.

E0 Read Test Inputs (PC/AT and PS/2) - This command causes the controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Keyboard Data	Keyboard Clock
1	Keyboard Clock	Mouse Clock
3-7	Read as 0's	Read as 0's

F0-FF Pulse Output Port (PC/AT and PS/2) - Bits 0-3 of the controller's output port may be pulsed low for approximately 6 µs. Bits 0-3 of the command specify which bit will be pulsed. A "0" indicates that the bit should be pulsed; a "1" indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port).

IDE Bus Interface Control

Integrated Drive Electronics bus interface control signals are provided by the VL82C106 Combo chip. The timing and drive for these lines are consistent with the Conner Peripherals CP342 Integrated Hard Disk Manual.

A set of signals are used for this interface when the VL82C106 Combo chip is configured to support the IDE interface via IDE_EN, bit 5 of Control Register 1 (RTC Register 51H).

Input Signals:

–IDACT This input signal is active (low) when the drive is busy. It is used to enable the interrupt request (IRQI) to the system.

IDINT This signal indicates an interrupt request to the system. It is used to generate IRQI.

Output Signals:

–CS4 Chip Select 4. This signal is used as the floppy disk chip select. The default decode is 03F4H-03F5H, but may be redefined as described in the section on Combo Chip Control Registers. The IDE_EN control bit of Control Register 1 has no effect on this signal. –CS4 is also active when –CDAK4 is active.

–CS5 Chip Select 5. This signal is used as the –HOST CS0 of the IDE bus. The default decode is 01F0H-01F7H, but may be redefined as described in the section on Combo Chip Control Registers. The IDE_EN control bit of Control Register 1 has no effect on this signal.

–HCS1 This signal is active (low) for address 03F6H-03F7H and is used as –HOST CS1 of the IDE bus.

–IDENH This signal is used to drive the –OE pin of an external 74LS245 buffering bits 8-15 of the IDE data bus to the SD bus. It is active (low) when:

(–CS5 is active AND SA2-SA0 = 000).

–IDENL This signal is used to drive the –OE pin of an external 74LS245 buffering bits 0-6 of the IDE data bus. It is active (low) when:

–CS5 is active OR SA0-SA9 = 3FXH OR –CDAK4 is active.

This allows a simple implementation for an IDE bus that includes both the hard disk controller and the floppy disk controller.

IRQI This is the three-state interrupt request to the CPU. It is normally tied directly to the IRQ14 signal of the system. It reflects the state of the IDINT input and is enabled when –IDACT is low.

–IOCS16 The VL82C106 Combo chip has multiple sources for this signal. It is driven active (low) when:

)–CS5 is active AND SA0-SA2 = 000 AND IDE_EN = 1 AND {(CS_MODE = 0) OR (CS_MODE = 1 AND 16-bit operation selected for CS5)}) OR (any other CS is active with 16-bit operation selected AND CS_MODE = 1) OR (IDE_EN = 0 AND CS5 is active AND 16-bit operation is selected AND CS_MODE = 1).

Bidirectional Signals:

IDB7, –DC The control for the transceiver between IDB7, –DC, and SD7 is as follows:

IDB7 –> SD7 when:

(–CS5 is active OR SA0-SA9 = 3FXH OR –CDAK4 is active) AND –IOR is active AND IDE_EN = 1 AND NOT SA0-SA9 = 3F7H.

–DC –> SD7 when SA0-SA9 = 3F7H AND –IOR is active AND IDE_EN = 1.

SD7 –> IDB7 at all other times.

Combo Chip Control Ports:

Contained in the VL82C106 are a set of 26 registers used for programming peripheral chip select base addresses, chip select address ranges, and enabling options. Each base address register is a 16-bit register with bits corresponding to address bits A15-A0. In addition to base address registers, there is an address range registers that can be used to "don't-care" bits (A0-A5) used in the address range comparison, effectively controlling the address space occupied by the chip select from 1 to 32 bytes. There are also programmable bits to selectively generate wait states, and assert –IOCS16 whenever the corresponding address range is present. These registers are used in groups of three per chip select, and are defined as shown below:

Base Address Register (LSB):

Bit	Description
0	Base Address, Bit A0
1	Base Address, Bit A1
2	Base Address, Bit A2
3	Base Address, Bit A3
4	Base Address, Bit A4
5	Base Address, Bit A5
6	Base Address, Bit A6
7	Base Address, Bit A7

Base Address Register (MSB):

Bit	Description
0	Base Address, Bit A8
1	Base Address, Bit A9
2	Base Address, Bit A10
3	Base Address, Bit A11
4	Base Address, Bit A12
5	Base Address, Bit A13
6	Base Address, Bit A14
7	Base Address, Bit A15

Range Register:

Bit	Description
0	Don't Care, Bit A0
1	Dont' Care, Bit A1
2	Don't Care, Bit A2
3	Don't Care, Bit A3
4	Don't Care, Bit A4
5	Wait State 0
6	Wait State 1
7	8/16 Bit I/O

The only bits that need detailed descriptions are those contained in the Range Register. These bits are defined as follows:

Bits 0 to 4 - Don't Care Bits, when set ("1") causes that corresponding bit to be ignored during the chip select generation, effectively allowing the chip select signals to correspond to a range or ranges of addresses in the space from Base Address + 0 to Base Address + 31.

Bits 5 & 6 - Wait State 0 and 1, these bits determine the number of wait states that will be generated whenever the corresponding chip select signal is generated. They generate wait states according to the following table:

WS1	WS0	Wait States
0	0	1 Wait State
0	1	2 Wait States
1	0	4 Wait States
1	1	8 Wait States

Note: Programmed wait states can only extend the I/O cycle set by the system architecture.

Bit 7- 8/16 Bit I/O, this bit is used to selectively assert –IOCS16 whenever the corresponding chip select signal is generated. When set ("1") the access is defined as an 8-bit access, and –IOCS16 is not asserted.

Default Chip Selects

The VL82C106 Combo chip also has several hard-wired default chip selects for the serial ports, line printer port, floppy disk chip select and hard disk chip select. These default chip selects are used after a reset until the battery-backed programmable values are enabled via bit 3 of the second control register (RTC register 51H). The wait state and non IDE –IOCS16 values are also disabled in this mode. This allows the combo chip to function normally without the need for programming. The default chip selects are:

Select/ Device	Address
COMA	3F8H-3FFH (Bit 3 of RTC Reg 50H = 1) 2F8H-2FFH (Bit 3 of RTC Reg 50H = 0)
COMB	2F8H-2FFH (Bit 3 of RTC Reg 50H = 1) 3F8H-3FFH (Bit 3 of RTC Reg 50H = 0)
LPT	03BCH-03BFH Bit 5, 6 of RTC Reg 50H = 0, 0) 0378H-037BH (Bit 5, 6 of RTC Reg 50H = 1, 0) 0278H-027BH (Bit 5, 6 of RTC Reg 50H = 0,1)
–CS4	03F4H-03F5H
–CS5	01F0H-01F7H
–CS6	03F2H AND –IOW is Active
–CS7	03F7H AND –IOW is Active

Note that on reset, COMA, COMB, LPT, and –CS4 through –CS7 are enabled and set to the hard-wired values.

Combo Chip Control Register

The VL82C106 Combo chip contains a number of programmable options, including peripheral base address and chip select "hole" size. The registers used to provide this control are located in the upper bytes of the RTC address space (PORT 70H). They are defined as follows:

Addr	Usage
69	Control Register 0
6A	Control Register 1
6B	CS1 COMA Base Add LSB
6C	CS1 COMA Base Add MSB
6D	CS1 COMA Range
6E	CS2 COMB Base Add LSB
6F	CS2 COMB Base Add MSB
70	CS2 COMB Range
71	CS3 LPT Base Add LSB
72	CS3 LPT Base Add MSB
73	CS3 LPT Range
74	CS4 FDC Base Add LSB
75	CS4 FDC Base Add MSB
76	CS4 FDC Range
77	CS5 HDC Base Add LSB
78	CS5 HDC Base Add MSB
79	CS5 HDC Range
7A	CS6 Base Add LSB
7B	CS6 Base Add MSB
7C	CS6 Range
7D	CS7 Base Add LSB
7E	CS7 Base Add MSB
7F	CS7 Range

Note: Control Register 0 and 1 are not battery-backed via the VBAT supply.

Control Register 0 (RTC Register 50H or I/O PORT 102H) Bits:

This register contains bits that enable or disable functionality of the internal components of the combo chip. The bits of this register are defined to be consistent with definitions used in the PS/2-50 family.

This register can also be accessed at address 102H, for PS/2 compatibility. The contents of the register are detailed below:

Bit	Usage	Value After Reset
0	SYS BD EN	Enabled (1)
1	FDCS EN (CS4)	Enabled (1)
2	COMA EN (CS1)	Enabled (1)
3	COMA DEF	COM1 (0)
4	LPT EN (CS3)	Enabled (1)
5	LPT DEF 0	Paralled Port 1 (1)
6	LPT DEF 1	Disabled (0)
7	EMODE	Compat. Mode (0)

Bit 0 - System Board Enable (SYS BD EN) Control bit, when set ("1") allows bits 1, 2, and 4 to enable and disable their respective devices. When reset ("0") the floppy disk chip select (CS4), COMA (CS1), and the LPT port (CS3) are disabled regardless of the contents of bits 1, 2, and 4.

Bit 1 - Floppy Disk CS Enable (FDCS EN) Control bit, when set ("1") allows the FD CS signal (CS4) to be asserted to an external floppy disk controller chip. When reset ("0") prevents the assertion of this chip select.

Bit 2 - Communications Port A Enable (COMA EN) Control bit, when set ("1") allows the internal COMA (CS1) port to be accessed. When reset ("0") COMA is disabled.

Bit 3 - Communications Port A Default Address (COMA DEF) Control bit, when set ("1") forces the hard-wired default base address to COMA to correspond to (3F8H-3FBH) and COMB to (2F8H-2FBH). When reset ("0") forces the COMA hard-wired address to (2F8H-2FBH) and COMB to (3F8H-3FBH). The base address will be the programmed values if bit 3 of control register 1 (RTC register 51H) is set.

Bit 4 - Line Printer Port Enable (LPT EN) Control bit, when set ("1") enables the LPT port (CS3). When reset ("0") disables the LPT port.

Bit 5 & 6 - Line Printer Default bits 0 and 1 (LPT DEF 0 and 1) Control bits, set the Line Printer Base hard-wired address defaults as shown below:

Bit 6	Bit 5	Address Range
0	0	03BCH-03BFH
0	1	0378H-037BH
1	0	0278H-027BH
1	1	Reserved

Setting bit 3 of RTC register 51H changes the base address to that set in the program address registers for LPT (CS3).

Bit 7 - Line Printer Extended Mode (EMODE) Control bit, when set ("1") disables the Extended Mode and forces PC/AT compatibility. When reset ("0") the Extended Mode is enabled, allowing the printer port direction to be controlled, and the interrupt status to be latched.

Control Register 1 (RTC Register 51H) Bits

This register is used to control peripheral chip selects that are not included in Control Register 0. The bits in this register are defined as follows:

Bit	Usage	Value After Reset
0	COMB EN	Enabled (1)
1	AT/PS2 KBD	AT (1)
2	PRIV EN	Enabled (1)
3	CS MODE	Hard-wire (0)
4	HDCS EN	Enabled (1)
5	IDE EN	Enabled (1)
6	CS6 EN	Enabled (1)
7	CS7 EN	Enabled (1)

Bit 0 - Communication Port B Enable. A "1" enables COMB (CS2). A zero ("0") disables COMB.

Bit 1 - AT or PS/2 Compatible Keyboard. A "1" selects PC/AT type keyboard controller functions, while a "0" places the keyboard controller in PS/2 mode.

Bit 2 - Private Controls Enable. When in AT mode (AT/PS2_KBD = 1), this bit is used to latch the values of the keyboard controller's output signals KHSE, KSRE, and IRQM to the VL82C106 output pins. When "1" these outputs follow the keyboard controller's outputs. When "0" these outputs held at that value regardless of the keyboard controller's outputs.

When in PS/2 mode (AT/PS2_KBD = 0), this bit has no effect on the KHSE, KSRE, and IRQM output pins. The combo chip outputs follow the keyboard controller's outputs.

Bit 3 - Chip Select Decode Mode. When "0", CS1-CS7 decodes revert to the hardwired address decoding and non IDE –IOCS16 and IOCHRDY generation is disabled. A "1" enables the address decoding, wait state generation and 8/16-bit operation as programmed into the RTC registers 52H-60H. (See sections on Default Chip Selects and Combo Chip Control Register.)

Bit 4 - Hard Disk Chip Select Enable. A "1" enables the Hard Disk Chip Select signal (–CS5), while a "0" disables the chip select.

Bit 5 - Integrated Drive Electronics Enable. A "1" enables the IDE functions of outputs –IDENH, –IDENL, IRQI, –IOCS16, and IDB7 as described in IDE Bus Interface Control section.

Bit 6 - Chip Select 6 Enable. When "0", the –CS6 output is disabled. A "1" enables the address decoding, wait state generation and 8/16-bit operation as programmed into the RTC registers 61H-63H. (See sections on Default Chip Selects and Combo Chjp Control Registers.)

Bit 7 - Chip Select 7 Enable. When "0", the –CS7 output is disabled. A "1" enables the address decoding, wait state generation and 8/16-bit operation as programmed into the RTC registers 64H-66H. (See sections Default Chip Selects and Combo Chip Control Register.)

Miscellaneous Control Signals

–XDDIR This input signal is generated by the VL82C101/VL82C201. It is inactive (low) when data is transferred from the XD bus to the SD bus, i.e., interrupt acknowledge cycles and I/O read accesses to addresses 000H-0FFH.

XDIRS This output signal is to control the direction pin of a transceiver between the XD bus and the SD bus when the Combo chip is on the SD bus. Since the architecture assumes the RTC and Keyboard Controller are on the XD bus, this signal is set active (high) when XDDIR is high or either the RTC or the Keyboard Controller is selected.

XDIRX This output signal is to control the direction pin of the transceiver between the XD bus and the SD bus when the Combo chip is on the XD bus. Since the architecture assumes the peripherals other than the RTC and Keyboard Controller are on the SD bus, this signal is inactive (low) when the XDDIR is low or when –IOR is low and any chip select (CS1-CS7) is generated.

–XDEN This output signal is used to enable the XD bus transceiver when the VL82C106 Combo chip is placed on the XD bus and DMA's are desired for peripherals controlled by the Combo chip selects. It is the AND of –IOR and –IOW (active low when either –IOR or –IOW are active).

–CDAK4 This input will directly produce an active low on –CS4 when active low itself and is used by the IDE logic.

–IOCS16 This output signal is used to indicate to the system that the peripheral being accessed is a 16-bit device. It is set active (low) when a programmed chip select, which specifies 16-bit I/O, is decoded or for certain IDE functions. (See sections on Combo Chip Control Ports and IDE Bus Interface Control.) This signal becomes active on the leading edge of ALE and inactive on the trailing edge of –IOW or –IOR.

IOCHRDY This output signal is used to the lengthen I/O cycle to the peripheral being accessed. It is set inactive (low) for the programmed number of wait states when a programmed chip select, which specifies two, four, or eight wait states, is decoded. (See the section IDE Bus Interface Control.)

Note: Programmed wait states can only extend the I/O cycle, i.e., if the system architecture provides four wait states for 8 bit I/O, programming 1 or 2 has no effect.

When 16 bit programmed chip select operation is selected, IOCHRDY becomes inactive on the leading edge of ALE and active on the trailing edge of –IOW or –IOR. For 8 bit operation or default chip select operation, IOCHRDY is inactive during –IOW or –IOR active.

XTAL1 This pin is the input to the on-board 18.432 MHz crystal oscillator. This pin may also be driven by an external CMOS clock signal at 18.432 MHz.

XTAL2 This pin is the output pin of the internal crystal oscillator and should be left open and unloaded if an external clock signal is applied to the XTAL1 pin. This pin is not capable driving external loads other than the crystal.

–TRI This pin is used for in-circuit testing. When low, all outputs and I/O pins are placed in the high impedance state.

–ICT This pin, when strobed low, places the VL82C106 into test mode, determined by the data on the SD0 thru SD3 pins. The chip will remain in this mode until –RES is asserted. Test mode may be changed by strobing this pin low again with different data on the SD0-SD3 pins.

VL82C37A

CMOS DIRECT MEMORY ACCESS (DMA) CONTROLLER

FEATURES

- Low-power CMOS version of popular 8237A DMA controller
- Four DMA channels
- Individual enable/disable control of DMA requests
- Directly expandable to any number of channels
- Independent auto-initialize feature for all channels
- High performance 8 MHz version available
- Transfers may be terminated by end-of-process input
- Software controlled DMA requests
- Independent polarity control for DREQ and DACK signals

DESCRIPTION

The VL82C37A Direct Memory Access (DMA) Controller serves as a peripheral interface circuit for microprocessor systems, and is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The VL82C37A DMA Controller offers many programmable control features that enhance data throughput and system performance. Dynamic reconfiguration is permitted under program control.

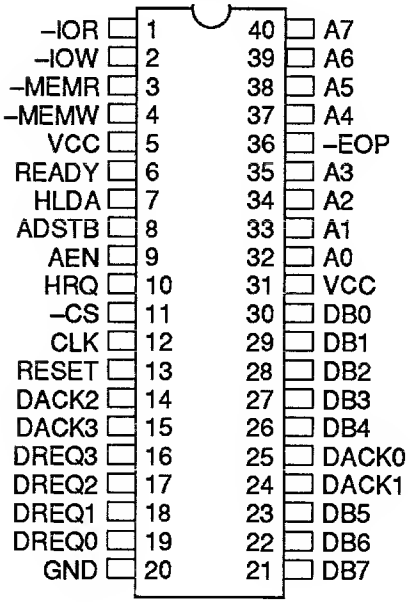
The VL82C37A is designed to be used with an external 8-bit address register such as the 8282. In addition to the four independent channels, the VL82C37A is expandable to any number of channels by cascading additional controller devices.

Three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to auto-initialize to its original condition following an end-of-process (EOP) input. Each channel also has a 64K address and word count handling ability.

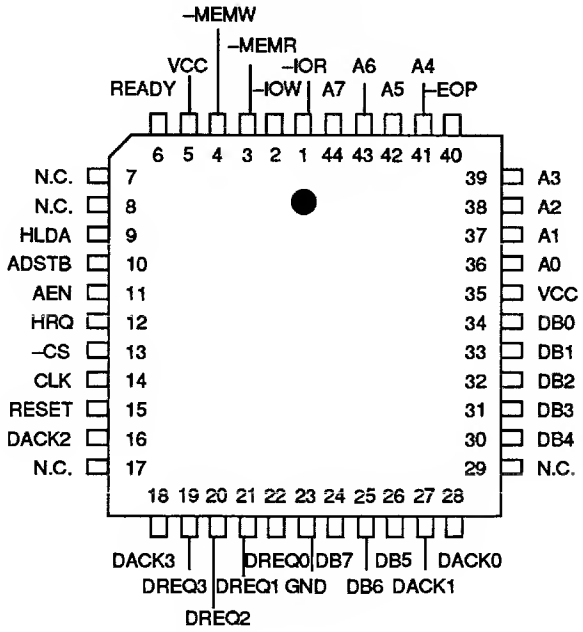
The VL82C37A DMA Controller is available in 5 MHz and 8 MHz clock frequencies.

PIN DIAGRAMS

VL82C37A



VL82C37A



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C37A-05PC VL82C37A-05QC	5 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)
VL82C37A-08PC VL82C37A-08QC	8 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

BLOCK DIAGRAM

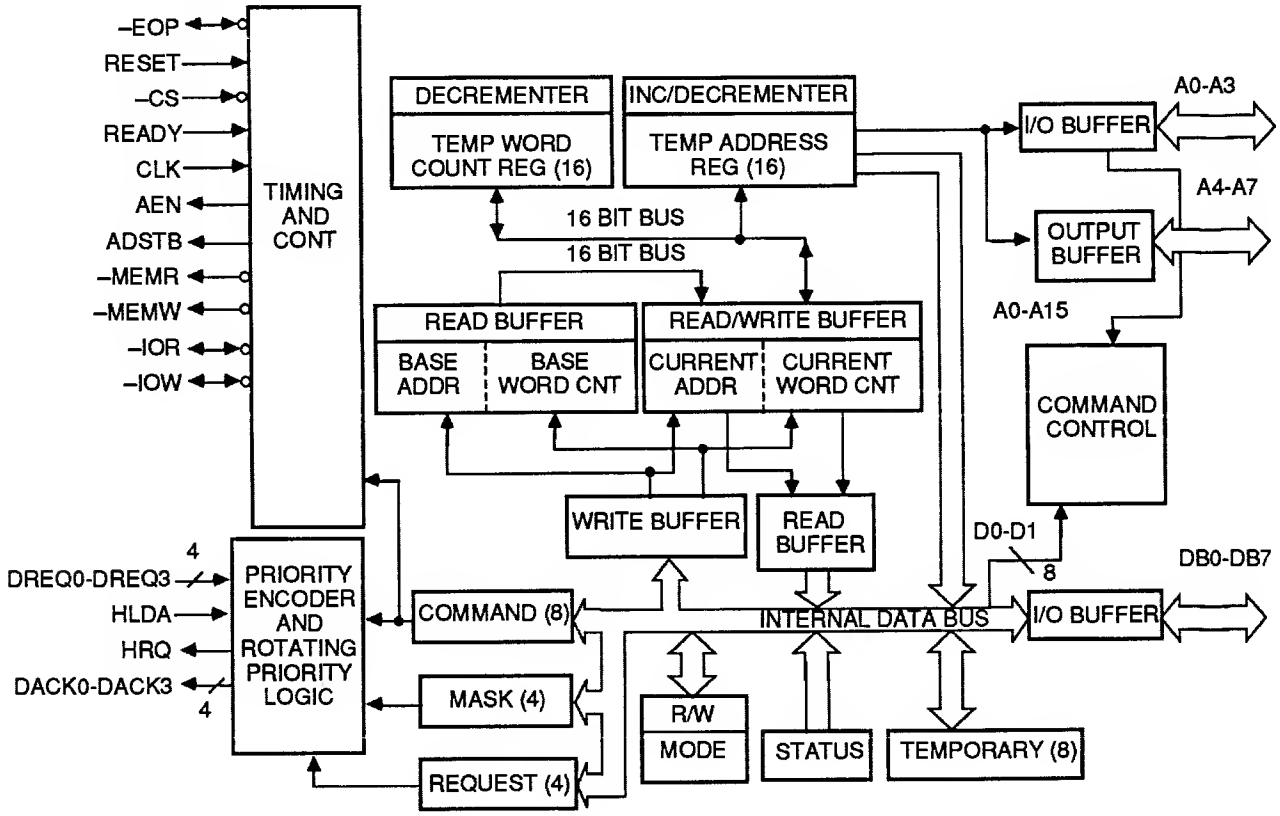


TABLE 1. INTERNAL REGISTERS

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CLK	12	I	Clock Input - Controls the internal operations of the VL82C37A DMA Controller and its rate of data transfers. This input may be driven at up to 5 MHz for the standard VL82C37A-05 and up to 8 MHz for the VL82C37A-08.
–CS	11	I	Chip Select - An active low input used to select the VL82C37A as an I/O device during the idle cycle, allows CPU communication on the data bus.
RESET	13	I	Reset - An active high input that clears the Command, Request, and Temporary Registers, clears the first/last flip-flop, and sets the Mask Register. The device is in the idle cycle following a RESET signal.
READY	6	I	Ready - An input that extends the memory read and write pulses from the VL82C37A accommodating slow memories or I/O peripheral devices. During its specified setup/hold time, READY must not make transitions.
HLDA	7		Hold Acknowledge - This active high signal from the CPU indicates that it has relinquished control of the system buses.
DREQ0-DREQ3	19-16	I	DMA Request - These lines are individual asynchronous channel request inputs. Peripheral circuits use these lines to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Activating the DREQ line of a channel generates a request. DACK then acknowledges the recognition of DREQ signal. Polarity of DREQ is programmable. RESET initializes these lines to active high. DREQ must be sustained until the corresponding DACK becomes active.
DB0-DB7	30-26, 23-21	I/O	Data Bus - These lines are bidirectional, three-state signals that connect to the system data bus. The outputs are enabled in the program condition during the I/O read to output the contents of an Address Register, a Status Register, the Temporary Register, or a Word Count Register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the VL82C37A control registers. During DMA cycles the most significant eight bits of the address are sent onto the data bus and are strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the VL82C37A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs determine the placement of the data, not the new memory location.
–IOR	1	I/O	I/O Read - This is a bidirectional, active low, three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the VL82C37A to access data from a peripheral during a DMA Write transfer.
–IOW	2	I/O	I/O Write - This signal is a bidirectional activelow, three-state line. It is used by the CPU to load information into the VL82C37A DMA Controller. In the active cycle, it is used as an output control signal used by the VL82C37A to load data to the peripheral during a DMA read transfer.
–EOP	36	I/O	End of Process - This is an active low bidirectional signal, which provides data on the completion of DMA services and is available at the bidirectional –EOP pin. The VL82C37A allows an external signal to terminate an active DMA service, by pulling the –EOP input low with an external –EOP signal. The VL82C37A also generates a pulse when the terminal count (TC) for any channel is achieved. This generates an –EOP signal that is active on the –EOP line. When –EOP is received, either internally or externally, it will cause the VL82C37A to terminate the service, reset the request, and, if auto-initialize is enabled, to write the base registers to the current registers

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
			of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by –EOP, unless the channel is programmed for auto-initialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, –EOP will be output when the TC for channel 1 occurs. To prevent erroneous end-of-process inputs, –EOP should be tied high with a pull-up resistor if it is not used.
A0 - A3	32 - 35	I/O	The four least significant address lines - These lines are bidirectional three-state signals. In the idle cycle, they are inputs used by the CPU to address the register to be loaded or read. In the active cycle they are outputs that provide the lower four bits of the output address to the system.
A4 - A7	37 - 40	O	The four most significant address lines - These lines are three-state outputs that provide four bits of address. They are enabled only during the DMA service.
HRQ	10	O	Hold Request - This is the hold request to the CPU. It is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the VL82C37A to issue the HRQ signal. After HRQ is asserted, at least one clock cycle (TCY) must occur before HLDA can be valid.
DACK0 - DACK3	25, 24, 14, 15	O	DMA Acknowledge - This signal is used to notify an individual peripheral when it has been granted a DMA cycle. The sense of these lines is programmable; RESET initializes them to an active low.
AEN	9	O	Address Enable - This active high line enables the 8-bit latch containing the upper eight address bits onto the system address bus. It can also be used to disable other system bus drivers during DMA transfers.
ADSTB	8	O	Address Strobe - This active high is used to strobe the upper address byte into an external latch.
–MEMR	3	O	Memory Read - This active low signal is a three-state output used to access data from a selected memory location during a DMA read or memory-to-memory transfer.
–MEMW	4	O	Memory Write - This signal is an active low three-state output used to write data to a selected memory location during a DMA write or memory-to-memory transfer.
VCC	5, 31		+5 V ±5% power supply
GND	20		Ground.

FUNCTIONAL DESCRIPTION

The internal registers and major logic blocks of the VL82C37A are shown in the block diagram. Data interconnection paths are also shown, but the various control signals between the blocks are not. The VL82C37A contains 344 bits of internal register memory. Table 1 describes these registers and shows them by size. A complete description of the registers and their functions can be found in the Register Descriptions section.

The VL82C37A contains three basic control logic blocks. The Timing Control block generates internal timing and external control signals for the VL82C37A. The program command control block decodes the various commands given to the VL82C37A by the microprocessor before servicing a DMA Request. Further, it decodes the mode control word used to select the type of DMA during the servicing. The priority encoder block settles priority contention between DMA channels requesting service at the same time.

The external clock drives the timing control block. In most VL82C37A systems, this clock will usually be the Ø2 TTL clock from a 8284. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) will not meet VL82C37A-05 (5 MHz) clock low and high time requirements. In this case, an external clock should be used to drive the VL82C37A-05.

DMA OPERATION

The VL82C37A is designed to operate in two major cycles: the idle and active. Several states are contained in each device cycle. The VL82C37A supports seven separate states, each being one full clock period. State I (SI), the inactive state, is entered when the VL82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The VL82C37A has requested a hold, but the processor has not yet responded with an acknowledge. The VL82C37A may still be programmed DA from the CPU. An acknowledge from the CPU signals that DMA transfers may begin. S1, S2, S3 and S4 are the functional states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (WS) can be placed between S2 or S3 and S4 by using the Ready line on the VL82C37A. The data is transferred directly from the I/O device to memory (or vice versa) with –IOR and –MEMW (or –MEMR and –IOW) being active simultaneously. The data is not read into or driven out of the VL82C37A during I/O-to-memory or memory-to-I/O DMA transfers.

To complete memory-to-memory transfers requires a read-from and a write-to-memory. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are needed for each transfer: the first four states (S11, S12, S13, S14), are used for read-from-memory and the last four states (S21, S22, S23, S24), for the write-to-memory of the transfer.

IDLE CYCLE

When no channels are requesting service, the VL82C37A enters the idle cycle and performs SI states, sampling the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device also samples –CS, looking for an attempt by the microprocessor to write or read to the internal registers of the VL82C37A. When –CS is low and HLDA is low, the VL82C37A initiates the program condition. The CPU now establishes, changes or inspects the internal definition of the part by reading from or writing to the internal register. Address lines A0-A3 are inputs to the device. They select registers that will be read or written. The –IOR and –IOW lines are used to select and time reads or writes. Because of the number and size of the internal registers, an internal flip-flop is used to generate one more bit of address. This bit is used to determine the upper or lower byte of the 16-bit address and Word Count Registers. This flip-flop can be reset by a separate software command.

Special software commands executed in the VL82C37A during the program condition are decoded as sets of addresses with the –CS and –IOW signals. The commands do not use the data bus. Clear First/Last Flip-Flop and Master Clear instructions are included.

ACTIVE CYCLE

When the VL82C37A is in the idle cycle and a nonmasked channel requests a DMA service, the device outputs an HRQ to the microprocessor and then enters the active cycle. During this cycle the DMA service takes place, in one of four modes.

In the single transfer mode, the device is programmed to make only one transfer. The word count is decremented and the address decremented or incremented, following each transfer. When the word count is completed from zero to FFFFH, a Terminal Count (TC) causes an auto-initialize if the channel has been so programmed.

The DREQ signal must be held active until DACK becomes active, in order to be recognized. If DREQ is held active for the entire single transfer, HRQ will become inactive and release the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed. In 8080A, 8085AH, 8088, or 8086 systems this insures one full machine cycle execution between DMA transfers. Details of timing between the VL82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

In the block transfer mode, the device is activated by the DREQ signal to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external end of process (–EOP) is encountered. DREQ need only be held active until DACK becomes active. An auto-initialization will occur at the end of the service, if the channel has been programmed for it.

In the demand transfer mode the device is programmed to continue making transfers until a TC or external –EOP is encountered or until the DREQ signal goes inactive. Transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has caught up, the DMA service is re-established by a DREQ signal. During the interval between services, when the microprocessor is operating, the intermediate values of address and word count are stored in the VL82C37A Current Address and Current Word Count Registers. Only an –EOP can

cause an auto-initialize at the end of the service. –EOP is generated either by TC or by an external signal.

The fourth mode cascades multiple VL82C37As together for easy system expansion. The HRQ and HLDA signals from additional VL82C37As are connected to the DREQ and DACK signals of a channel of the primary VL82C37A. This permits the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is not broken, and the new device waits for its turn to acknowledge requests. As the cascade channel of the primary VL82C37A is used only to prioritize the additional device, it does not produce any address or control signals of its own, which could conflict with the outputs of the active channel in the added device. The VL82C37A responds to the DREQ and DACK signal, but all other outputs except HRQ are disabled.

Figure 8 shows two devices cascaded into a primary device using two of the previous channels. This forms a two-level DMA system. More VL82C37A's could be added at the second level by using the remaining channels of the first level. More devices can also be cascaded into the channels of the second level devices, forming a third level.

TRANSFER TYPES

Each of the three modes of active transfer can perform three different types of transfers: read, write and verify. Write transfers move data from an I/O device to the memory by activating –MEMW and –IOR; read transfers move data from memory to an I/O device by activating –MEMR and –IOW.

Verify transfers are pseudo routines: the VL82C37A DMA Controller operates as in read or write transfers generating addresses, and responding to –EOP, and other operations. The memory and I/O control lines remain inactive. The Verify Mode is not permitted during memory-to-memory operation.

To perform block moves of data from one memory address space to another with a minimum of programming, the VL82C37A includes a memory-to-memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The VL82C37A requests a DMA device as usual. After HLDA is true, the device, using eight-state transfers in block transfer mode, reads data from the memory. The channel 0 Current Address Register is the source for the address, and is decremented or incremented as usual. The data byte read from the memory is then stored in the VL82C37A internal Temporary Register. Channel 1 writes the data from the Temporary Register to memory using the address in its Current Address Register and incrementing or decrementing it as usual. The channel 1 current word count is decremented. When the word count goes to FFFFH, a TC is generated causing an –EOP output terminating the service.

Channel 0 may be programmed to hold the same address for all transfers, which permits a single word to be written to a block of memory.

The VL82C37A responds to external –EOP signals during memory-to-memory transfers. In block search schemes data comparators may use this input on finding a match. The timing of memory-to-memory transfers is shown in Figure 10. Memory-to-memory operations can be detected as an active AEN signal with no DACK outputs.

A channel may be set up to auto-initialize by setting a bit in the Mode Register. During initialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following –EOP. The base registers and the current registers are loaded at the same time. They remain unchanged thoughout the DMA service. The mask bit is not set when the channel is in auto-initialize. Following auto-initialize, the channel is prepared to perform another DMA service, without CPU action, as soon as a valid DREQ is detected.

The VL82C37A has two types of priority encoding available as software-selectable options. The fixed priority option sets the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, then 2,1 and the highest priority channel is 0. After recognizing any one channel for service, the other channels are prevented from interferring with that service until it is completed.

In the rotating priority option, the last channel to get service becomes the lowest priority channel with the others rotating in order.

Rotating priority allows a single chip DMA system. Any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from dominating the system.

To achieve even greater throughput where system characteristics permit, the VL82C37A DMA Controller can compress the transfer time to two clock cycles. State S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width, and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 state still occurs when A8-A15 need updating (see the Address Generation section.)

To reduce pin count, the VL82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch, where they may be placed on the address bus. The falling edge of the Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are directly sent by the VL82C37A. Lines A0-A7 are connected to the address bus.

During block and demand transfer mode services, including multiple transfers, the addresses generated will be in order. During a large number of transfers the data held in the external address latch will not change. This data will change when a carry or borrow from A7 to A8 takes place in the normal order of addresses. To expedite transfers, the VL82C37A DMA Controller executes S1

states only when needed to update A8-A15 in the latch. For long services, S1 states and address strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address Register throughout the transfer. The microprocessor reads this register in successive 8-bit bytes. It may also be reinitialized by an auto-initialize to its original value which takes place only after an –EOP.

Current Word Register: Each channel has a 16-bit Current Word Count Register that determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Word Count Register; programming a count of 100 will result in 101 transfers. The word count is decremented after each transfer; the intermediate value of this word count is stored in the register during the transfer. When the value in the register goes from 0 to FFFFH, a TC is generated. The register is then loaded or read in successive 8-bit bytes by the microprocessor in the program condition. Following the end of a DMA service, it may also be reinitialized by an auto-initialization to its original value which occurs only on –EOP. If it is not auto-initialized, this register has a count of FFFFH after TC.

Base Address and Base Word Count Registers: Each channel has a pair of 16-bit Base Address and Base Word Count Registers that store the original value of their associated current registers. Throughout auto-initialization these values are used to restore the current registers to their original values. The base registers are written at the same time with their corresponding current register in 8-bit bytes in the program condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register: This 8-bit register controls the operation of the VL82C37A, is programmed by the microprocessor in the program condition and is cleared by reset or a master clear instruction. Figure 2 lists and describes the function of the command bits.

Mode Register: All channels have a 6-bit Mode Register. When the register is being written to by the microprocessor in the program condition, bits 0 to 1 determine which channel the Mode Register is to be written.

Request Register: The VL82C37A can responds to requests for DMA service that are initiated by software as well as by a DREQ signal. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and can be prioritized by the priority encoder network.

Each register bit is set or reset separately under software control, or is cleared upon generation of a TC or external –EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the correct form of the data word. Table 2 shows register address coding. To make a software request, the channel must be in block mode.

Mask Register: Each channel has an associated mask bit that can be set to disable the incoming DREQ signal. A mask bit is set when its associated channel produces an –EOP, if the channel is not programmed for auto-initialize. Any bit of the 4-bit Mask Register may also be set or cleared separately under software control. The entire register is set by a reset, which disables all DMA requests until a clear Mask Register instruction allows them to occur. This instruction to separately set or clear the mask bits is similar in form to that used with the Request Register.

Status Register: The Status Register is available to be read out of the VL82C37A DMA Controller by the microprocessor and contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set each time a TC is reached by that channel or an external –EOP is applied and are cleared upon reset and on every status read. Bits 4 through 7 are set whenever their corresponding channel is requesting service.

Temporary Register: The Temporary Register is used to hold data during memory-to-memory transfers. The last word moved can be read by the microprocessor in the Program Condition following the completion of the transfers. The Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a reset.

Software Commands: These additional special software commands can be executed in the program condition and do not depend on any specific bit pattern on the data bus.

The clear first/last flip-flop command is executed prior to writing or reading new address or word count information to the VL82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

The Master Clear software instruction has the same effect as the hardware reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The VL82C37A enters an idle cycle.

The Clear Mask Register command clears the mask bits of all four channels, enabling them to accept DMA requests.

PROGRAMMING

The VL82C37A DMA Controller accepts programming from the host processor any time that HLDA is inactive, even if the HRQ signal is active. The host must assure that programming and HLDA are mutually exclusive. A problem can occur if a DMA request occurs, on an unmasked channel while the VL82C37A is being programmed.

For example, the CPU may be starting to reprogram the two-byte Address Register of a channel when that channel receives a DMA request. If the VL82C37A is enabled (bit 2 in the command register is 0) and that channel is unmasked, a DMA service will occur after one byte of the Address Register

has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming another registers. Once the programming is complete, the controller can be enabled (unmasked).

After power-up all internal locations, including the Mode Registers, should be loaded with a valid value. This should be done to unused channels as well.

APPLICATION

Figure 1 shows a convenient method for configuring a DMA system with the VL82C37A DMA Controller and an 8080A/8085AH microprocessor system. Whenever there is at least one valid DMA request from a peripheral device, the multimode VL82C37A DMA Controller issues a HRQ to the processor.

When the processor replies with a HLDA signal, the VL82C37A takes control of the address, data, and control buses. The address for the first transfer operation is output in two bytes - the least significant eight bits on the eight address outputs, and the most significant eight bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high-speed, 8-bit, three-state latch in a 20-pin DIP package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are available when one VL82C37A DMA Controller is used.

FIGURE 1. SYSTEM INTERFACE

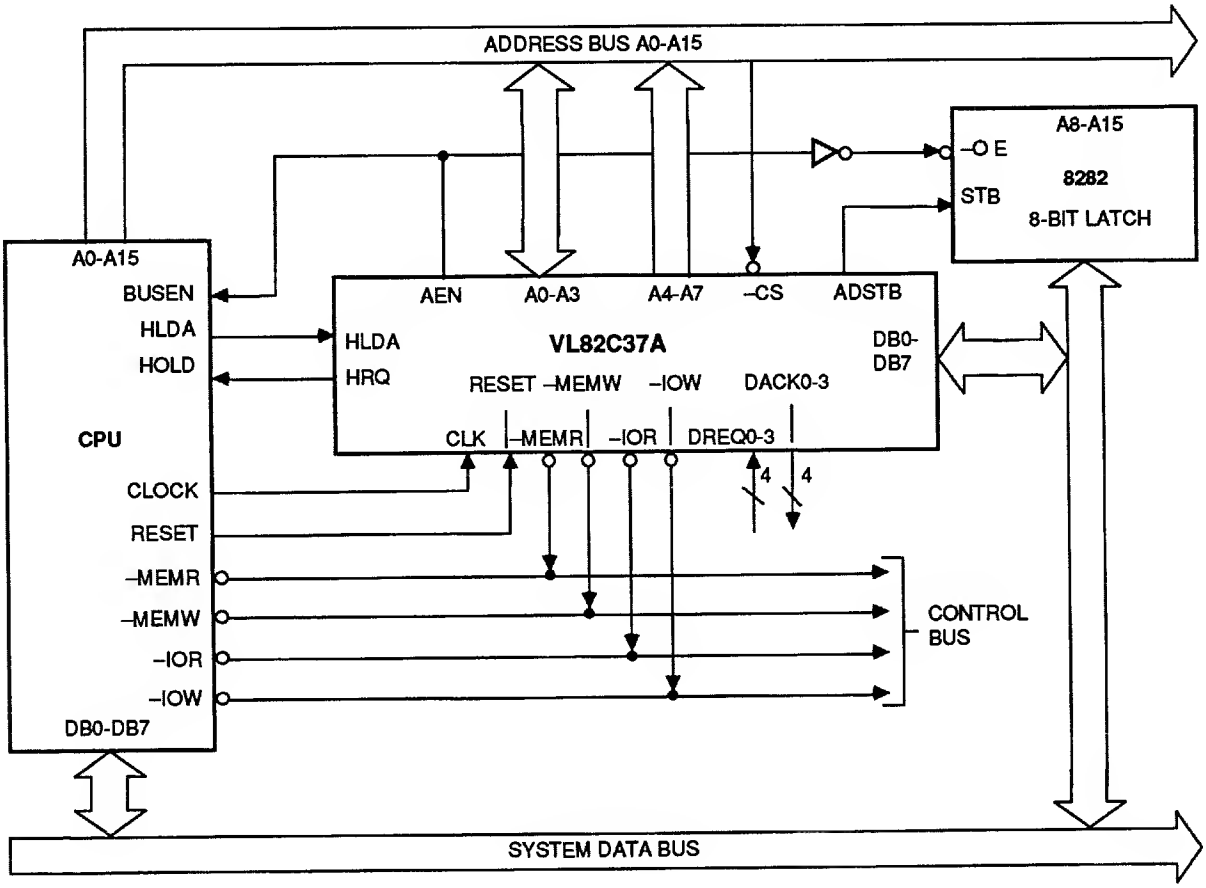


FIGURE 2. COMMAND REGISTER

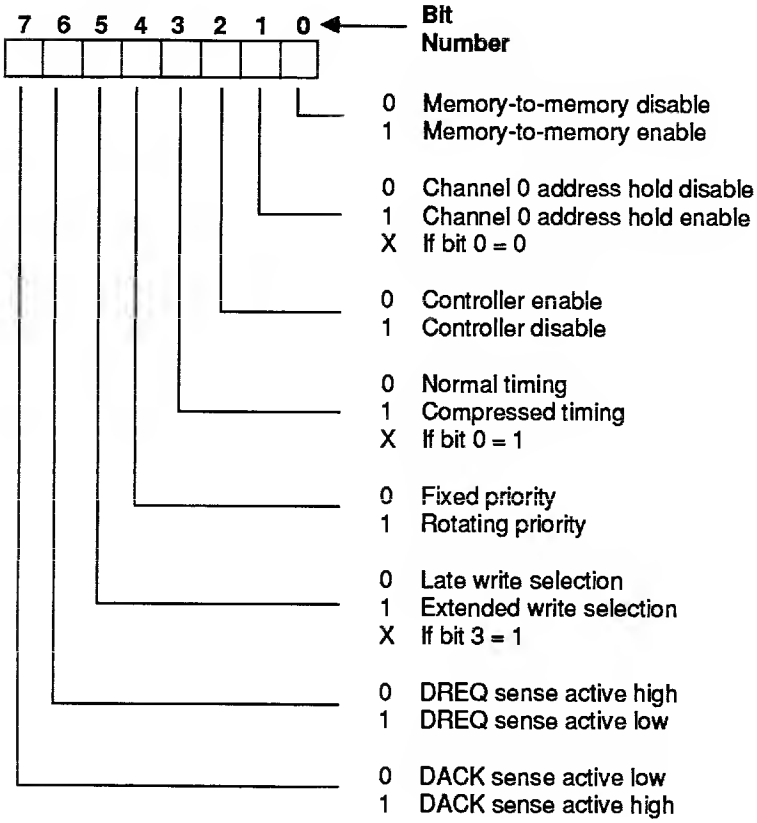


FIGURE 3. MODE REGISTER

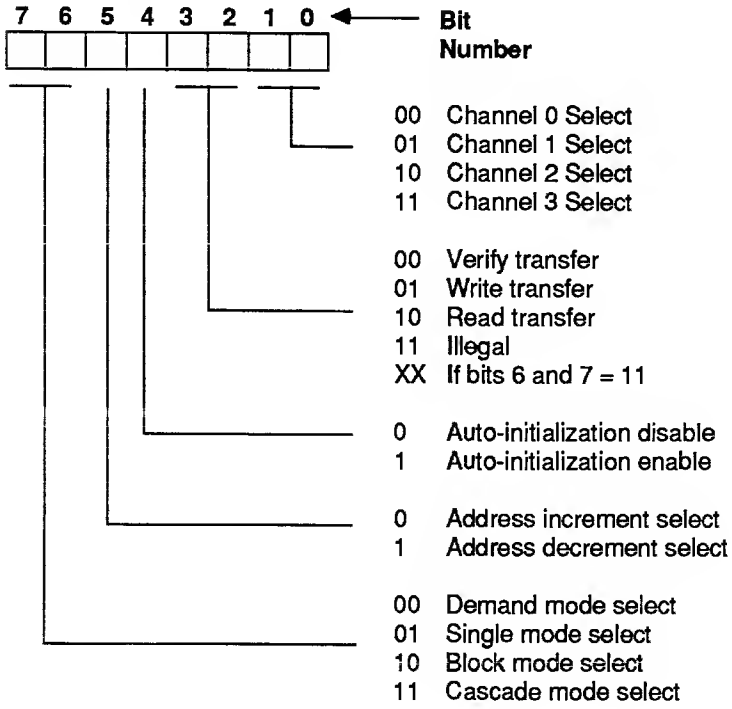


FIGURE 4. REQUEST REGISTER

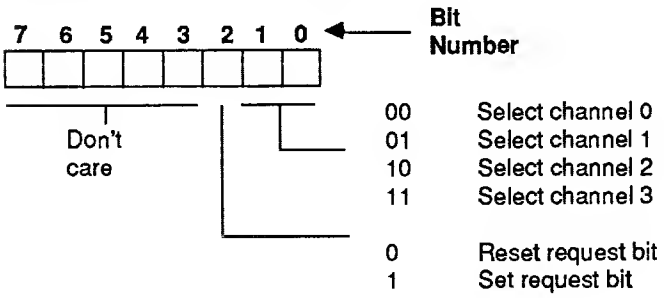


FIGURE 5. STATUS REGISTER

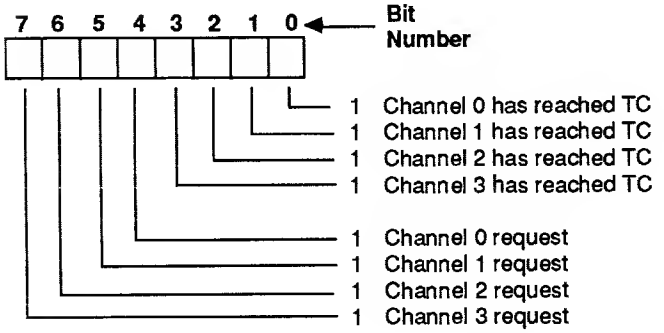


FIGURE 6. MASK REGISTER (SELECT MODE)

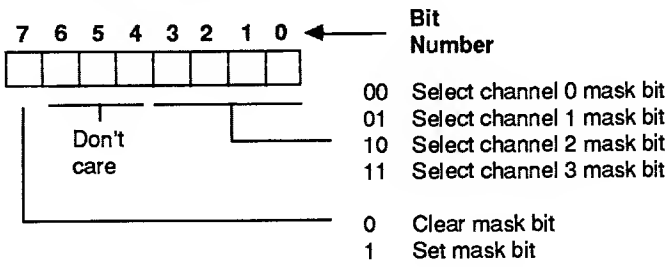


FIGURE 7. MASK REGISTER (MASK MODE)

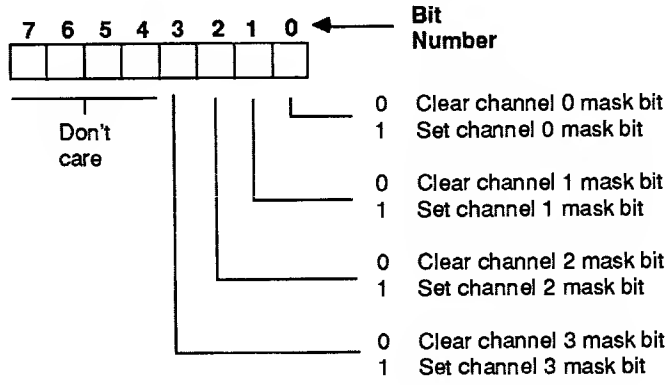


TABLE 2. REGISTER CODES

Register	Operation	Signals						
		–CS	–IOR	–IOW	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

TABLE 3. SOFTWARE COMMAND CODES

Signals						Operation
A3	A2	A1	A0	–IOR	–IOW	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

FIGURE 8. CASCADED VL82C37A CONTROLLERS

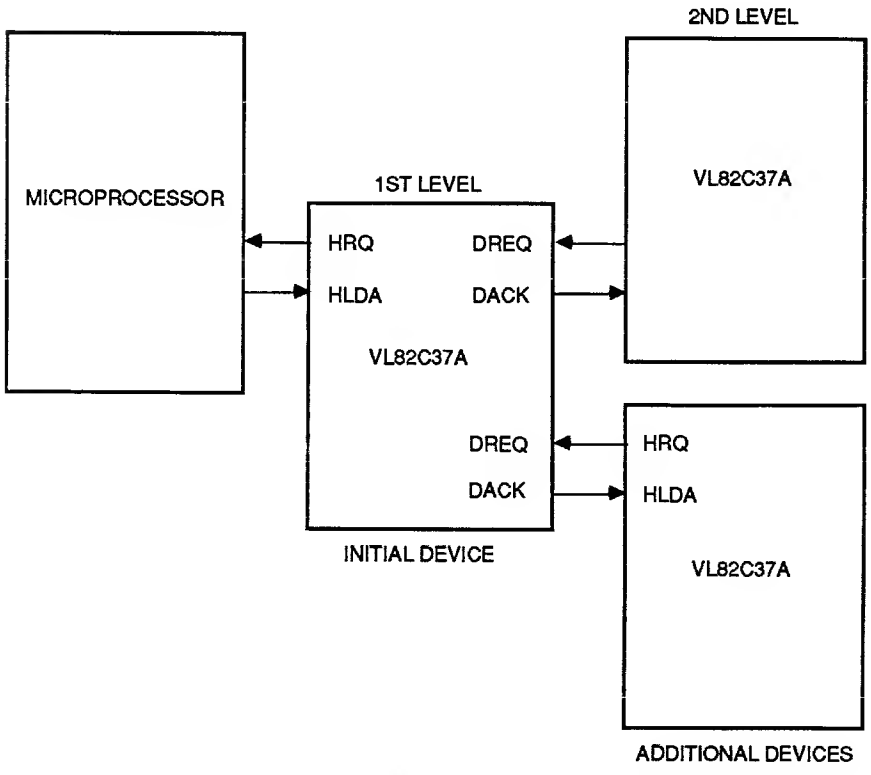


TABLE 4. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

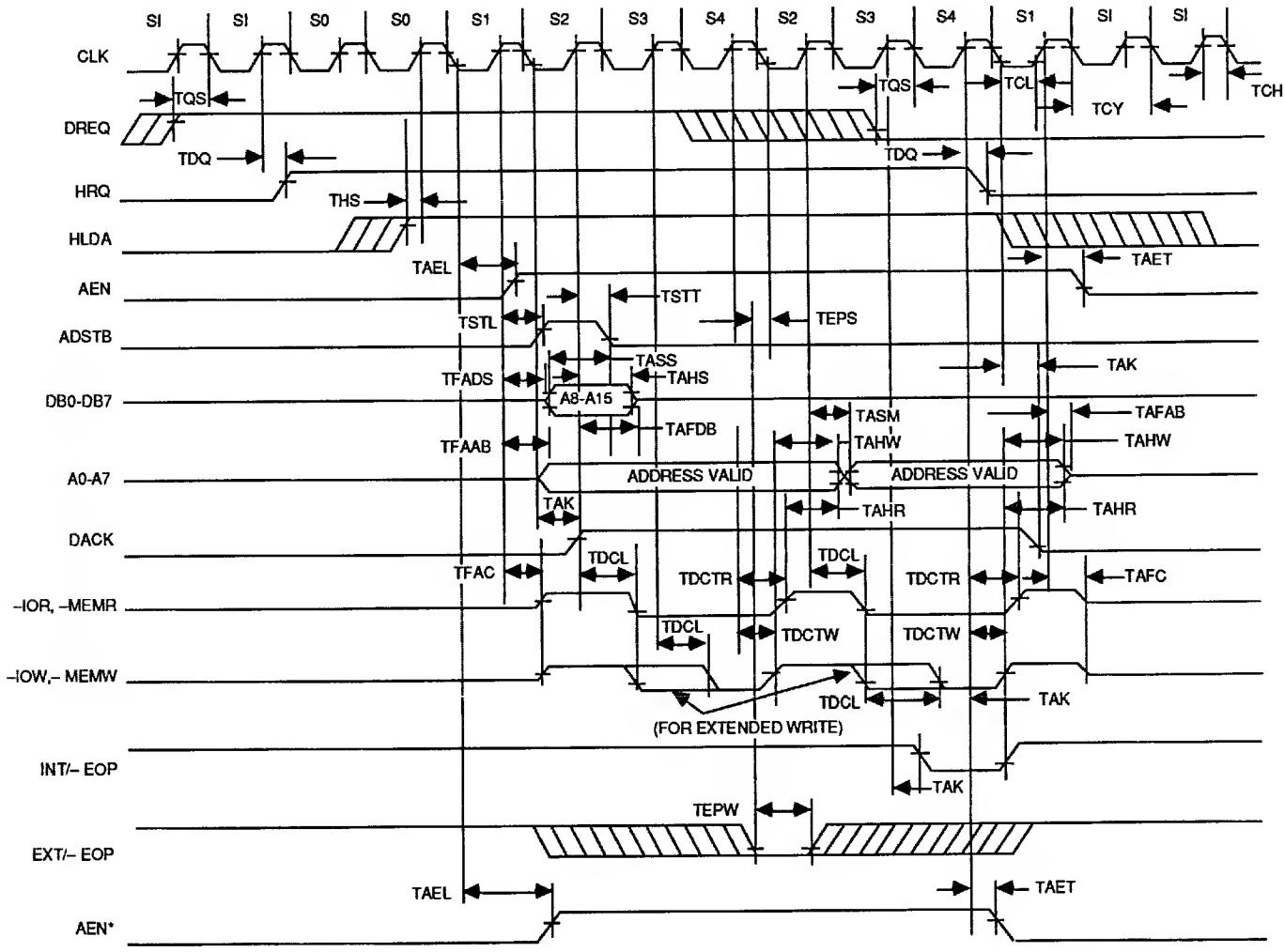
Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			–CS	–IOR	–IOW	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

TABLE 5. DMA MODE AC CHARACTERISTICS

Symbol	Parameter	VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	
TAEL	AEN High from CLK Low (S1) Delay Time		200		105	ns
TAET	AEN Low from CLK High (S1) Delay Time		130		80	ns
TAFAB	ADR Active to Float Delay from CLK High		90		55	ns
TAFC	Read or Write Float from CLK High		120		75	ns
TAFDB	DB Active Float Delay from CLK High		170		135	ns
TAHR	ADR from Read High Hold Time	TCY-100		TCY-75		ns
TAHS	DB from ADSTB Low Hold Time	30		40		ns
TAHW	ADR from Write High Hold Time	TCY-50		TCY-50		ns
TAK	DACK Valid from CLK Low Delay Time (Note 7)		170		105	ns
	–EOP High from CLK High Delay Time (Note 10)		170		105	ns
	–EOP Low from CLK High Delay Time		170		105	ns
TASM	ADR Stable from CLK High		170		105	ns
TASS	DB to ADSTB Low Setup Time	100		65		ns
TCH	Clock High Time (Transitions ≤ 10 ns)	80		55		ns
TCL	Clock Low Time (Transitions ≤ 10 ns)	68		43		ns
TCY	CLK Cycle Time	200		125		ns
TDCL	CLK High to Read or Write Low Delay (Note 4)		190		120	ns
TDCTR	Read High from CLK High (S4) Delay Time (Note 4)		190		115	ns
TDCTW	Write High from CLK High (S4) Delay (Note 4)		130		80	ns
TDQ1	HRQ Valid from CLK High Delay Time (Note 5)		120		75	ns
TDQ2			120		75	ns
TEPS	–EOP Low from CLK Low Setup Time	40		25		ns
TEPW	–EOP Pulse Width	220		135		ns
TFAAB	ADR Float to Active Delay from CLK High		170		100	ns
TFAC	Read or Write Active from CLK High		150		90	ns
TFADB	DB Float to Active Delay from CLK High		200		110	ns
THS	HLDA Valid to CLK High Setup Time	75		45		ns
TIDH	Input Data from –MEMR High Hold Time	0		0		ns
TIDS	Input Data to –MEMR High Setup Time	170		90		ns
TODH	Output Data from –MEMW High Hold Time	10		10		ns
TODV	Output Data Valid to –MEMW High	125		90		ns
TQS	DREQ to CLK Low (S1,S4) Setup Time	0		0		ns
TRH	CLK to READY Low Hold Time	20		20		ns
TRS	READY to CLK Low Setup Time	60		35		ns
TSTL	ADSTB High from CLK High Delay Time		130		110	ns
TSTT	ADSTB Low from CLK High Delay Time		90		65	ns

Explanatory notes follow DC Characteristics Table.

FIGURE 9. DMA TRANSFER TIMING (SEE TABLE 5.)



* In Cascade Mode the AEN signal returns low in the S4 cycle one cycle earlier than when in single transfer mode.

FIGURE 10. MEMORY-TO-MEMORY TRANSFER TIMING (SEE TABLE 5)

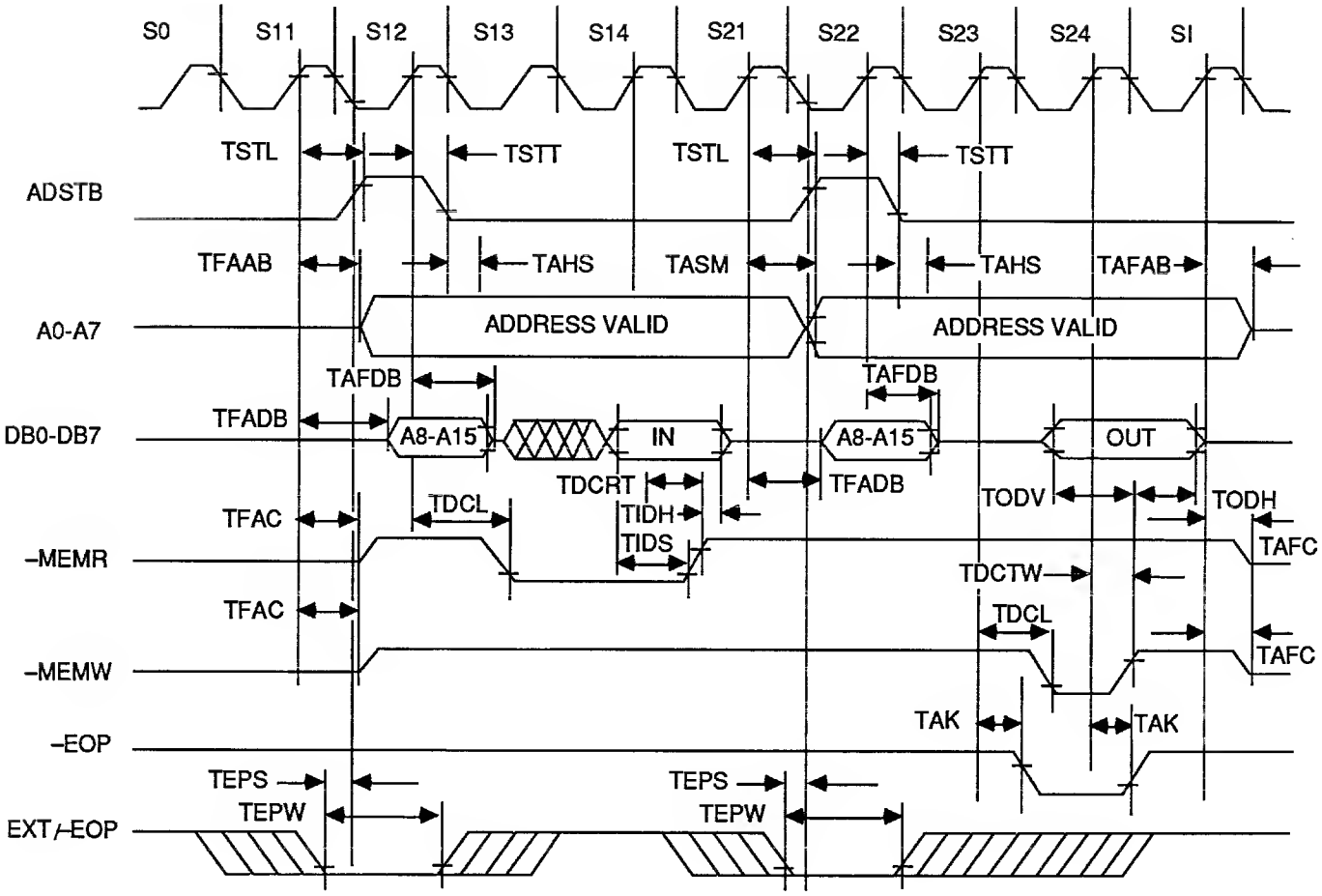


TABLE 6. PERIPHERAL MODE AC CHARACTERISTICS

Symbol	Parameter	VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	
TAR	ADR Valid or –CS Low to Read Low	50		30		ns
TAW	ADR Valid to Write High Setup Time	130		80		ns
TCW	CS Low to Write High Setup Time	130		80		ns
TDW	Data Valid to Write High Setup Time	130		80		ns
TRA	ADR or CS Hold from Read High	0		0		ns
TRDE	Data Access from Read Low (Note 3)		140		120	ns
TRDF	DB Float Delay from Read High	0	70	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		ns
TRSTS	RESET to First –IOWR	2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		ns
TRW	READ Width	200		155		ns
TWA	ADR from Write High Hold Time	20		10		ns
TWC	CS High from Write High Hold Time	20		10		ns
TWD	Data from Write High Hold Time	30		20		ns
TWWS	Write Width	160		100		ns

Explanatory notes follow DC Characteristics

FIGURE 11. SLAVE MODE WRITE TIMING (SEE TABLE 6)

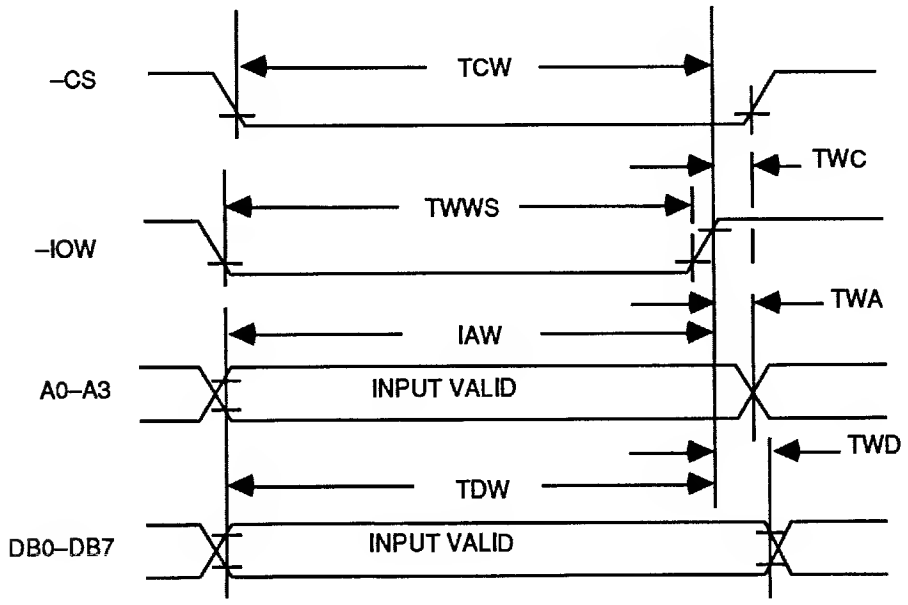


FIGURE 12. SLAVE MODE READ TIMING (SEE TABLE 6)

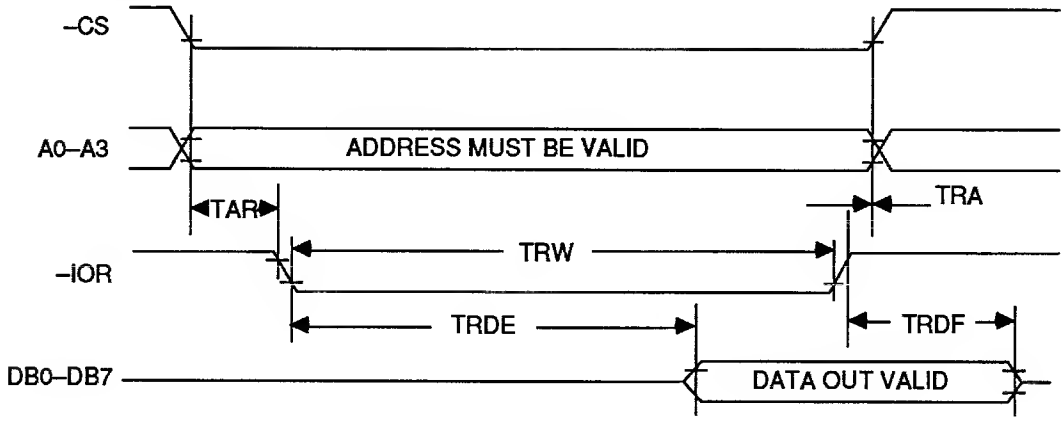


FIGURE 13. READY TIMING (SEE TABLE 5)

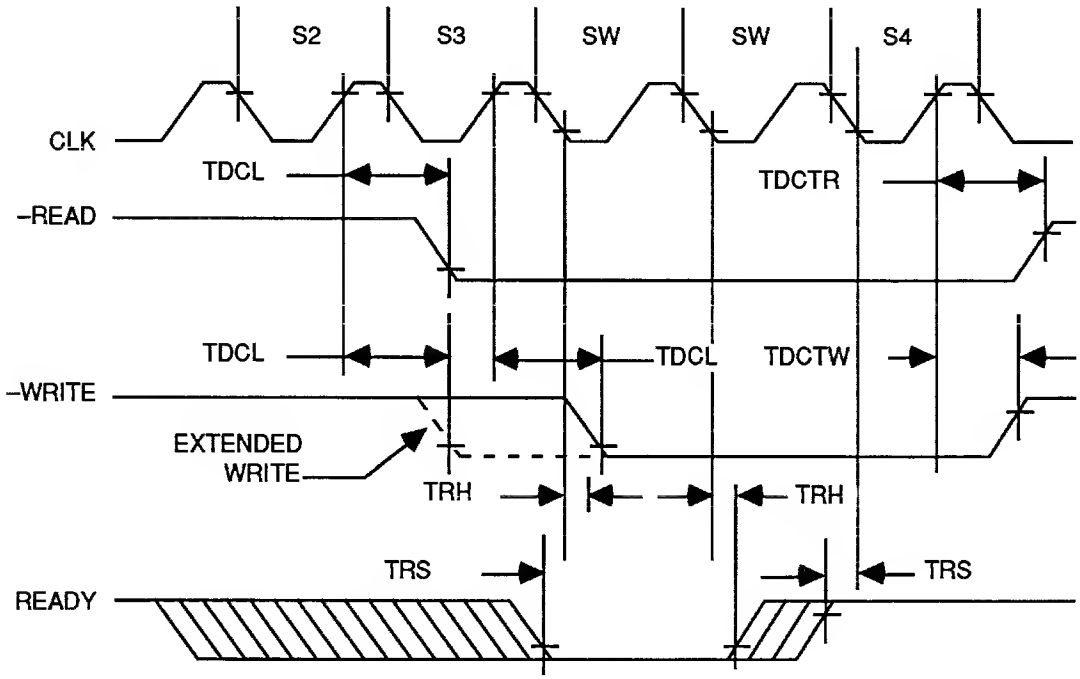


FIGURE 14. COMPRESSED TRANSFER TIMING (SEE TABLE 5)

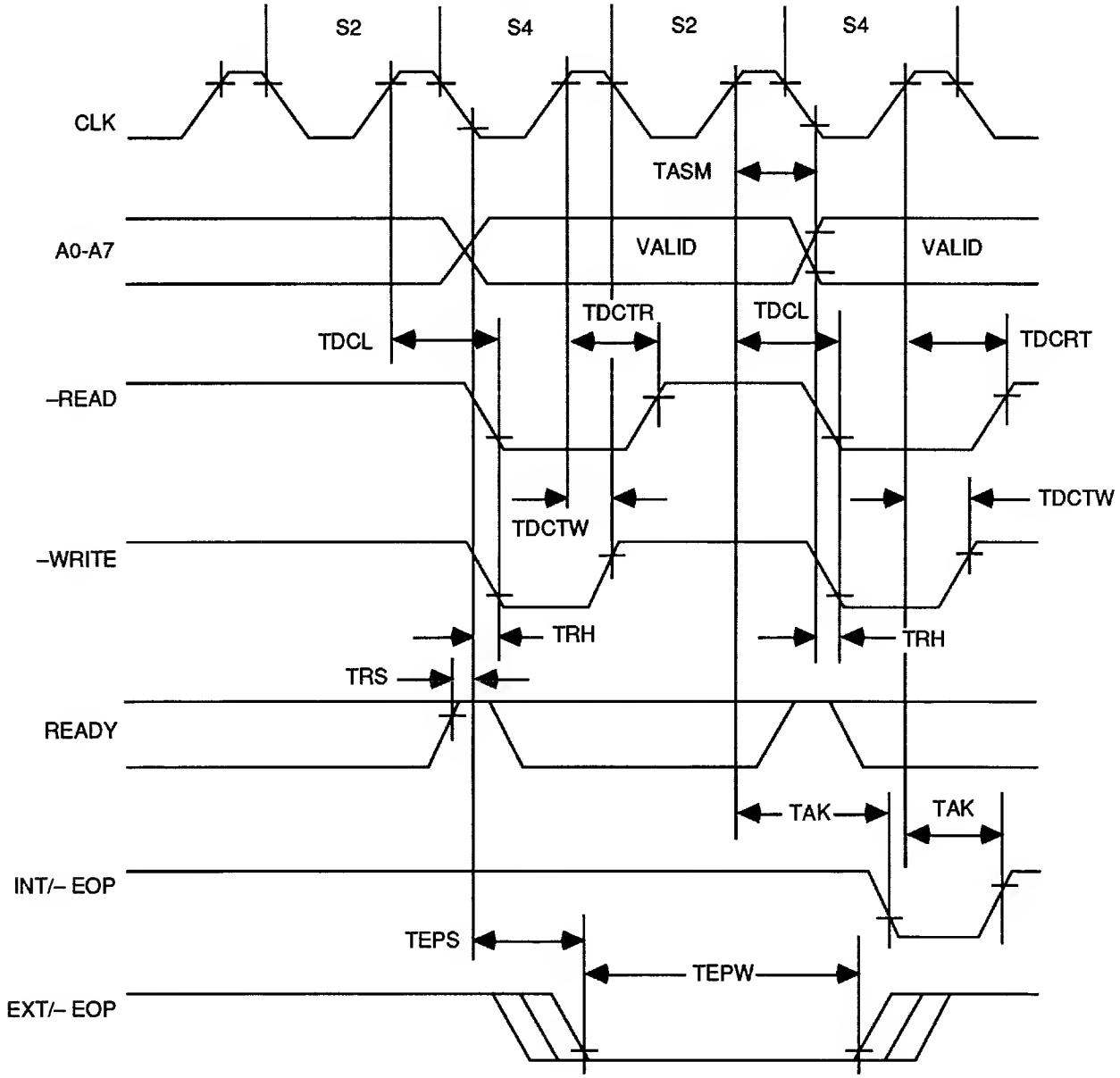
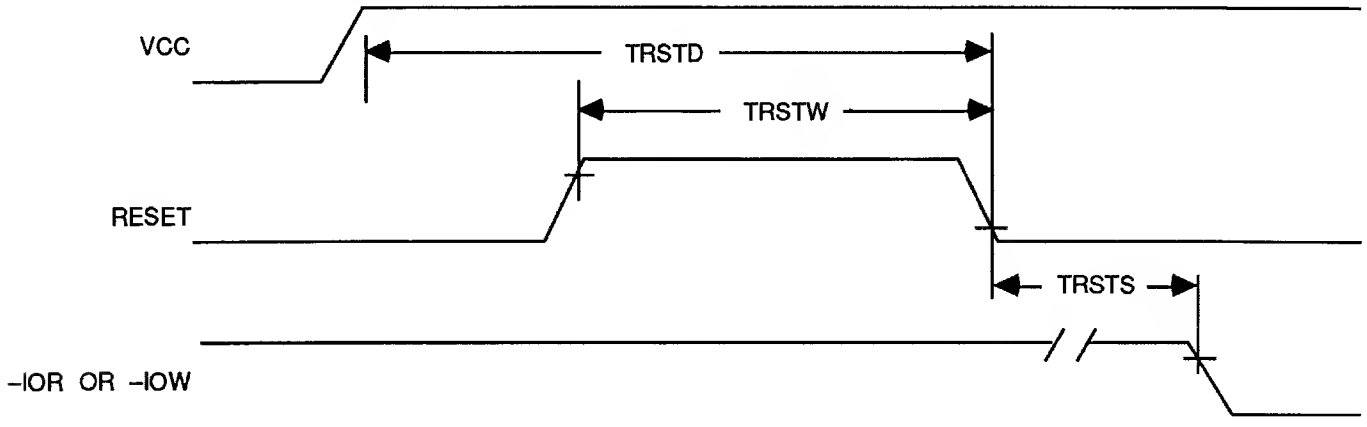


FIGURE 15. RESET TIMING (SEE TABLE 6)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 to 7.0 V
Input Voltage	–0.5 to 5.5 V
Output Voltage	–0.5 to 5.5 V
Operating Temperature	0°C to +150°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS:

Symbol	Parameter	Min	Typ (1)	Max	Unit	Test Conditions
VOH	Output High Voltage	2.4			V	IOH = –200 µA
		3.3			V	IOH = –100 µA (HRQ Only)
VOL	Output Low Voltage			450	mV	IOL = 2.0 mA (data bus) –EOP IOL = 3.2 mA (other outputs) (8) IOL = 2.5 mA (ADSTB) (8)
VIH	Input High Voltage	2.2		VCC + 0.5	V	
VIL	Input Low Voltage	–0.5		0.8	V	
ILI	Input Load Current			±10	µA	0 V ≤ VIN ≤ VCC
ILO	Output Leakage Current			±10	µA	0.45 V ≤ VOUT ≤ VCC
ICC	VCC Supply Current			30	mA	Clk. Freg. = 5 MHz, 8 MHz
C0	Output Capacitance		4	8	pF	fC = 1.0 MHz, Inputs = 0 V
C1	Input Capacitance		8	15	pF	
CIO	I/O Capacitance		10	18	pF	

AC and DC Characteristics Notes:

1. Typical values are for TA = 25°C, nominal supply voltage, and nominal processing parameters.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0 V for high and 0.8 V for low, unless otherwise noted.
3. Output loading is one TTL gate plus 150 pF capacitance, unless otherwise noted.
4. The net –IOW or –MEMW pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net –IOR or –MEMR pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output high levels: TDQ1 is measured at 2.0 V, TDQ2 is measured at 3.3 V. The value for TDQ2 assumes an external 3.3K ohm pull-up resistor connected from HRQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Successive read and/or write operations, by the external processor, to program or examine the controller must be timed to allow at least 400 ns for the VL82C37A-05 and at least 250 ns for the VL82C37A-08, as recovery time between active read or write pulses.
9. –EOP is an open-collector output. This parameter assumes the presence of a 2.2 kΩ pull-up resistor to VCC.
10. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended, however, that pin 5 be tied to VCC.

NOTES:

VLSI TECHNOLOGY, INC.

SECTION 7

APPLICATION INFORMATION

Logic Products Division


VLSI TECHNOLOGY, INC.

FIGURE 1. 386SX/387SX TO VLSI PC/AT 80286 CHIP SET (Cont.)

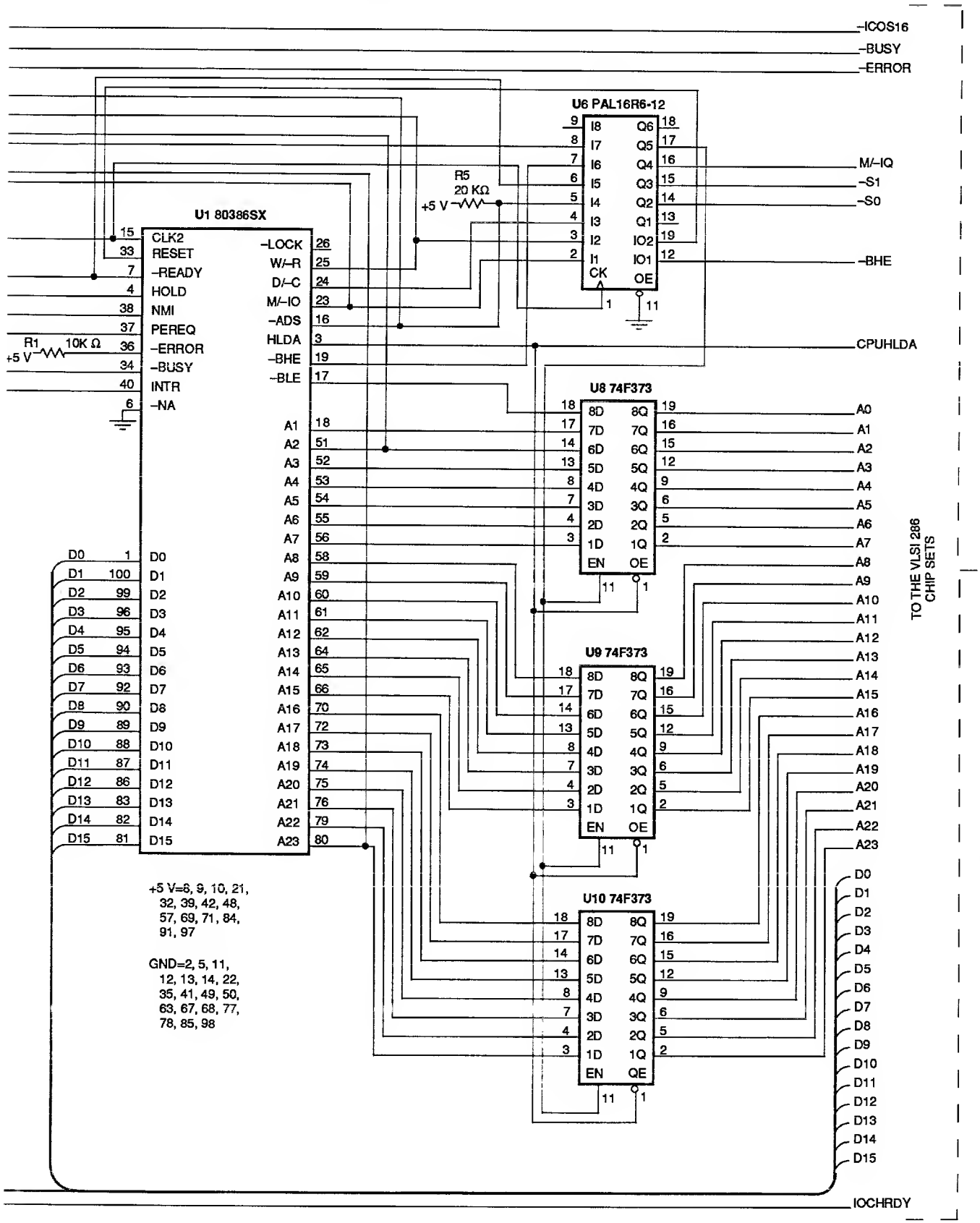


TABLE 1. 386SX PAL EQUATIONS

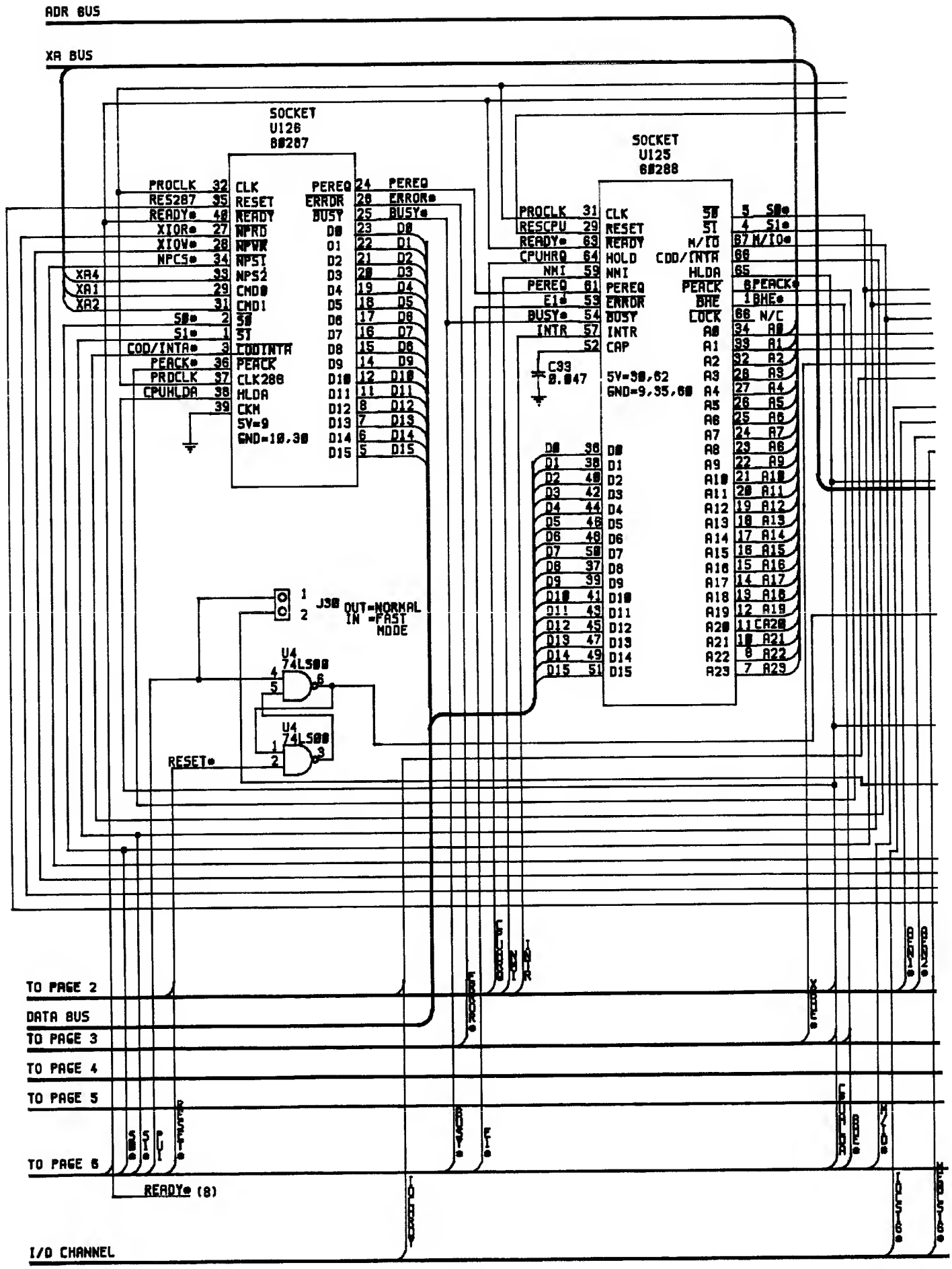
```
TITLE   386SX TO 286 STATUS
PATTERN P9-286.PAL
REVISION B
AUTHOR  AL WEIDNER
COMPANY VLSI PHOENIX, AZ.
DATE    10/25/88

CHIP    P9TO286          PAL16R6
;PIN#  1     2       3     4     5      6     7     8      9     10
     CLK2 MIO3    WRT3  CMD3  /ADS /RDY286 /BHE3 RST286  NC    GND
;PIN# 11    12      13    14    15     16    17    18     19    20
     /OE /BHE2  /SFAZ1 /S0   /S1    MIO   ADS2  SYSCLK RST386 VCC


EQUATIONS
/ADS2 := /(ADS*/ADS2)                    ;2ND PHASE OF ADS, WHETHER READY OR NOT

BHE2  = BHE3*ADS2 + BHE2*/ADS2           ;LATCHED /BHE

SFAZ1:= ADS2*RDY286                      ;1ST STAT PHASE, ALWAYS FOLLOWS ADS
                                         ; WHEN READY

/SYSCLK := SYSCLK + SFAZ1                ;INTERAL SYSCLK - SYNC EACH STATUS CYC.

/RST386 = /(RST286 + RST386*RST286       ;RESET TO TURN OFF ONLY DURING PHASE 2
        +   RST386*SYSCLK)

/MIO := /((ADS*MIO3)+(/ADS*MIO))         ;286 MIO, LATCHED BY ADS

S1    := ADS2*RDY286*/WRT3               ;286  S1, HELD FOR 2 PHASE STAT CYCLE
       + ADS2*RDY286*/CMD3*MIO3          ; 0 ALL OTHER TIMES
       + SFAZ1*S1

S0    := ADS2*RDY286*WRT3*MIO3           ;286 S0,  HELD FOR 2 PHASE STAT CYCLE
       + ADS2*RDY286*CMD3*WRT3           ; 0 ALL OTHER TIMES
       + ADS2*RDY286*/MIO3*/CMD3*/WRT3
       + SFAZ1*S0
```

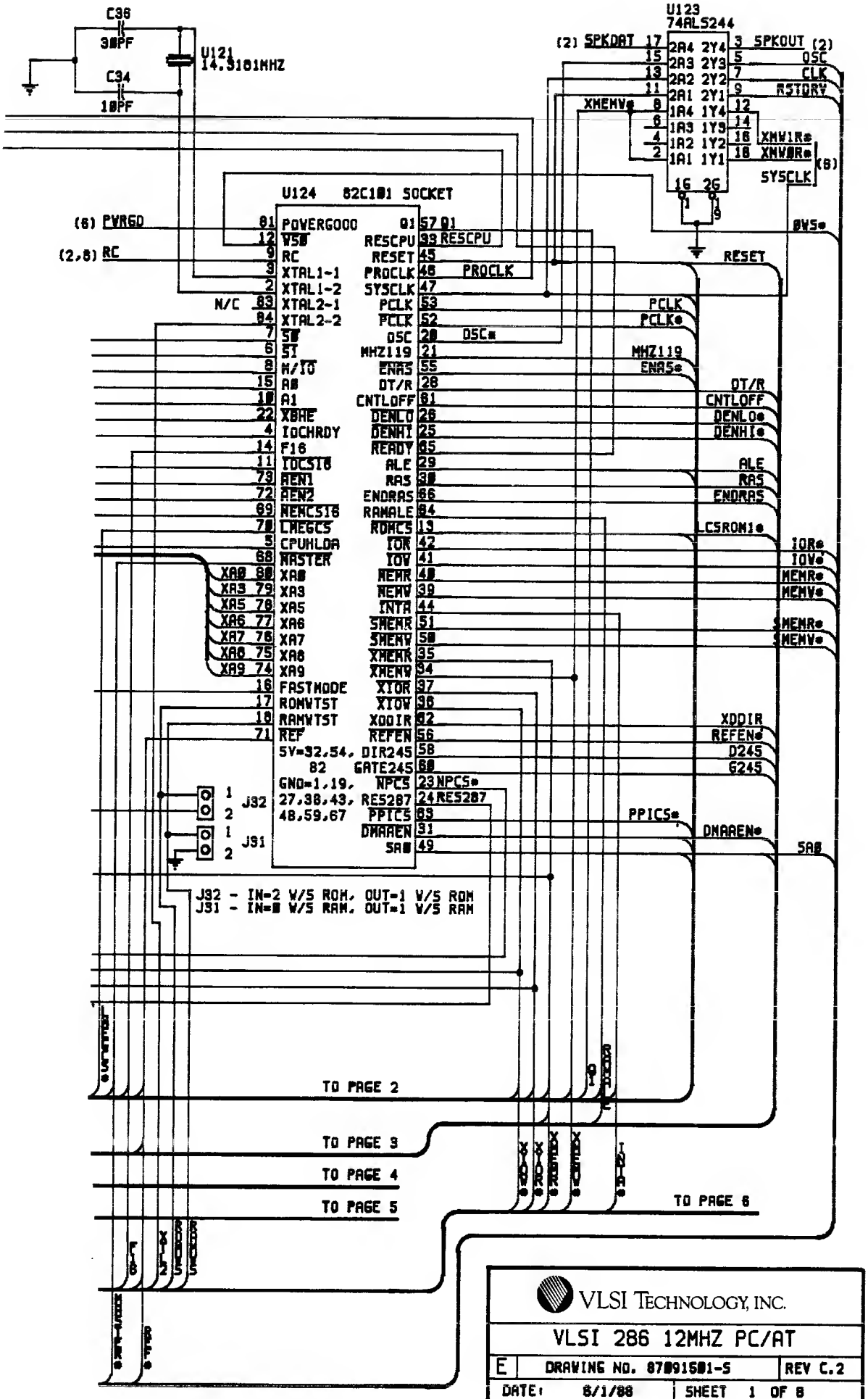
TABLE 2. 387SX PAL EQUATIONS

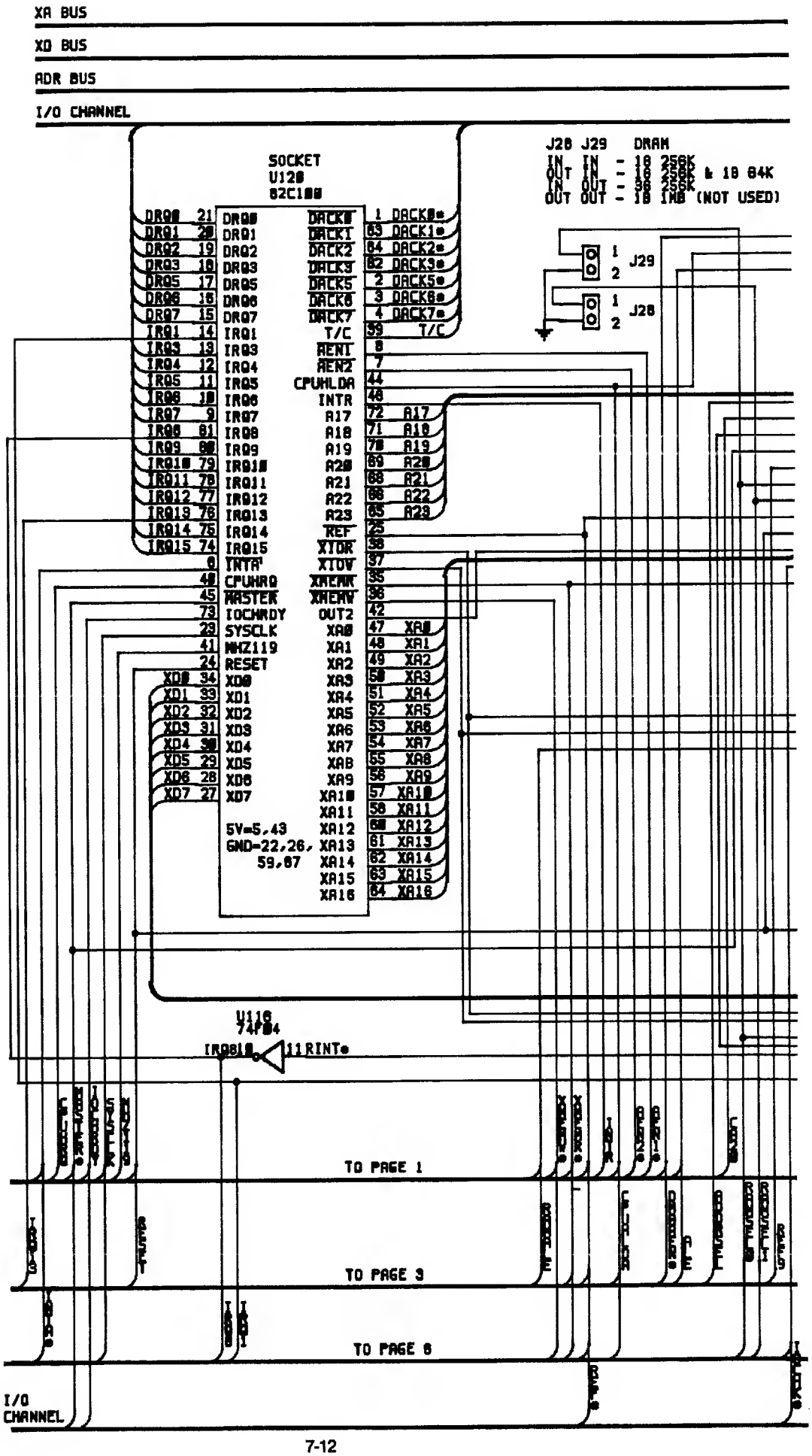
```
TITLE 387SX INTERFACE PAL
PATTERN 387SX.PDS
REVISION B
AUTHOR  AL WEIDNER
COMPANY VLSI PHOENIX, AZ.
DATE    11/16/88

CHIP    387SX   PAL16R8
;PIN#
;1       2        3       4       5       6       7       8       9       10
CLK4    NC     RES287M   NC      NC      NC      NC      NC      NC      GND
;11     12       13      14      15      16      17      18      19      20
/ENAS  IORDY    /Q5     /Q4     /Q3     /Q2     /Q1     /Q0    RES387   VCC

EQUATIONS

;6 BIT COUNTER - COUNTS WHEN RES287M IS HIGH, RESETS TO 0 WHEN RES287M IS LOW
;
Q0      := RES287M * /Q0
Q1      := RES287M * (Q1:+:Q0)
Q2      := RES287M * (Q2:+:(Q1*Q0))
Q3      := RES287M * (Q3:+:(Q2*Q1*Q0))
Q4      := RES287M * (Q4:+:(Q3*Q2*Q1*Q0))
Q5      := RES287M * (Q5:+:(Q4*Q3*Q2*Q1*Q0))

/IORDY  := RES287M * /(Q5*Q4*Q3*Q2)      ;PULLS IORDY (LOW) UNTIL CNT = 3Ch,
                                         ; THIS CAUSES RES287M TO STAY HIGH

/RES387 := /RES287M + Q5                ;GENERATES THE 387SX RESET FOR 32 CLKS

;DESCRIPTION
; PULLS "IOCHRDY" TO HOLD THE CPU WHILE THE 387SX IS PERFORMING ITS RESET
; SEQUENCE.
; ALSO GENERATES A LONGER RESET (32 CLKS WIDE) TO THE 387SX
```

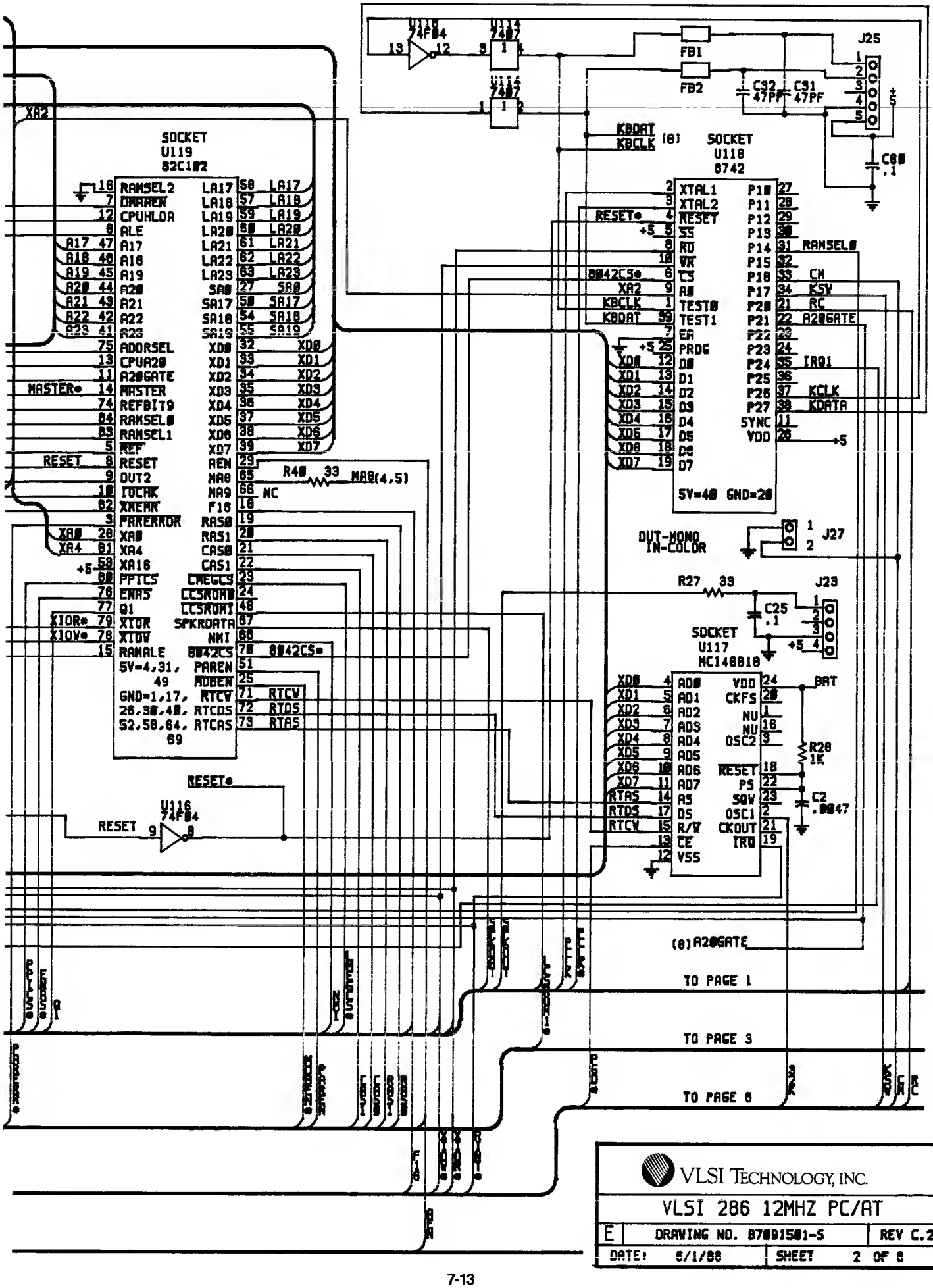
NOTES:

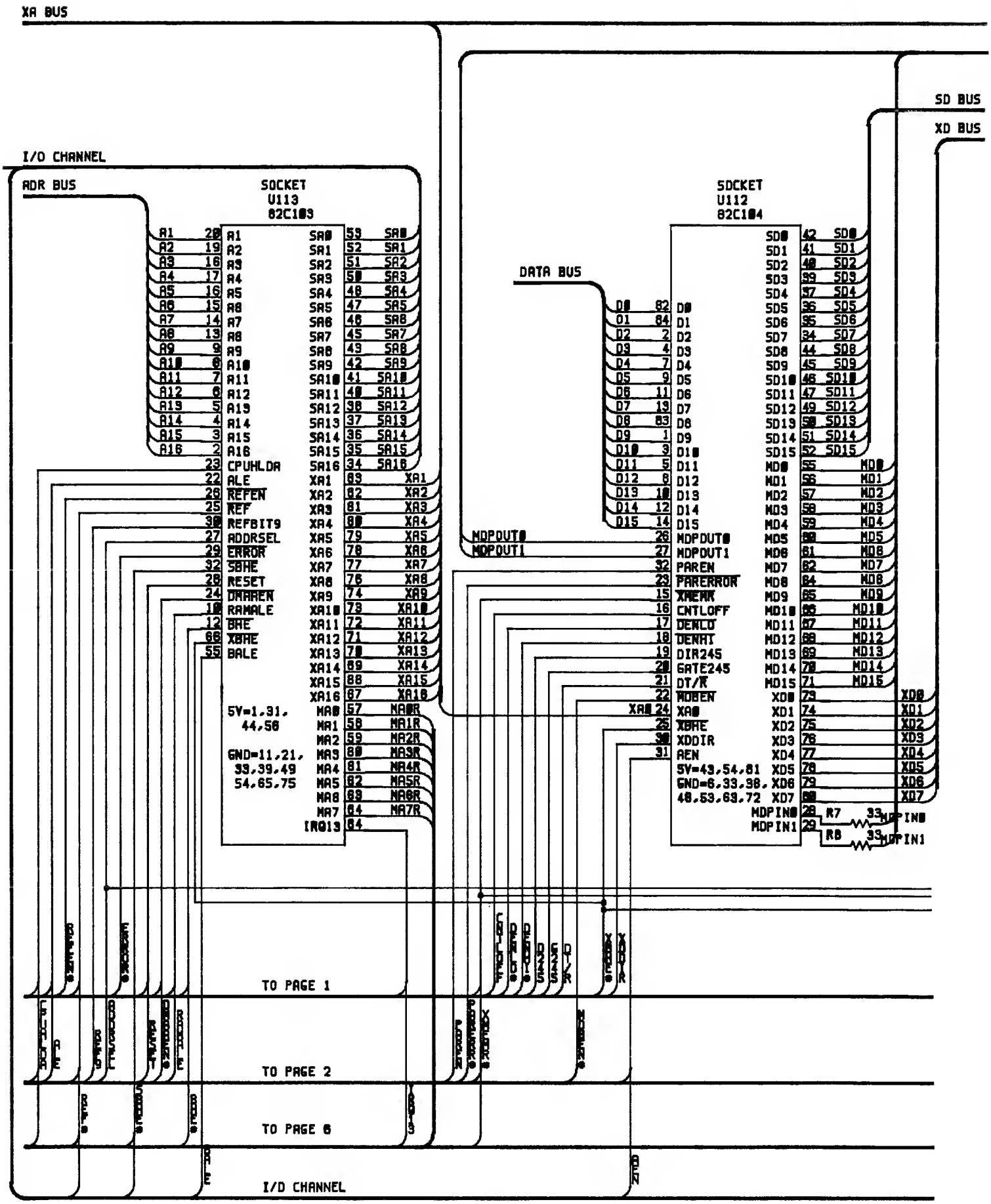
12 MHz PC/AT-COMPATIBLE SCHEMATICS

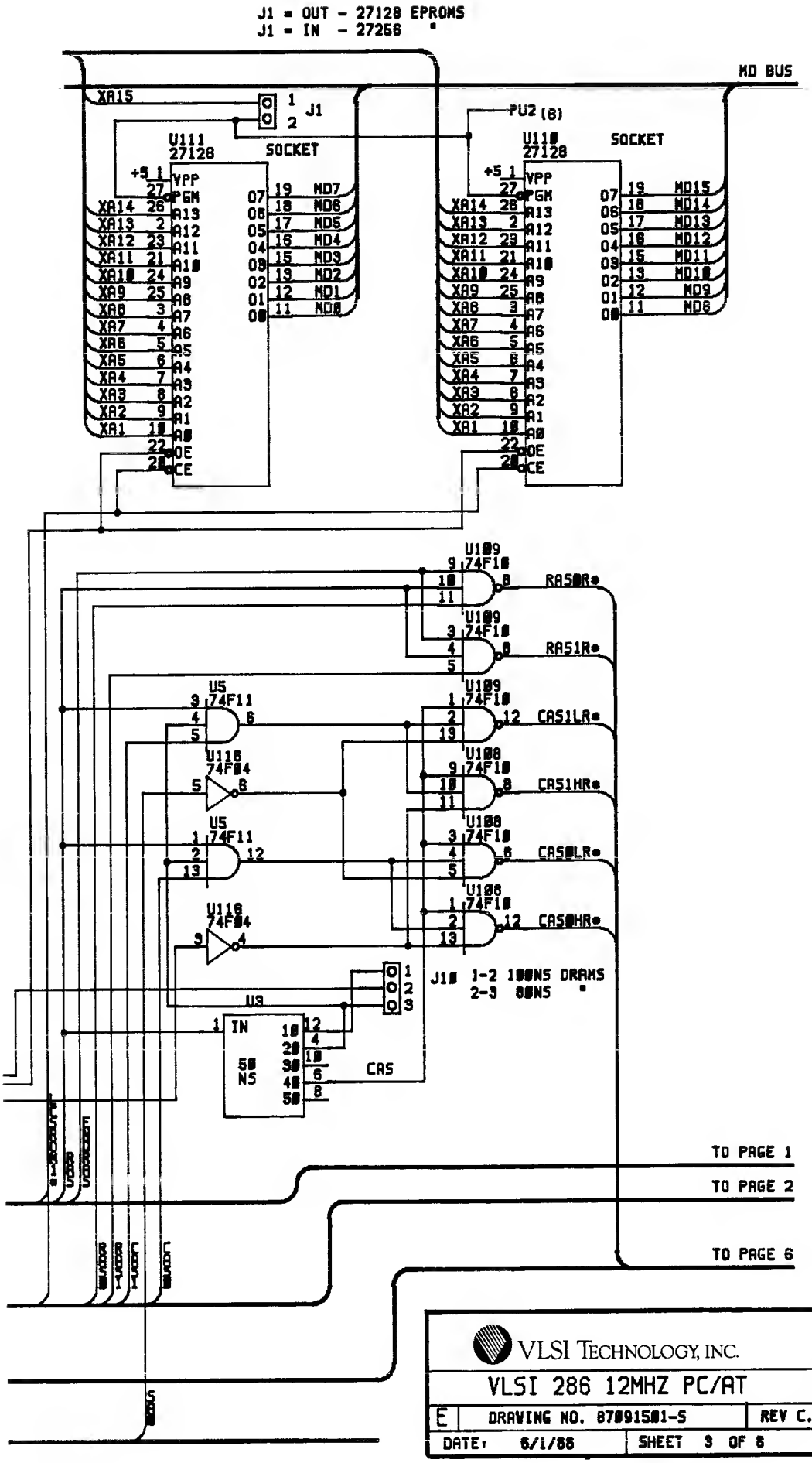

ADR BUS
XA BUS
SOCKET
U126
80287
PROCLK 32
RES287 35
READY* 40
XIOR* 27
XIOW* 28
NPCS* 34
XA4 33
XA1 29
XA2 31
S0* 2
S1* 1
COD/INTA* 3
PEACK* 36
PRDCLK 37
CPUHLDA 38
39
CLK
RESET
READY
NPRD
NPWR
NPS1
NPS2
CMD0
CMD1
S0
S1
CODINTA
PEACK
CLK286
HLDA
CKM
5V=9
GND=10,30
PEREQ 24
ERROR 26
BUSY 25
D0 23
D1 22
D2 21
D3 20
D4 19
D5 18
D6 17
D7 16
D8 15
D9 14
D10 12
D11 11
D12 8
D13 7
D14 6
D15 5
PEREQ
ERROR*
BUSY*
SOCKET
U125
80288
PROCLK 31
RESCPU 29
READY* 69
CPUHRQ 64
NMI 59
PEREQ 61
E1* 55
BUSY* 54
INTR 57
52
CLK
RESET
READY
HOLD
NMI
PEREQ
ERROR
BUSY
INTR
CAP
S0
S1
M/IO
COD/INTA
HLDA
PEACK
BHE
LOCK
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
5 S0*
4 S1*
67 M/IO*
66
65
8 PEACK*
1 BHE*
66 N/C
34 A0
33 A1
32 A2
28 A3
27 A4
26 A5
25 A6
24 A7
23 A8
22 A9
21 A10
20 A11
19 A12
18 A13
17 A14
16 A15
15 A16
14 A17
13 A18
12 A19
11 CA20
10 A21
9 A22
7 A23
C93
0.047
5V=30,62
GND=9,35,60
D0 36
D1 38
D2 40
D3 42
D4 44
D5 46
D6 48
D7 50
D8 37
D9 39
D10 41
D11 43
D12 45
D13 47
D14 49
D15 51
J30
1
2
OUT=NORMAL
IN =FAST
MODE
U4
74LS00
4
5
6
U4
74LS00
1
2
3
RESET*
TO PAGE 2
DATA BUS
TO PAGE 3
TO PAGE 4
TO PAGE 5
TO PAGE 6
READY* (8)
I/O CHANNEL

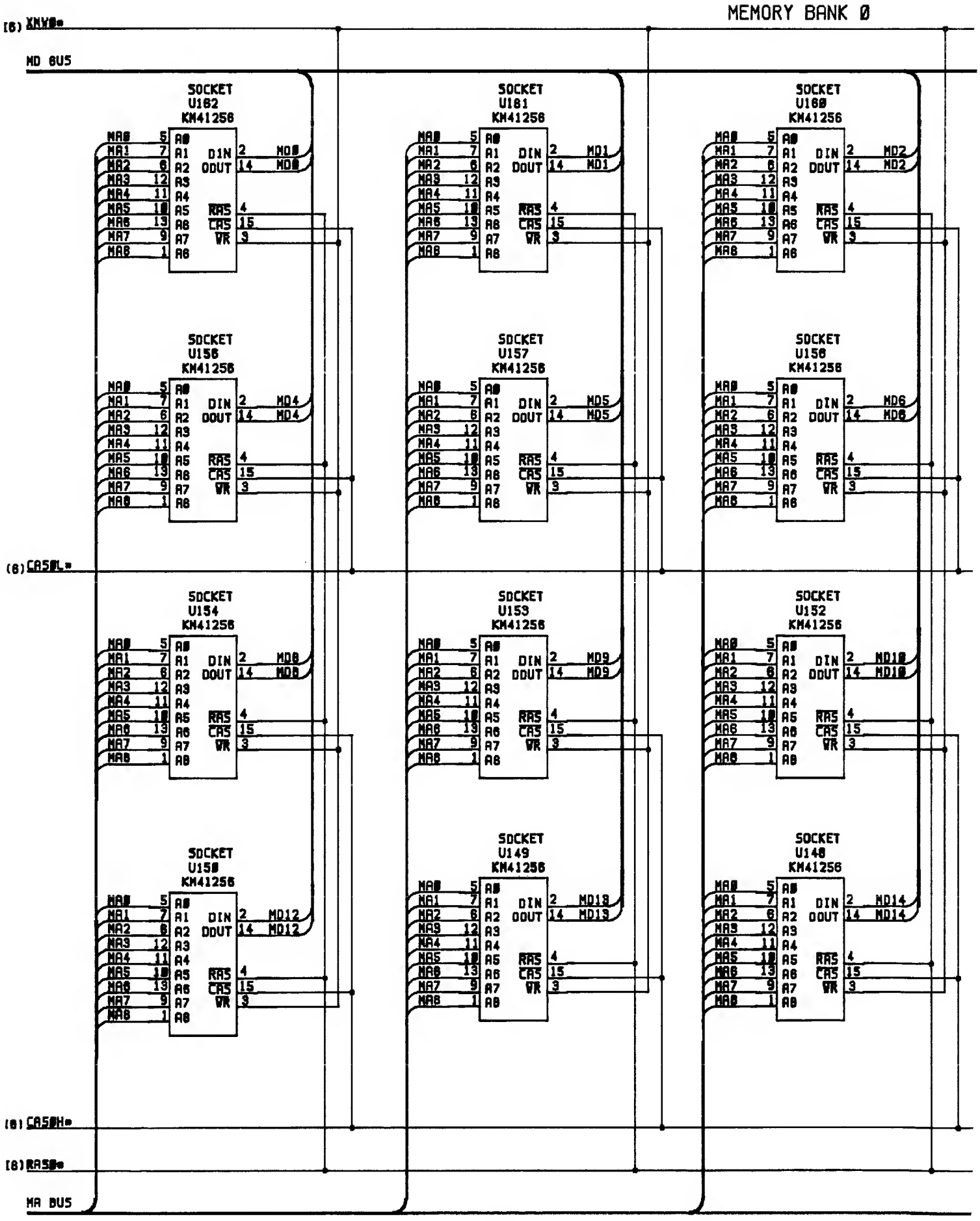

C36
30PF
C34
18PF
U121
14.3181MHZ
U123
74ALS244
(2) SPKDAT
SPKOUT (2)
OSC
CLK
RSTDRV
XMEMW#
XMW1R#
XMW0R#
(8)
SYSCLK
U124 82C101 SOCKET
(6) PWRGD
(2,8) RC
N/C
POWERGOOD
VSW
RC
XTAL1-1
XTAL1-2
XTAL2-1
XTAL2-2
SW
SI
M/IO
A0
A1
XBHE
IOCHRDY
F16
IOCS16
AEN1
AEN2
MEMCS16
LMEGCS
CPUHLDA
MASTER
XA0
XA3
XA5
XA6
XA7
XA8
XA9
FASTMODE
ROMWTST
RAMWTST
REF
5V=32,54, 82
GND=1,19, 27,38,43, 48,59,67
RESCPU
RESET
PROCLK
SYSCLK
PCLK
PCLK
OSC
MHZ119
ENA5
DT/R
CNTLOFF
DENLO
DENHI
READY
ALE
RAS
ENDRAS
RAMALE
ROMCS
IOR
IOW
MEMR
MEMW
INTA
SMEMR
SMEMW
XMEMR
XMEMW
XIOR
XIOW
XDDIR
REFEN
DIR245
GATE245
NPCS
RES287
PPICS
DMAAEN
SA0
J32
J31
J32 - IN=2 W/S ROM, OUT=1 W/S ROM
J31 - IN=0 W/S RAM, OUT=1 W/S RAM
RESET
PCLK
PCLK#
OSC#
MHZ119
ENA5#
DT/R
CNTLOFF
DENLO#
DENHI#
ALE
RAS
ENDRAS
LCSROM1#
IOR#
IOW#
MEMR#
MEMW#
SMEMR#
SMEMW#
XDDIR
REFEN#
D245
G245
PPICS#
DMAAEN#
SA0
TO PAGE 2
TO PAGE 3
TO PAGE 4
TO PAGE 5
TO PAGE 6
VLSI TECHNOLOGY, INC.
VLSI 286 12MHZ PC/AT
E
DRAWING NO. 87091501-5
REV C.2
DATE: 8/1/88
SHEET 1 OF 8

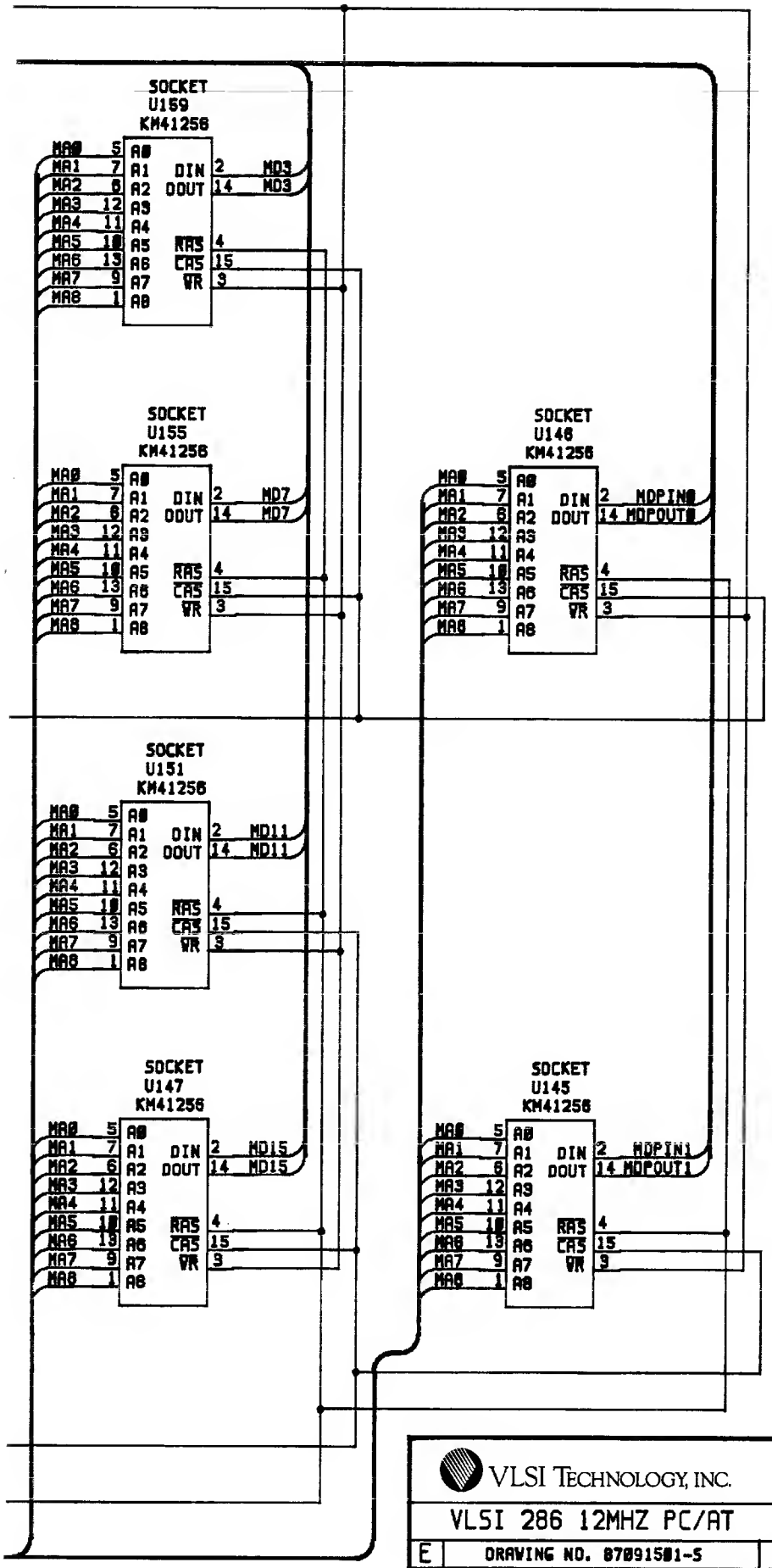

XA BUS
XD BUS
ADR BUS
I/O CHANNEL
SOCKET
U128
82C188
J28 J29 DRAM
IN IN - 1B 256K
OUT IN - 1B 256K & 1B 64K
IN OUT - 3B 256K
OUT OUT - 1B 1MB (NOT USED)
J29
J28
DRQ0 21
DRQ1 20
DRQ2 19
DRQ3 18
DRQ5 17
DRQ6 16
DRQ7 15
IRQ1 14
IRQ3 13
IRQ4 12
IRQ5 11
IRQ6 10
IRQ7 9
IRQ8 81
IRQ9 80
IRQ10 79
IRQ11 78
IRQ12 77
IRQ13 76
IRQ14 75
IRQ15 74
INTA' 0
CPUHRQ 48
MASTER 45
IOCHRDY 73
SYSCLK 23
MHZ119 41
RESET 24
XD0 34
XD1 33
XD2 32
XD3 31
XD4 30
XD5 29
XD6 28
XD7 27
5V=5,43
GND=22,26,
59,87
DRQ0
DRQ1
DRQ2
DRQ3
DRQ5
DRQ6
DRQ7
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
INTA'
CPUHRQ
MASTER
IOCHRDY
SYSCLK
MHZ119
RESET
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
DACK0
DACK1
DACK2
DACK3
DACK5
DACK6
DACK7
T/C
AENT
AEN2
CPUHLDA
INTR
A17
A18
A19
A20
A21
A22
A23
REF
XIOR
XIOW
XMEMR
XMEMW
OUT2
XA0
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XA8
XA9
XA10
XA11
XA12
XA13
XA14
XA15
XA16
1 DACK0*
65 DACK1*
64 DACK2*
62 DACK3*
2 DACK5*
3 DACK6*
4 DACK7*
59 T/C
8
7
44
46
72 A17
71 A18
70 A19
69 A20
68 A21
66 A22
65 A23
25
36
37
35
36
42
47 XA0
48 XA1
49 XA2
50 XA3
51 XA4
52 XA5
53 XA6
54 XA7
55 XA8
56 XA9
57 XA10
58 XA11
60 XA12
61 XA13
62 XA14
63 XA15
64 XA16
U116
74F04
IRQ11
11RINT*
TO PAGE 1
TO PAGE 3
TO PAGE 8
I/O
CHANNEL


SOCKET
U119
82C182
SOCKET
U118
8742
SOCKET
U117
MC146818
J25
J27
J29
FB1
FB2
C32 47PF
C31 47PF
C88 .1
C25 .1
C2 .0047
R48 33
R27 33
R28 1K
XA2
KBDAT
KBCLK
RESET
RESET•
MASTER•
XIOR•
XIOW•
RAMSEL#
A20GATE
IRQ1
KCLK
KDATA
BAT
+5
OUT-MONO
IN-COLOR
(8)A20GATE
TO PAGE 1
TO PAGE 3
TO PAGE 8
VLSI TECHNOLOGY, INC.
VLSI 286 12MHZ PC/AT
DRAWING NO. 87#91581-5
REV C.2
DATE: 5/1/88
SHEET 2 OF 8


XA BUS
SD BUS
XD BUS
I/O CHANNEL
ADR BUS
SOCKET
U113
82C103
DATA BUS
SOCKET
U112
82C104
5V=1,31,
44,56
GND=11,21,
33,39,49
54,65,75
5V=43,54,81
GND=6,33,38,
48,53,69,72
R7
R8
33
33
TO PAGE 1
TO PAGE 2
TO PAGE 6
I/O CHANNEL


J1 = OUT - 27128 EPROMS
J1 = IN - 27256
MD BUS
XA15
J1
U111
27128
SOCKET
U110
27128
SOCKET
PU2 (8)
VPP
PGM
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
OE
CE
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MD15
MD14
MD13
MD12
MD11
MD10
MD9
MD8
U109
74F10
RAS0R*
RAS1R*
U5
74F11
U116
74F04
CAS1LR*
CAS1HR*
CAS0LR*
CAS0HR*
J10 1-2 100NS DRAMS
2-3 80NS
U3
IN
50
NS
CAS
TO PAGE 1
TO PAGE 2
TO PAGE 6
VLSI TECHNOLOGY, INC.
VLSI 286 12MHZ PC/AT
E
DRAWING NO. 87091501-5
REV C.2
DATE: 6/1/88
SHEET 3 OF 8


MEMORY BANK Ø
(6) XNXØ*
MD BUS
SOCKET U162 KM41256
SOCKET U161 KM41256
SOCKET U160 KM41256
SOCKET U156 KM41256
SOCKET U157 KM41256
SOCKET U158 KM41256
(6) CASØL*
SOCKET U154 KM41256
SOCKET U153 KM41256
SOCKET U152 KM41256
SOCKET U150 KM41256
SOCKET U149 KM41256
SOCKET U148 KM41256
(8) CASØH*
(8) RASØ*
MA BUS
DIN
DOUT
RAS
CAS
WR

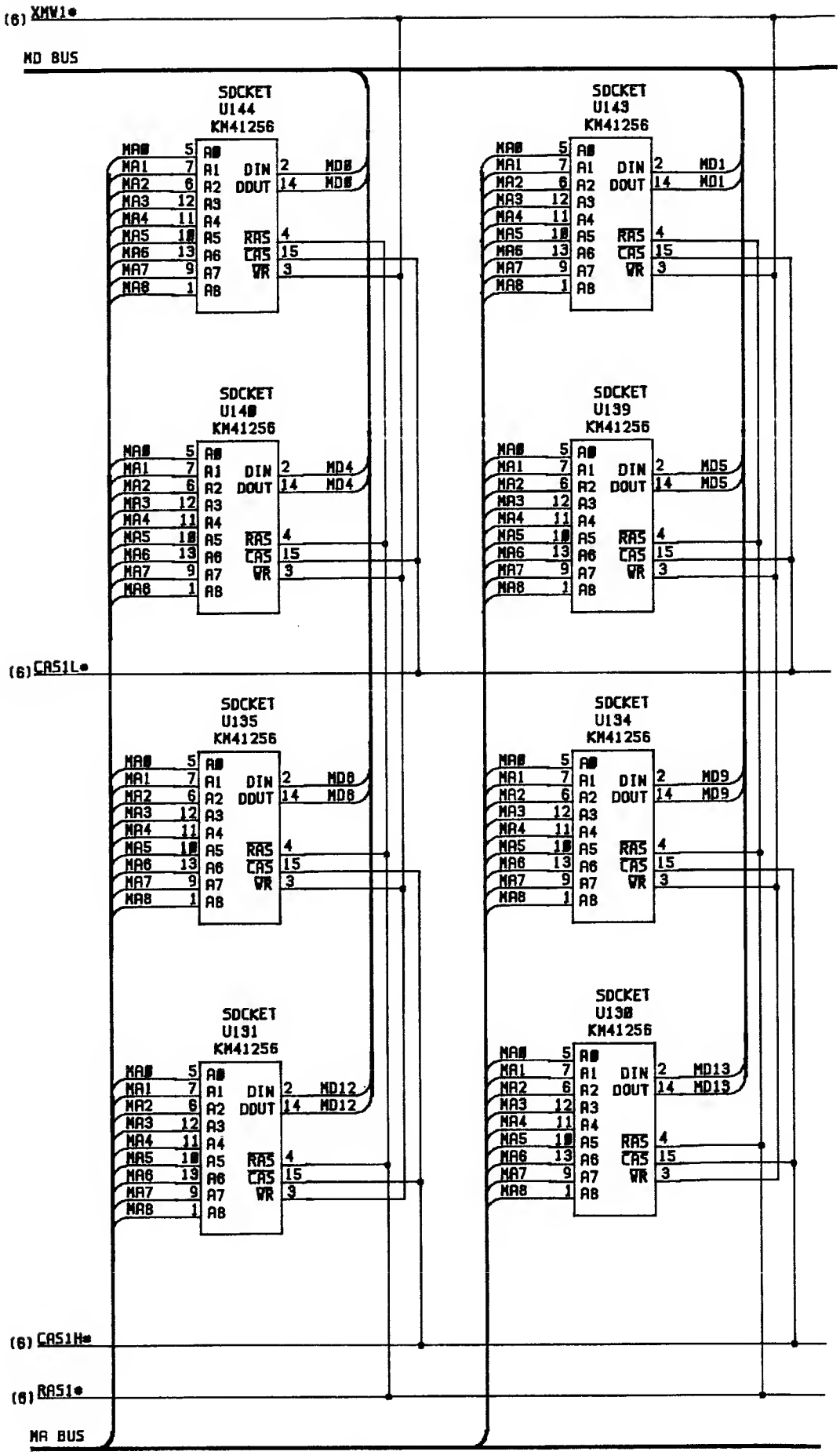


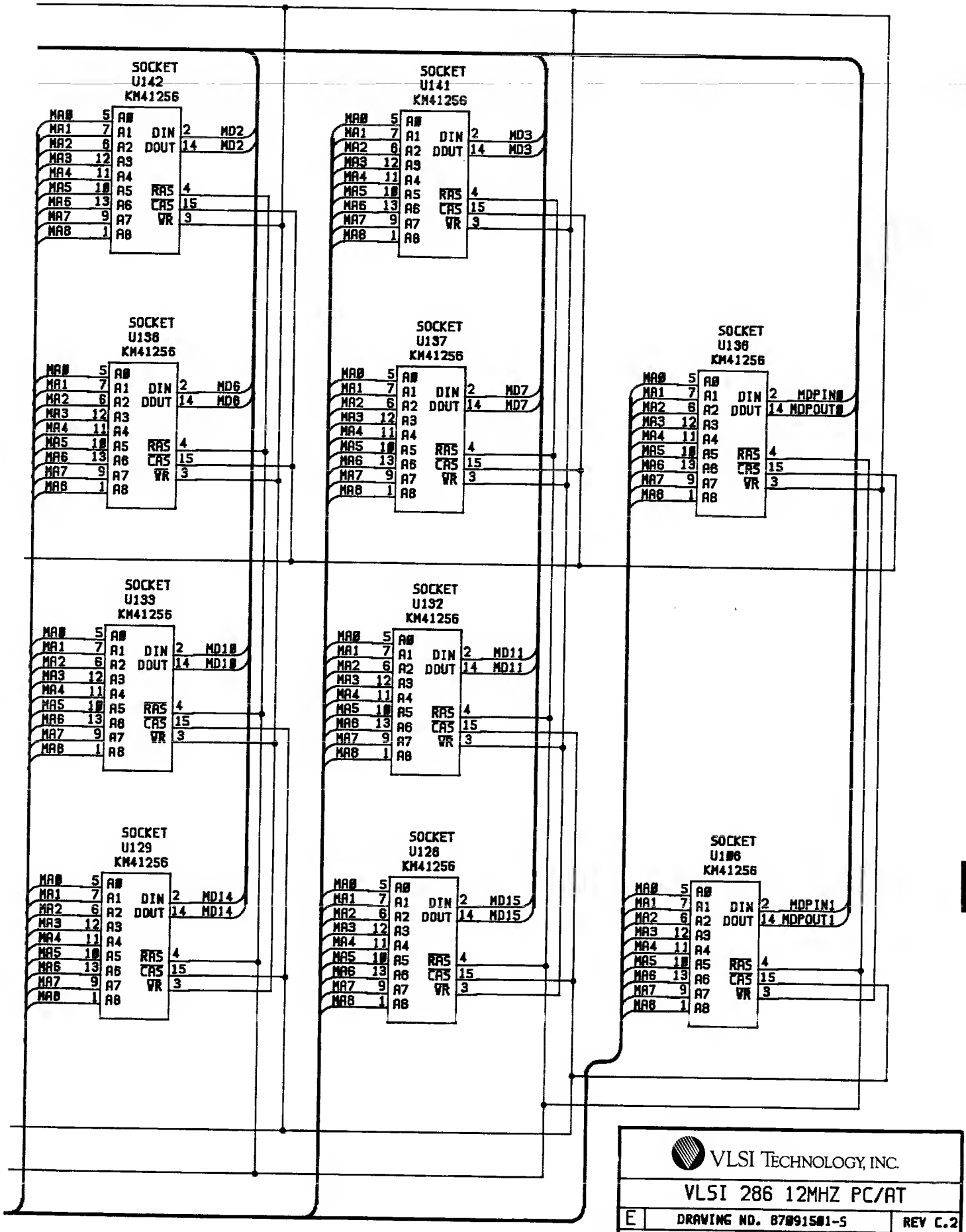
VLSI TECHNOLOGY, INC.

VLSI 286 12MHZ PC/AT

E	DRAWING NO. 870915B1-5	REV C.2
DATE: 6/1/88	SHEET 4 OF 8	

7


(6) XMV1*
MD BUS
SOCKET U144 KM41256
SOCKET U143 KM41256
SOCKET U140 KM41256
SOCKET U139 KM41256
(6) CAS1L*
SOCKET U135 KM41256
SOCKET U134 KM41256
SOCKET U131 KM41256
SOCKET U130 KM41256
(6) CAS1H*
(6) RAS1*
MA BUS
MA0 5
MA1 7
MA2 6
MA3 12
MA4 11
MA5 10
MA6 13
MA7 9
MA8 1
A0
A1
A2
A3
A4
A5
A6
A7
A8
DIN
DOUT
RAS
CAS
WR
2
14
4
15
3
MD0
MD1
MD4
MD5
MD8
MD9
MD12
MD13

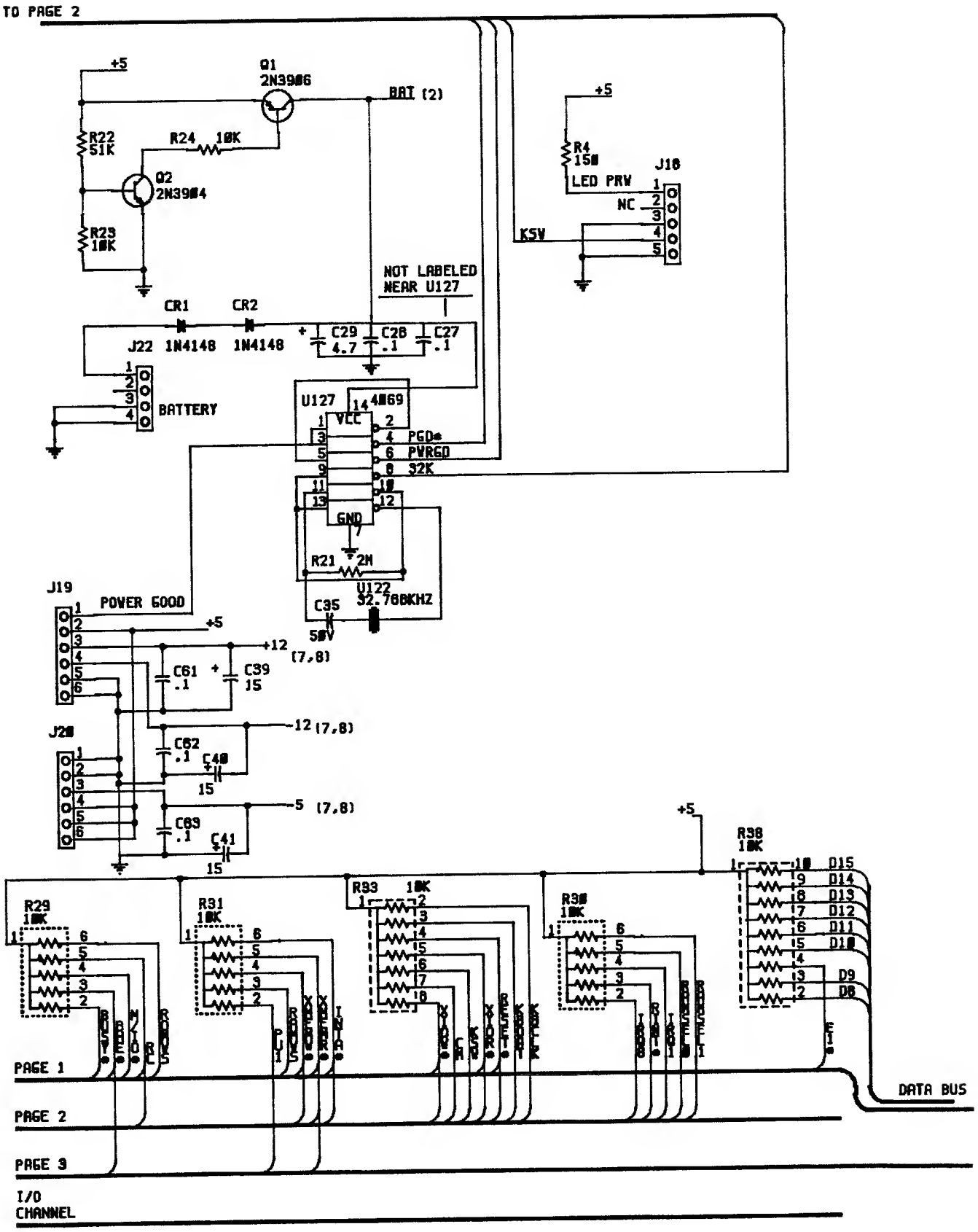


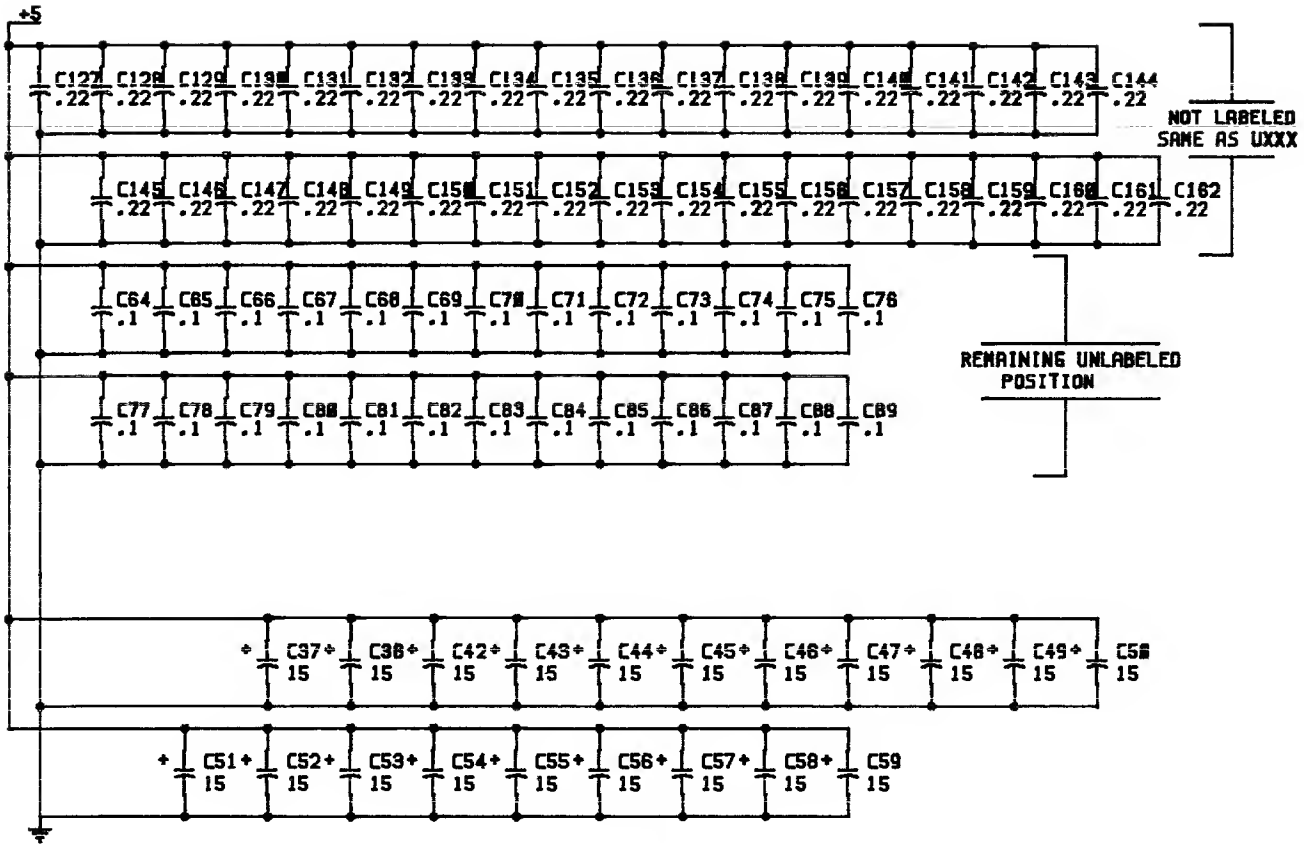
VLSI TECHNOLOGY, INC.

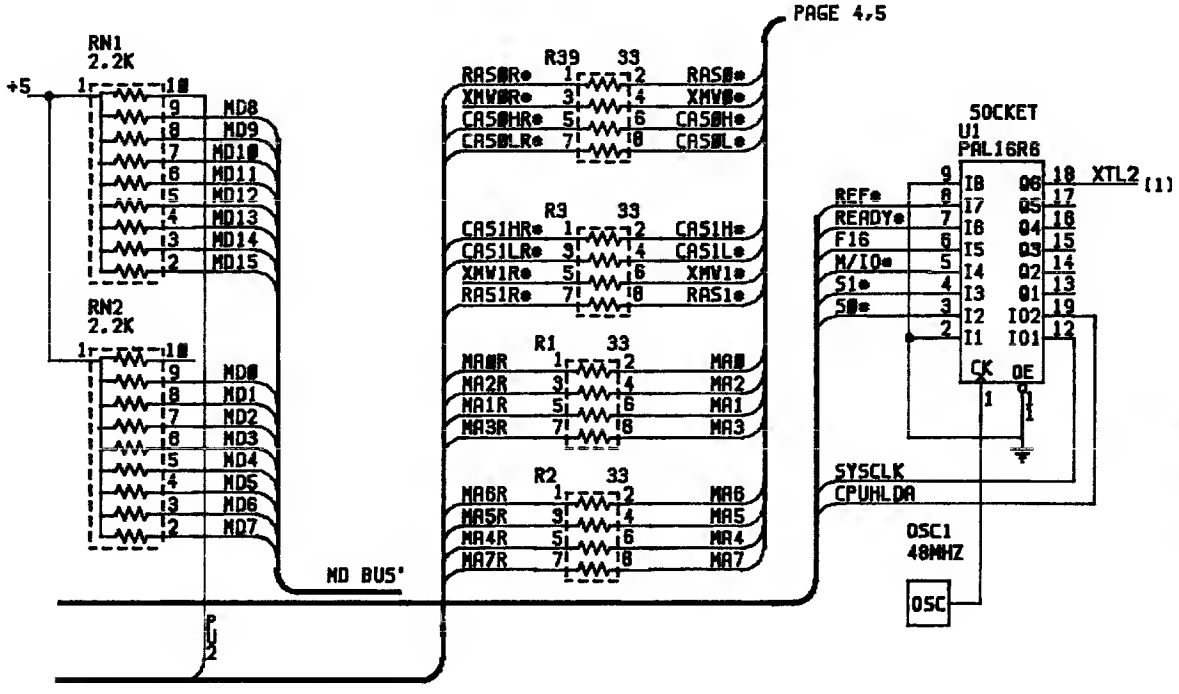
VLSI 286 12MHZ PC/AT

E	DRAWING NO. 87091501-5	REV C.2
DATE: 6/1/88	SHEET 5 OF 8	

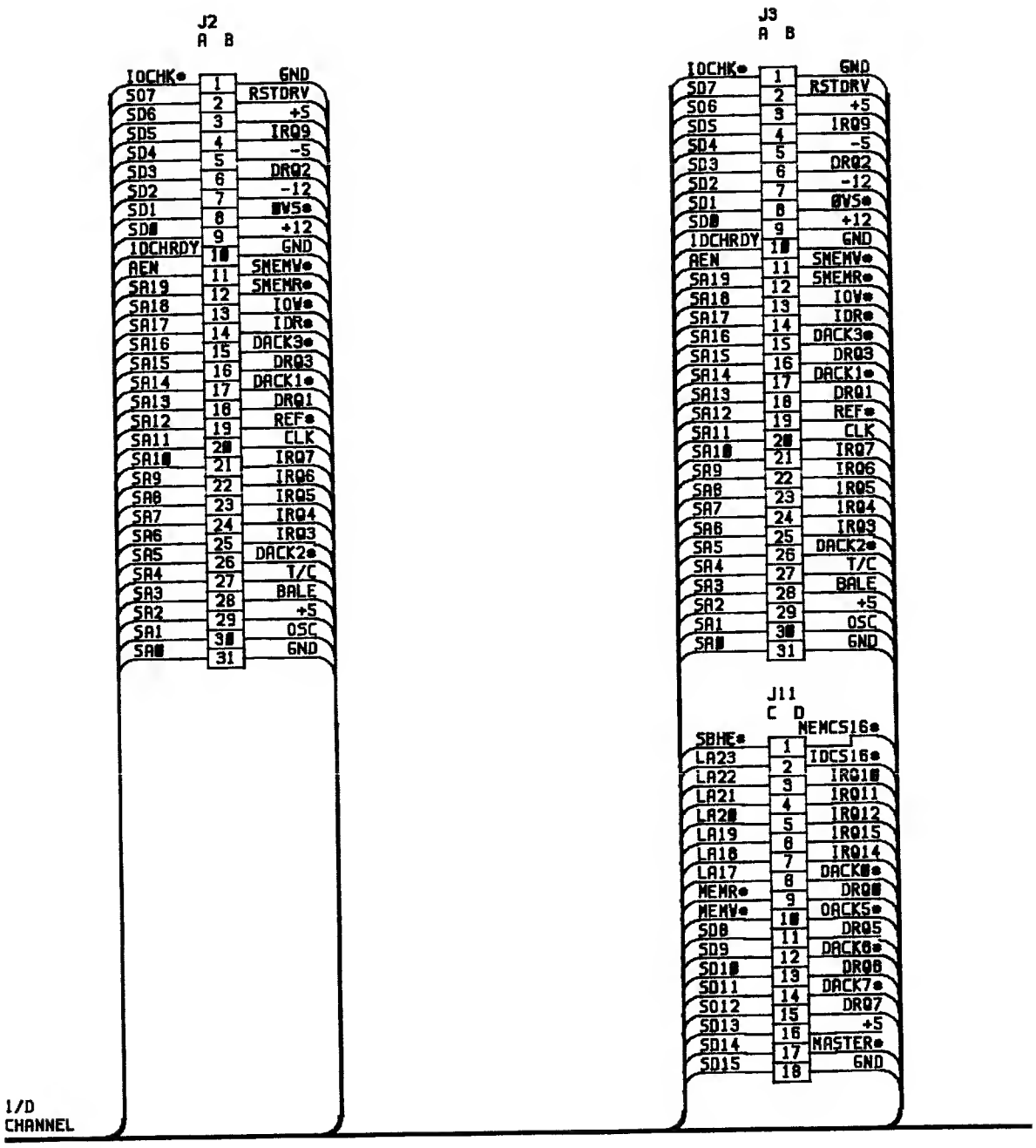
7

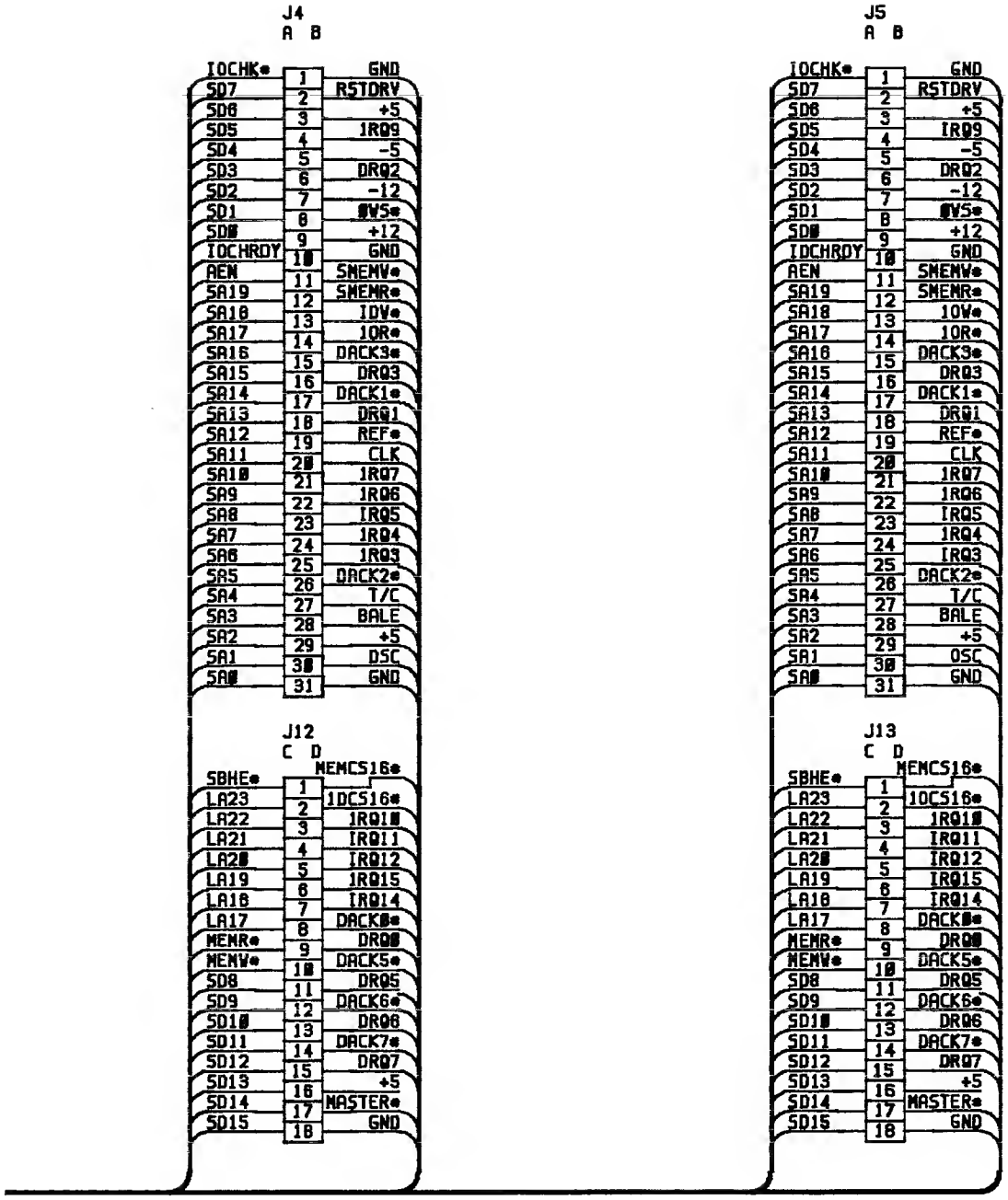

TO PAGE 2
+5
Q1
2N3906
BAT (2)
R22
51K
R24 10K
Q2
2N3904
R23
10K
+5
R4
150
LED PRV
J18
NC
K5V
NOT LABELED
NEAR U127
CR1
CR2
J22 1N4148 1N4148
C29
4.7
C28
.1
C27
.1
BATTERY
U127
4069
VCC
PGD
PVRGD
32K
GND
R21 2M
U122
32.768KHZ
C35
50V
J19
POWER GOOD
+5
+12 (7,8)
C61
.1
C39
15
J20
12 (7,8)
C62
.1
C40
15
5 (7,8)
C63
.1
C41
15
+5
R38
10K
R29
10K
R31
10K
R33 10K
R36
10K
D15
D14
D13
D12
D11
D10
D9
D8
PAGE 1
PAGE 2
PAGE 3
I/O
CHANNEL
DATA BUS





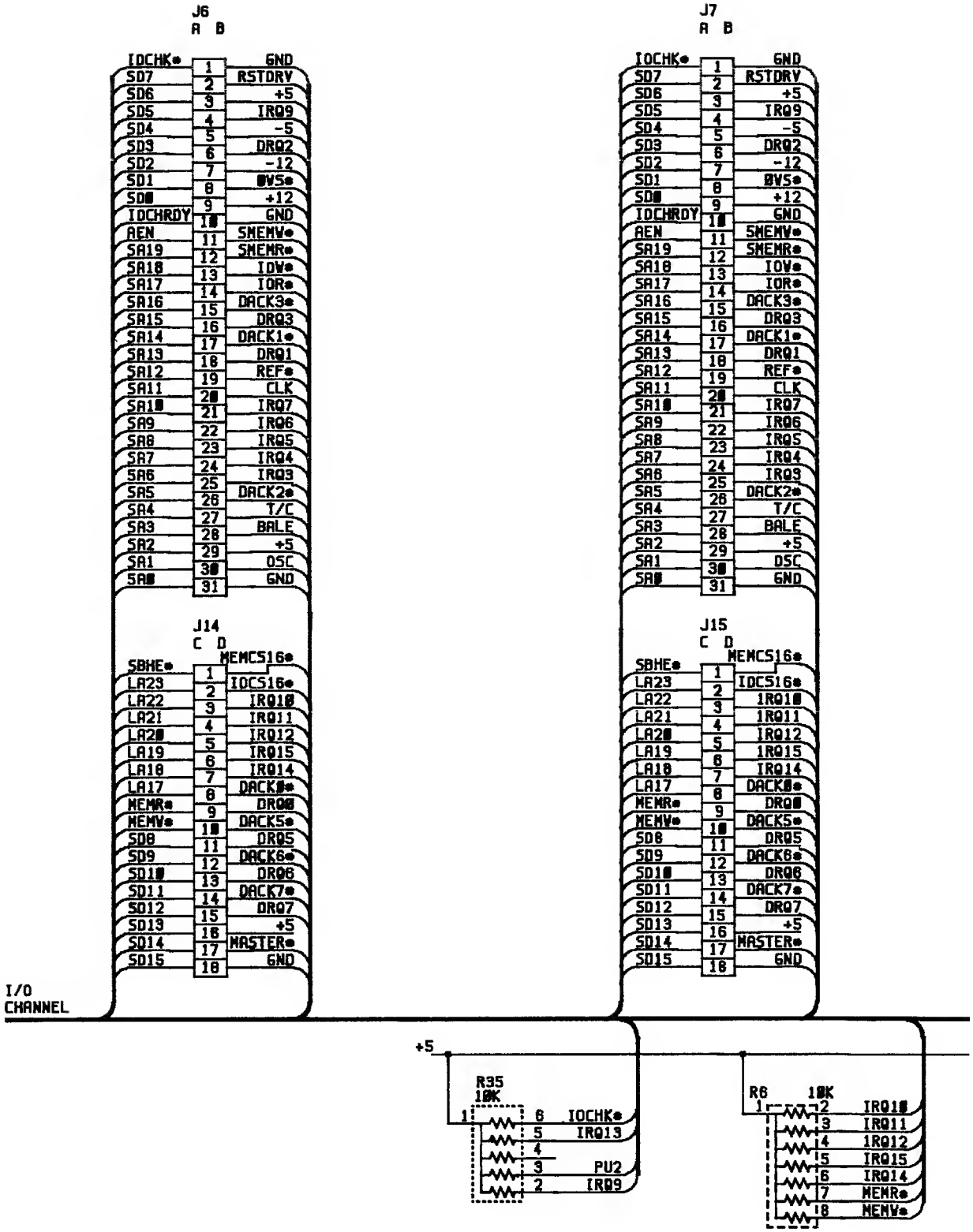
VLSI TECHNOLOGY, INC.		
VLSI 286 12MHZ PC/AT		
E	DRAWING NO. 870915#1-S	REV C.2
DATE: 6/1/88	SHEET 6 OF 6	

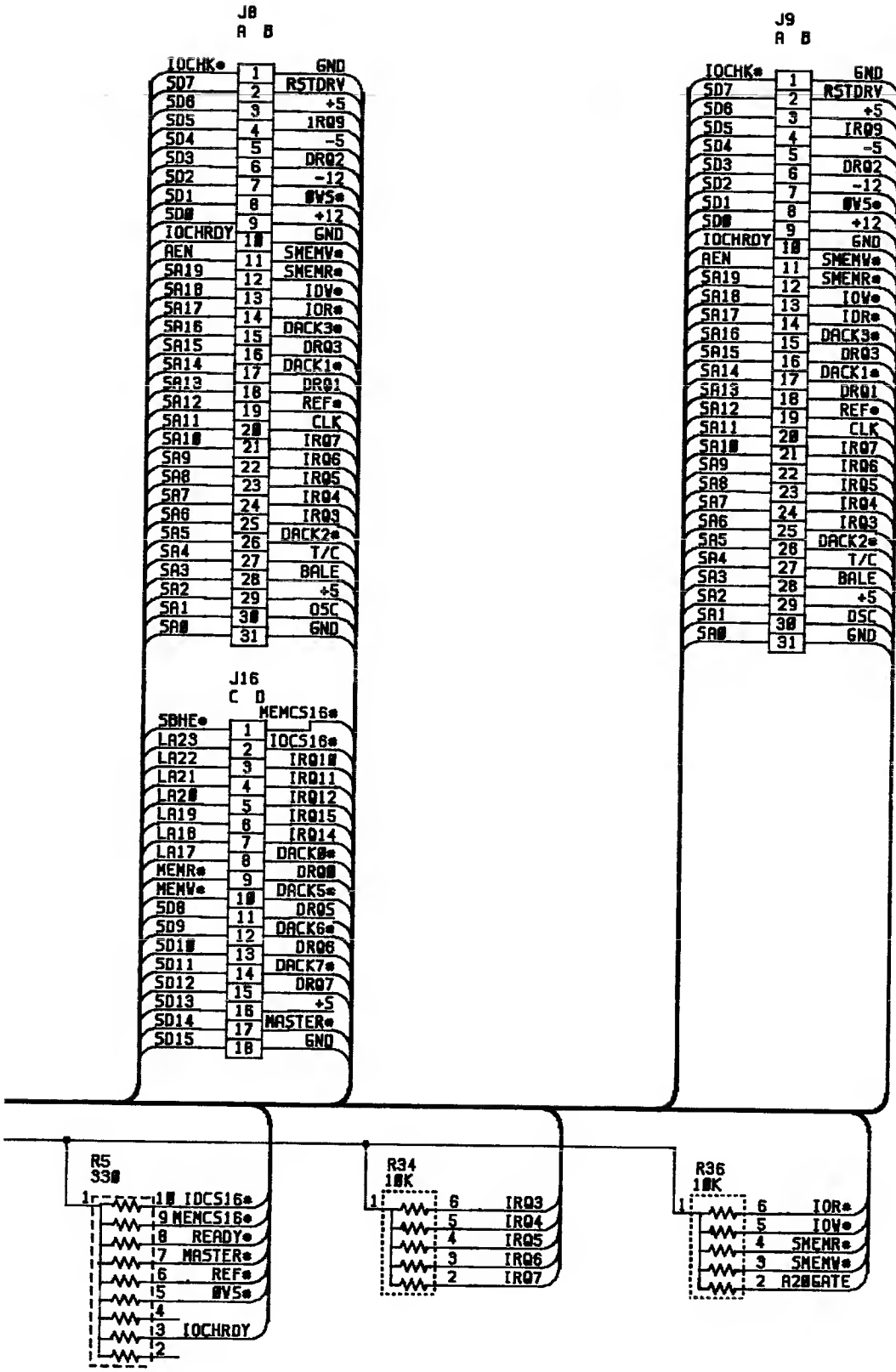

J2
A B
IOCHK• 1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 ØV5•
SD0 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW•
SA19 12 SMEMR•
SA18 13 IOW•
SA17 14 IOR•
SA16 15 DACK3•
SA15 16 DRQ3
SA14 17 DACK1•
SA13 18 DRQ1
SA12 19 REF•
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2•
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SA0 31 GND
J3
A B
IOCHK• 1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 ØV5•
SD0 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW•
SA19 12 SMEMR•
SA18 13 IOW•
SA17 14 IOR•
SA16 15 DACK3•
SA15 16 DRQ3
SA14 17 DACK1•
SA13 18 DRQ1
SA12 19 REF•
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2•
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SA0 31 GND
J11
C D
SBHE• 1 MEMCS16•
LA23 2 IOCS16•
LA22 3 IRQ10
LA21 4 IRQ11
LA20 5 IRQ12
LA19 6 IRQ15
LA18 7 IRQ14
LA17 8 DACK0•
MEMR• 9 DRQ0
MEMW• 10 DACK5•
SD8 11 DRQ5
SD9 12 DACK6•
SD10 13 DRQ6
SD11 14 DACK7•
SD12 15 DRQ7
SD13 16 +5
SD14 17 MASTER•
SD15 18 GND
I/O
CHANNEL



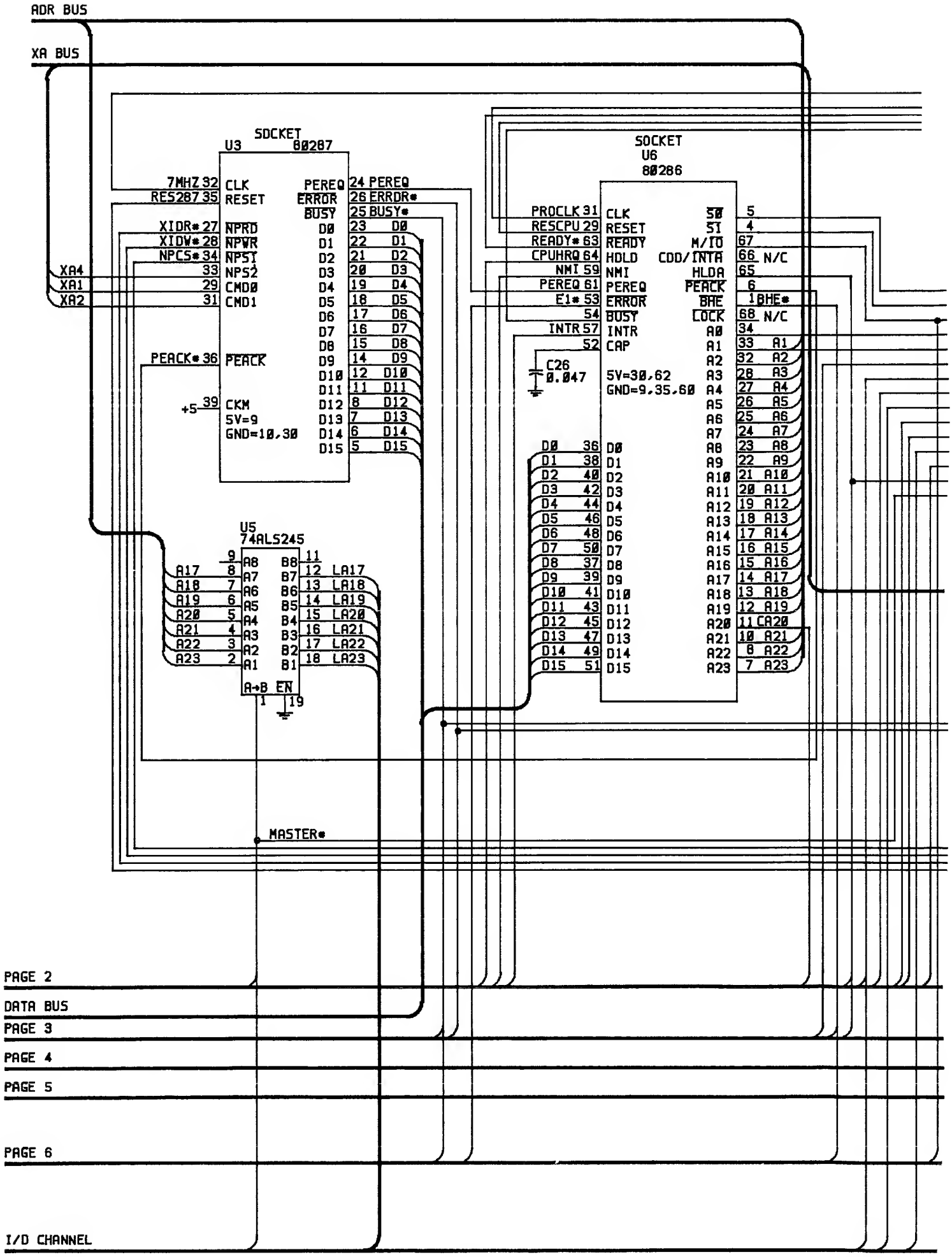
7

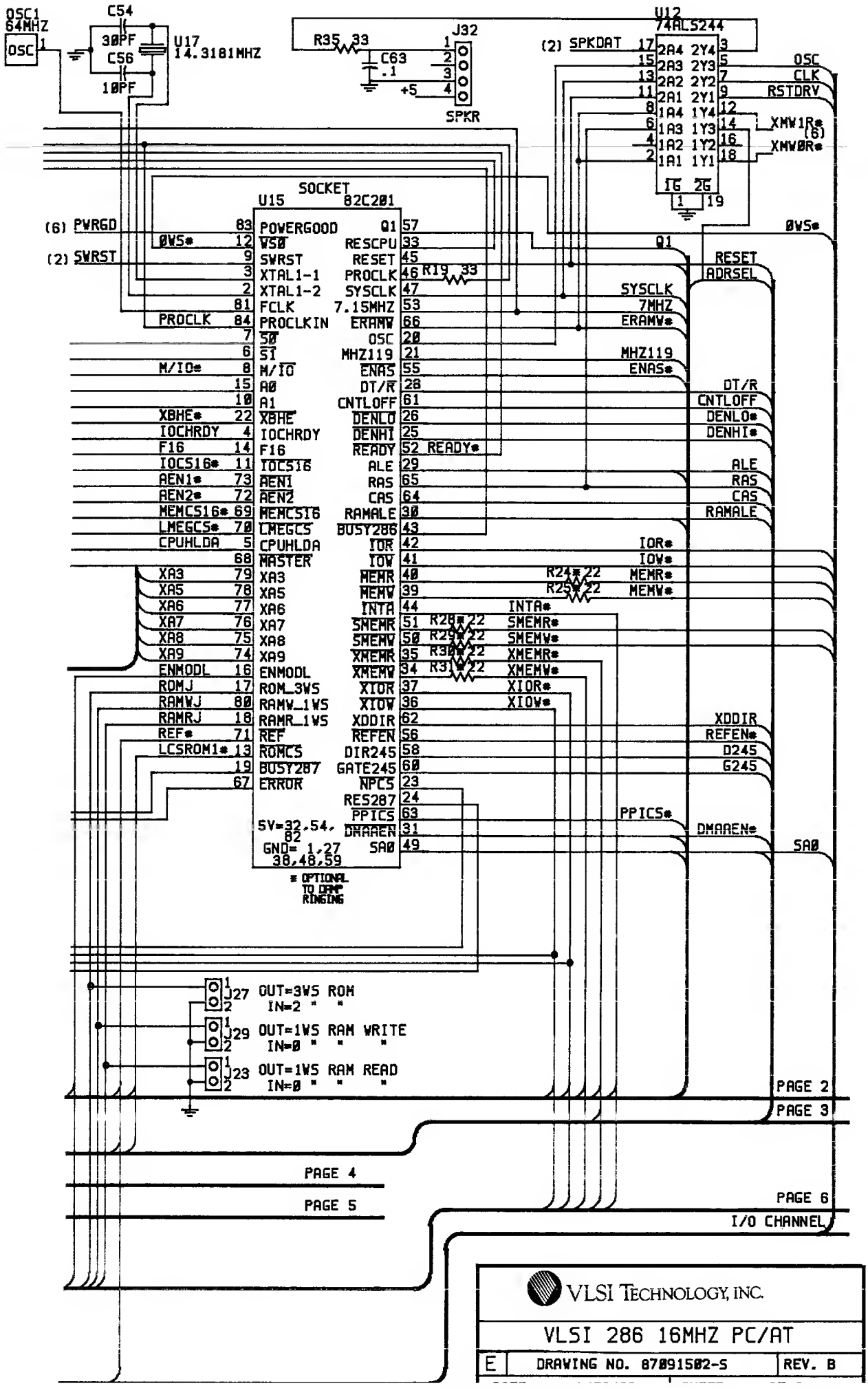
VLSI TECHNOLOGY, INC.		
VLSI 286 12MHZ PC/AT		
E	DRAWING NO. 87#915#1-5	REV C.2
DATE: 6/1/88	SHEET 7 OF 8	

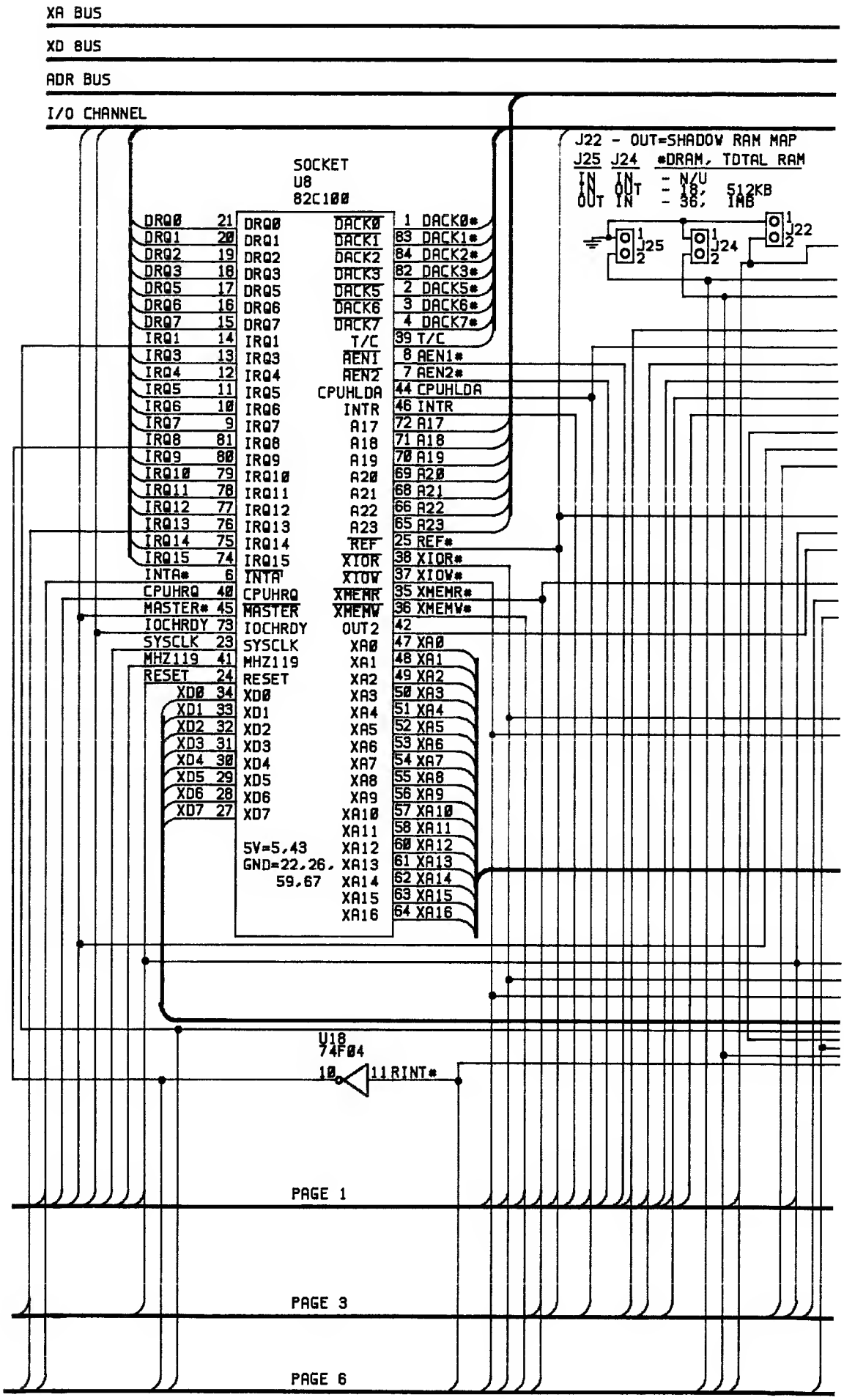

J6
A B
IOCHK* 1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 0WS*
SD0 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW*
SA19 12 SMEMR*
SA18 13 IOW*
SA17 14 IOR*
SA16 15 DACK3*
SA15 16 DRQ3
SA14 17 DACK1*
SA13 18 DRQ1
SA12 19 REF*
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2*
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SA0 31 GND
J14
C D
SBHE* MEMCS16*
LA23 1 IOCS16*
LA22 2 IRQ10
LA21 3 IRQ11
LA20 4 IRQ12
LA19 5 IRQ15
LA18 6 IRQ14
LA17 7 DACK0*
MEMR* 8 DRQ0
MEMW* 9 DACK5*
SD8 10 DRQ5
SD9 11 DACK6*
SD10 12 DRQ6
SD11 13 DACK7*
SD12 14 DRQ7
SD13 15 +5
SD14 16 MASTER*
SD15 17 GND
18
I/O
CHANNEL
J7
A B
IOCHK* 1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 0WS*
SD0 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW*
SA19 12 SMEMR*
SA18 13 IOW*
SA17 14 IOR*
SA16 15 DACK3*
SA15 16 DRQ3
SA14 17 DACK1*
SA13 18 DRQ1
SA12 19 REF*
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2*
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SA0 31 GND
J15
C D
SBHE* MEMCS16*
LA23 1 IOCS16*
LA22 2 IRQ10
LA21 3 IRQ11
LA20 4 IRQ12
LA19 5 IRQ15
LA18 6 IRQ14
LA17 7 DACK0*
MEMR* 8 DRQ0
MEMW* 9 DACK5*
SD8 10 DRQ5
SD9 11 DACK6*
SD10 12 DRQ6
SD11 13 DACK7*
SD12 14 DRQ7
SD13 15 +5
SD14 16 MASTER*
SD15 17 GND
18
+5
R35
10K
1 6 IOCHK*
5 IRQ13
4
3 PU2
2 IRQ9
R6 10K
1 2 IRQ10
3 IRQ11
4 IRQ12
5 IRQ15
6 IRQ14
7 MEMR*
8 MEMW*

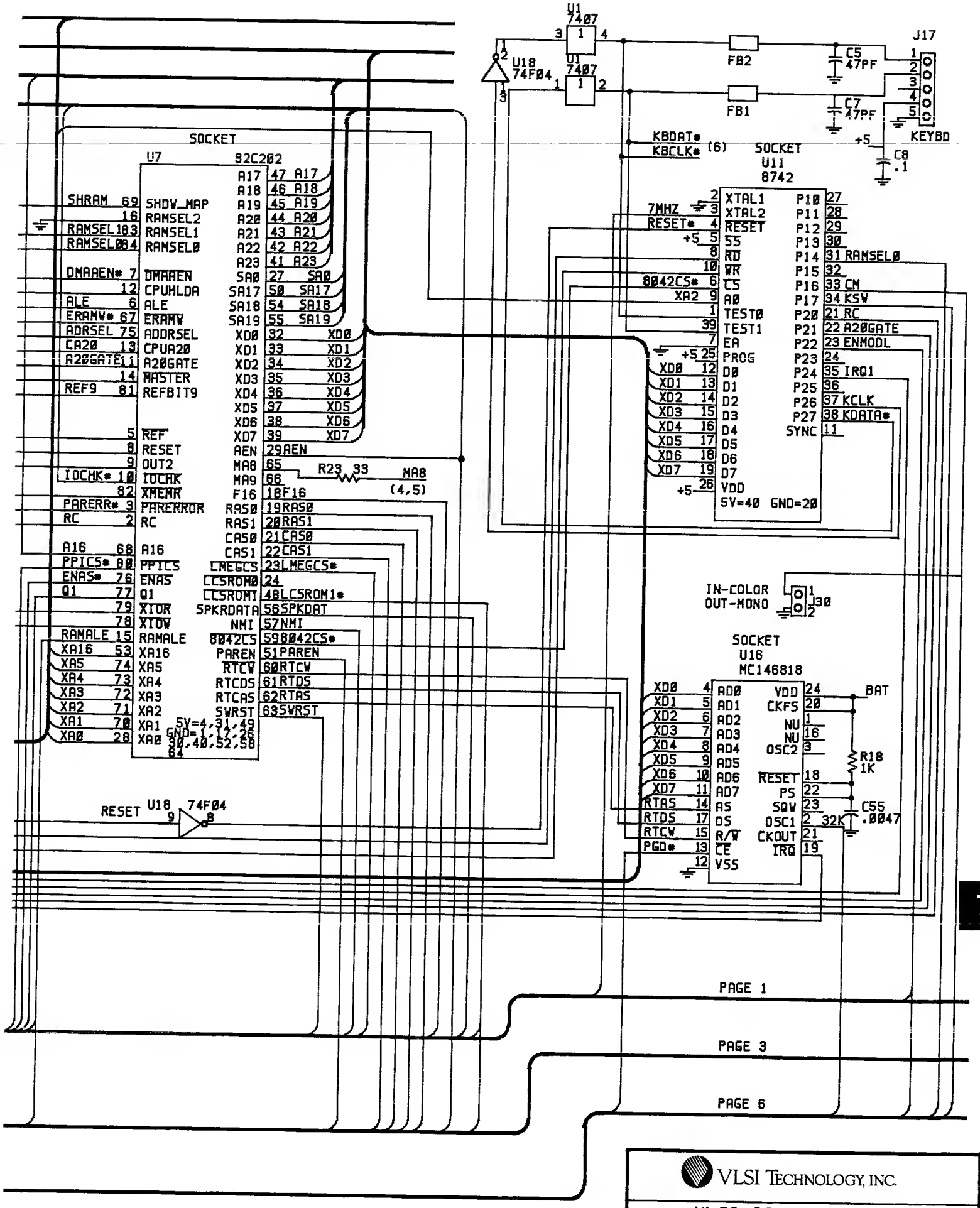


VLSI TECHNOLOGY, INC.		
VLSI 286 12MHZ PC/AT		
E	DRAWING NO. 87#9150I-5	REV C.2
DATE: 6/1/88	SHEET 8 OF 8	


ADR BUS
XA BUS
SOCKET
U3
80287
7MHZ 32 CLK
RES287 35 RESET
XIOR* 27 NPRD
XIOW* 28 NPWR
NPCS* 34 NPSI
33 NPS2
XA4
29 CMD0
XA1
31 CMD1
XA2
PEACK* 36 PEACK
+5 39 CKM
5V=9
GND=10,30
PEREQ 24 PEREQ
ERROR 26 ERRDR*
BUSY 25 BUSY*
D0 23 D0
D1 22 D1
D2 21 D2
D3 20 D3
D4 19 D4
D5 18 D5
D6 17 D6
D7 16 D7
D8 15 D8
D9 14 D9
D10 12 D10
D11 11 D11
D12 8 D12
D13 7 D13
D14 6 D14
D15 5 D15
SOCKET
U6
80286
PROCLK 31 CLK
RESCPU 29 RESET
READY* 63 READY
CPUHRQ 64 HOLD
NMI 59 NMI
PEREQ 61 PEREQ
E1* 53 ERROR
54 BUSY
INTR 57 INTR
52 CAP
C26
0.047
5V=30,62
GND=9,35,60
S0 5
S1 4
M/IO 67
CDD/INTA 66 N/C
HLDA 65
PEACK 6
BHE 1 BHE*
LOCK 68 N/C
A0 34
A1 33 A1
A2 32 A2
A3 28 A3
A4 27 A4
A5 26 A5
A6 25 A6
A7 24 A7
A8 23 A8
A9 22 A9
A10 21 A10
A11 20 A11
A12 19 A12
A13 18 A13
A14 17 A14
A15 16 A15
A16 15 A16
A17 14 A17
A18 13 A18
A19 12 A19
A20 11 CA20
A21 10 A21
A22 8 A22
A23 7 A23
D0 36 D0
D1 38 D1
D2 40 D2
D3 42 D3
D4 44 D4
D5 46 D5
D6 48 D6
D7 50 D7
D8 37 D8
D9 39 D9
D10 41 D10
D11 43 D11
D12 45 D12
D13 47 D13
D14 49 D14
D15 51 D15
U5
74ALS245
9 A8 B8 11
A17 8 A7 B7 12 LA17
A18 7 A6 B6 13 LA18
A19 6 A5 B5 14 LA19
A20 5 A4 B4 15 LA20
A21 4 A3 B3 16 LA21
A22 3 A2 B2 17 LA22
A23 2 A1 B1 18 LA23
A→B EN
1 19
MASTER*
PAGE 2
DATA BUS
PAGE 3
PAGE 4
PAGE 5
PAGE 6
I/O CHANNEL

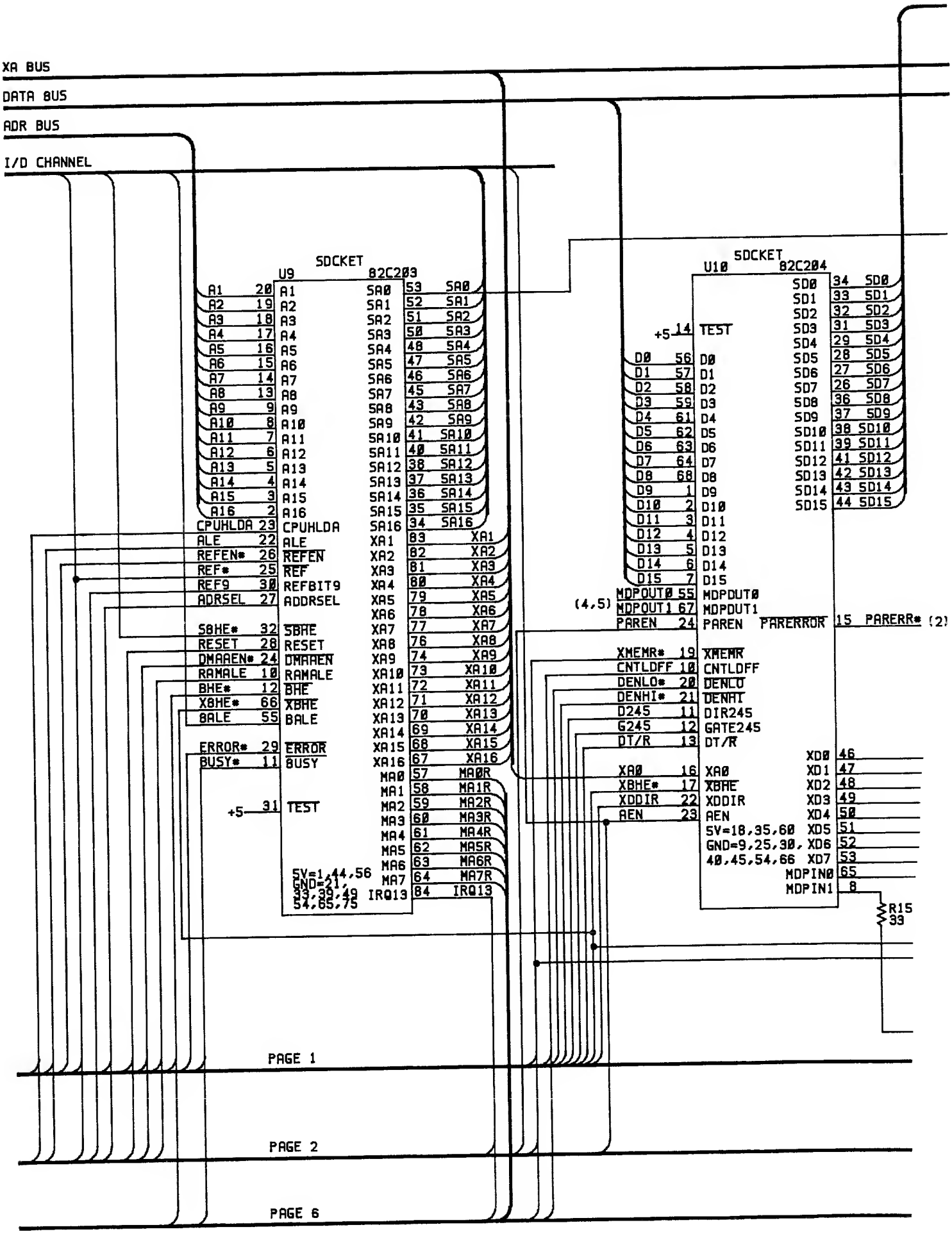

OSC1
64MHZ
OSC
C54
30PF
C56
10PF
U17
14.3181MHZ
R35 33
C63
.1
+5
J32
SPKR
U12
74ALS244
(2) SPKDAT
OSC
CLK
RSTDRV
XMW1R*
XMW0R*
(6)
SOCKET
U15 82C201
(6) PWRGD
0WS*
(2) SWRST
PROCLK
M/IO*
XBHE*
IOCHRDY
F16
IOCS16*
AEN1*
AEN2*
MEMCS16*
LMEGCS*
CPUHLDA
XA3
XA5
XA6
XA7
XA8
XA9
ENMODL
ROMJ
RAMWJ
RAMRJ
REF*
LCSROM1*
POWERGOOD
WS0
SWRST
XTAL1-1
XTAL1-2
FCLK
PROCLKIN
S0
S1
M/IO
A0
A1
XBHE
IOCHRDY
F16
IOCS16
AEN1
AEN2
MEMCS16
LMEGCS
CPUHLDA
MASTER
XA3
XA5
XA6
XA7
XA8
XA9
ENMODL
ROM_3WS
RAMW_1WS
RAMR_1WS
REF
ROMCS
BUSY287
ERROR
5V=32,54,82
GND= 1,27 38,48,59
Q1
RESCPU
RESET
PROCLK
SYSCLK
7.15MHZ
ERAMW
OSC
MHZ119
ENAS
DT/R
CNTLOFF
DENLO
DENHI
READY
ALE
RAS
CAS
RAMALE
BUSY286
IOR
IOW
MEMR
MEMW
INTA
SMEMR
SMEMW
XMEMR
XMEMW
XIOR
XIOW
XDDIR
REFEN
DIR245
GATE245
NPCS
RES287
PPICS
DMAAEN
SA0
R19 33
READY*
R24* 22
R25* 22
R26* 22
R29* 22
R30* 22
R31* 22
MEMR*
MEMW*
INTA*
SMEMR*
SMEMW*
XMEMR*
XMEMW*
XIOR*
XIOW*
* OPTIONAL TO DAMP RINGING
J27 OUT=3WS ROM
IN=2 " "
J29 OUT=1WS RAM WRITE
IN=0 " " "
J23 OUT=1WS RAM READ
IN=0 " " "
0WS*
Q1
RESET
ADRSEL
SYSCLK
7MHZ
ERAMW*
MHZ119
ENAS*
DT/R
CNTLOFF
DENLO*
DENHI*
ALE
RAS
CAS
RAMALE
IOR*
IOW*
MEMR*
MEMW*
PPICS*
DMAAEN*
SA0
XDDIR
REFEN*
D245
G245
PAGE 2
PAGE 3
PAGE 4
PAGE 5
PAGE 6
I/O CHANNEL
VLSI TECHNOLOGY, INC.
VLSI 286 16MHZ PC/AT
E
DRAWING NO. 87091502-S
REV. B

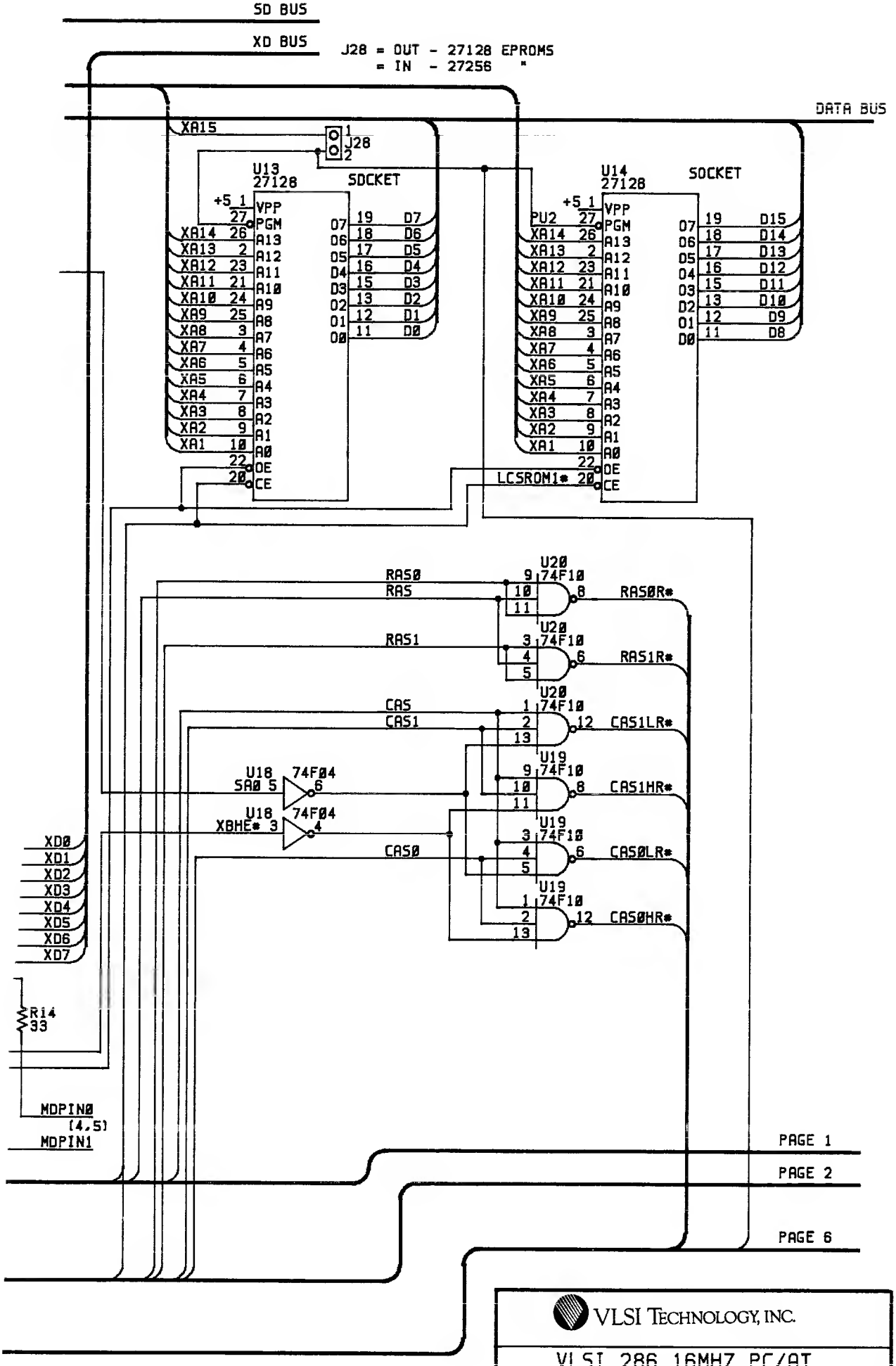

XA BUS
XD BUS
ADR BUS
I/O CHANNEL
SOCKET
U8
82C100
J22 - OUT=SHADOW RAM MAP
J25 J24 *DRAM, TOTAL RAM
IN IN - N/U
IN OUT - 18, 512KB
OUT IN - 36, 1MB
J25
J24
J22
DRQ0 21
DRQ1 20
DRQ2 19
DRQ3 18
DRQ5 17
DRQ6 16
DRQ7 15
IRQ1 14
IRQ3 13
IRQ4 12
IRQ5 11
IRQ6 10
IRQ7 9
IRQ8 81
IRQ9 80
IRQ10 79
IRQ11 78
IRQ12 77
IRQ13 76
IRQ14 75
IRQ15 74
INTA* 6
CPUHRQ 40
MASTER* 45
IOCHRDY 73
SYSCLK 23
MHZ119 41
RESET 24
XD0 34
XD1 33
XD2 32
XD3 31
XD4 30
XD5 29
XD6 28
XD7 27
5V=5,43
GND=22,26,
59,67
DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7 IRQ1 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ8 IRQ9 IRQ10 IRQ11 IRQ12 IRQ13 IRQ14 IRQ15 INTA CPUHRQ MASTER IOCHRDY SYSCLK MHZ119 RESET XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7
DACK0 DACK1 DACK2 DACK3 DACK5 DACK6 DACK7 T/C AEN1 AEN2 CPUHLDA INTR A17 A18 A19 A20 A21 A22 A23 REF XIOR XIOW XMEMR XMEMW OUT2 XA0 XA1 XA2 XA3 XA4 XA5 XA6 XA7 XA8 XA9 XA10 XA11 XA12 XA13 XA14 XA15 XA16
1 DACK0*
83 DACK1*
84 DACK2*
82 DACK3*
2 DACK5*
3 DACK6*
4 DACK7*
39 T/C
8 AEN1*
7 AEN2*
44 CPUHLDA
46 INTR
72 A17
71 A18
70 A19
69 A20
68 A21
66 A22
65 A23
25 REF*
38 XIOR*
37 XIOW*
35 XMEMR*
36 XMEMW*
42
47 XA0
48 XA1
49 XA2
50 XA3
51 XA4
52 XA5
53 XA6
54 XA7
55 XA8
56 XA9
57 XA10
58 XA11
60 XA12
61 XA13
62 XA14
63 XA15
64 XA16
U18
74F04
10
11 RINT*
PAGE 1
PAGE 3
PAGE 6



VLSI TECHNOLOGY, INC.		
VLSI 286 16MHZ PC/AT		
E	DRAWING NO. 87091502-5	REV. B
DATE: 1/03/89	SHEET 2 OF 8	

7

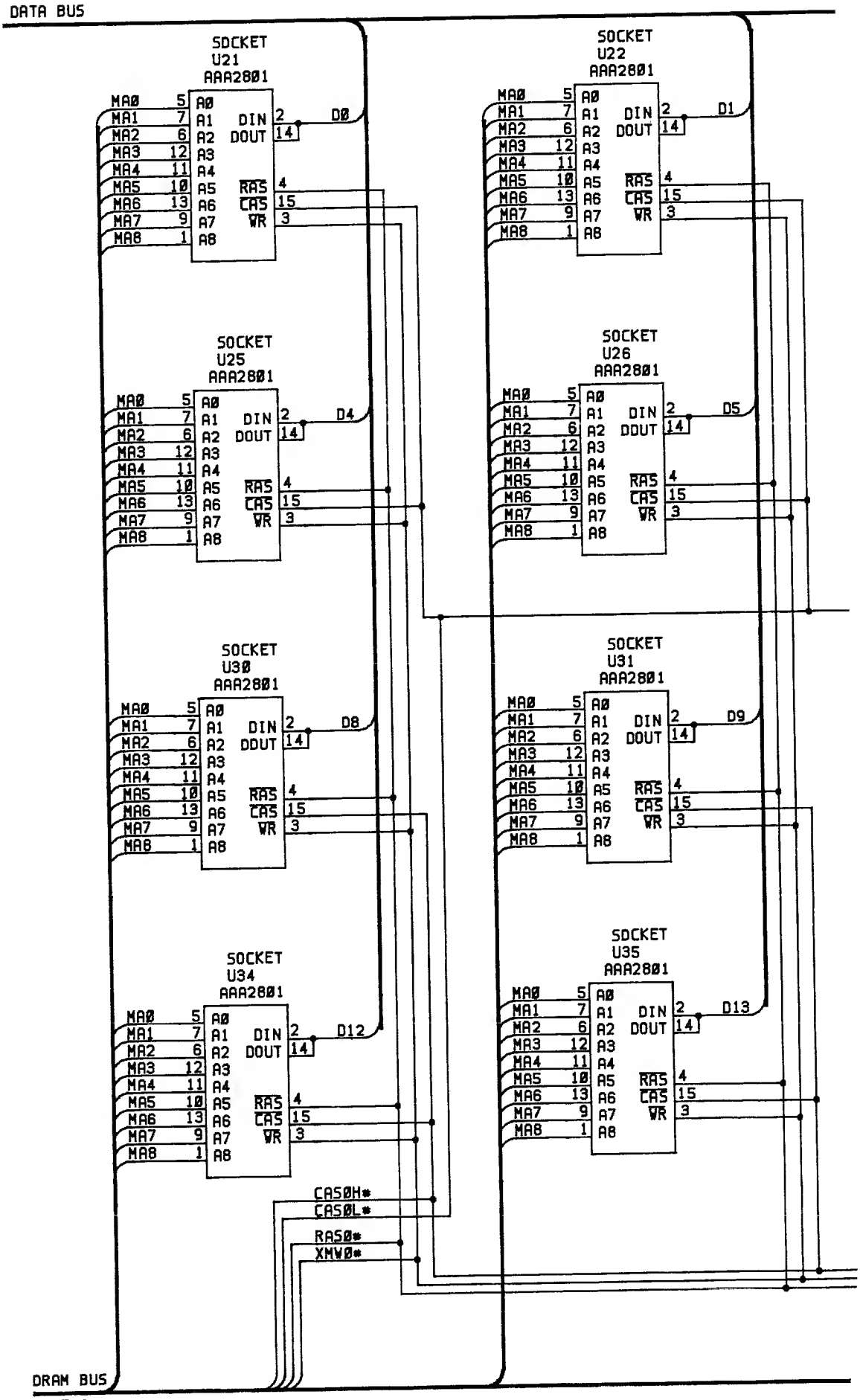

XA BUS
DATA BUS
ADR BUS
I/D CHANNEL
SOCKET
U9
82C203
A1 20 A1
A2 19 A2
A3 18 A3
A4 17 A4
A5 16 A5
A6 15 A6
A7 14 A7
A8 13 A8
A9 9 A9
A10 8 A10
A11 7 A11
A12 6 A12
A13 5 A13
A14 4 A14
A15 3 A15
A16 2 A16
CPUHLDA 23 CPUHLDA
ALE 22 ALE
REFEN* 26 REFEN
REF* 25 REF
REF9 30 REFBIT9
ADRSEL 27 ADDRSEL
SBHE* 32 SBHE
RESET 28 RESET
DMAAEN* 24 DMAAEN
RAMALE 10 RAMALE
BHE* 12 BHE
XBHE* 66 XBHE
BALE 55 BALE
ERROR* 29 ERROR
BUSY* 11 BUSY
+5 31 TEST
5V=1,44,56
GND=21,
33,39,49
54,65,75
SA0 53 SA0
SA1 52 SA1
SA2 51 SA2
SA3 50 SA3
SA4 48 SA4
SA5 47 SA5
SA6 46 SA6
SA7 45 SA7
SA8 43 SA8
SA9 42 SA9
SA10 41 SA10
SA11 40 SA11
SA12 38 SA12
SA13 37 SA13
SA14 36 SA14
SA15 35 SA15
SA16 34 SA16
XA1 83 XA1
XA2 82 XA2
XA3 81 XA3
XA4 80 XA4
XA5 79 XA5
XA6 78 XA6
XA7 77 XA7
XA8 76 XA8
XA9 74 XA9
XA10 73 XA10
XA11 72 XA11
XA12 71 XA12
XA13 70 XA13
XA14 69 XA14
XA15 68 XA15
XA16 67 XA16
MA0 57 MA0R
MA1 58 MA1R
MA2 59 MA2R
MA3 60 MA3R
MA4 61 MA4R
MA5 62 MA5R
MA6 63 MA6R
MA7 64 MA7R
IRQ13 84 IRQ13
SOCKET
U10
82C204
+5 14 TEST
D0 56 D0
D1 57 D1
D2 58 D2
D3 59 D3
D4 61 D4
D5 62 D5
D6 63 D6
D7 64 D7
D8 68 D8
D9 1 D9
D10 2 D10
D11 3 D11
D12 4 D12
D13 5 D13
D14 6 D14
D15 7 D15
MDPOUT0 55 MDPOUT0
(4,5) MDPOUT1 67 MDPOUT1
PAREN 24 PAREN
PARERROR 15 PARERR* (2)
XMEMR* 19 XMEMR
CNTLOFF 10 CNTLOFF
DENLO* 20 DENLO
DENHI* 21 DENHI
D245 11 DIR245
G245 12 GATE245
DT/R 13 DT/R
XA0 16 XA0
XBHE* 17 XBHE
XDDIR 22 XDDIR
AEN 23 AEN
5V=18,35,60
GND=9,25,30,
40,45,54,66
SD0 34 SD0
SD1 33 SD1
SD2 32 SD2
SD3 31 SD3
SD4 29 SD4
SD5 28 SD5
SD6 27 SD6
SD7 26 SD7
SD8 36 SD8
SD9 37 SD9
SD10 38 SD10
SD11 39 SD11
SD12 41 SD12
SD13 42 SD13
SD14 43 SD14
SD15 44 SD15
XD0 46
XD1 47
XD2 48
XD3 49
XD4 50
XD5 51
XD6 52
XD7 53
MDPIN0 65
MDPIN1 8
R15
33
PAGE 1
PAGE 2
PAGE 6



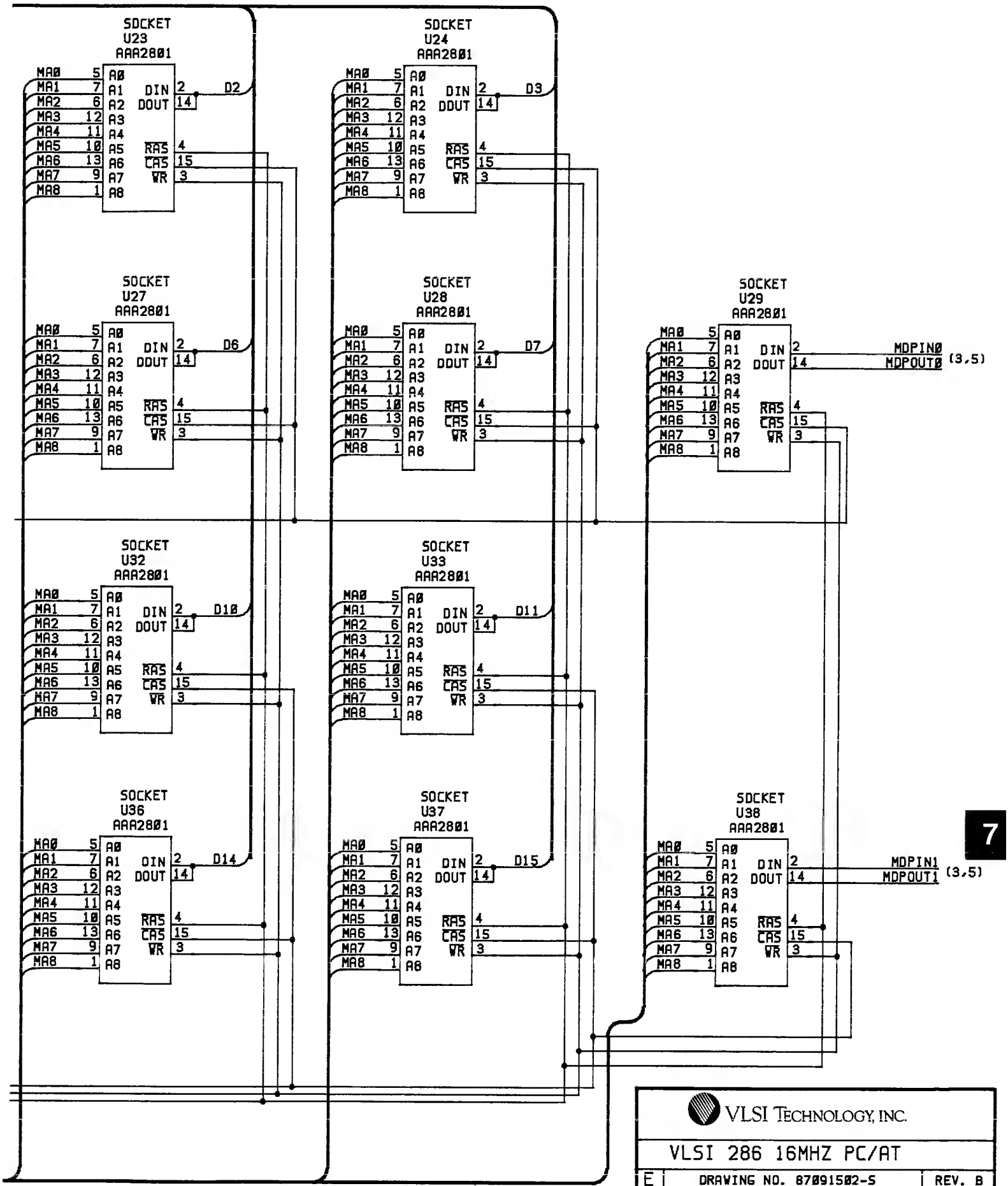
VLSI TECHNOLOGY, INC.

VLSI 286 16MHZ PC/AT

E | DRAWING NO. 87091502-S | REV. B


DATA BUS
SOCKET U21 AAA2801
SOCKET U22 AAA2801
SOCKET U25 AAA2801
SOCKET U26 AAA2801
SOCKET U30 AAA2801
SOCKET U31 AAA2801
SOCKET U34 AAA2801
SOCKET U35 AAA2801
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8
A0 A1 A2 A3 A4 A5 A6 A7 A8
DIN DOUT
RAS CAS WR
D0 D1 D4 D5 D8 D9 D12 D13
CAS0H*
CAS0L*
RAS0*
XMW0*
DRAM BUS

MEMORY BANK Ø

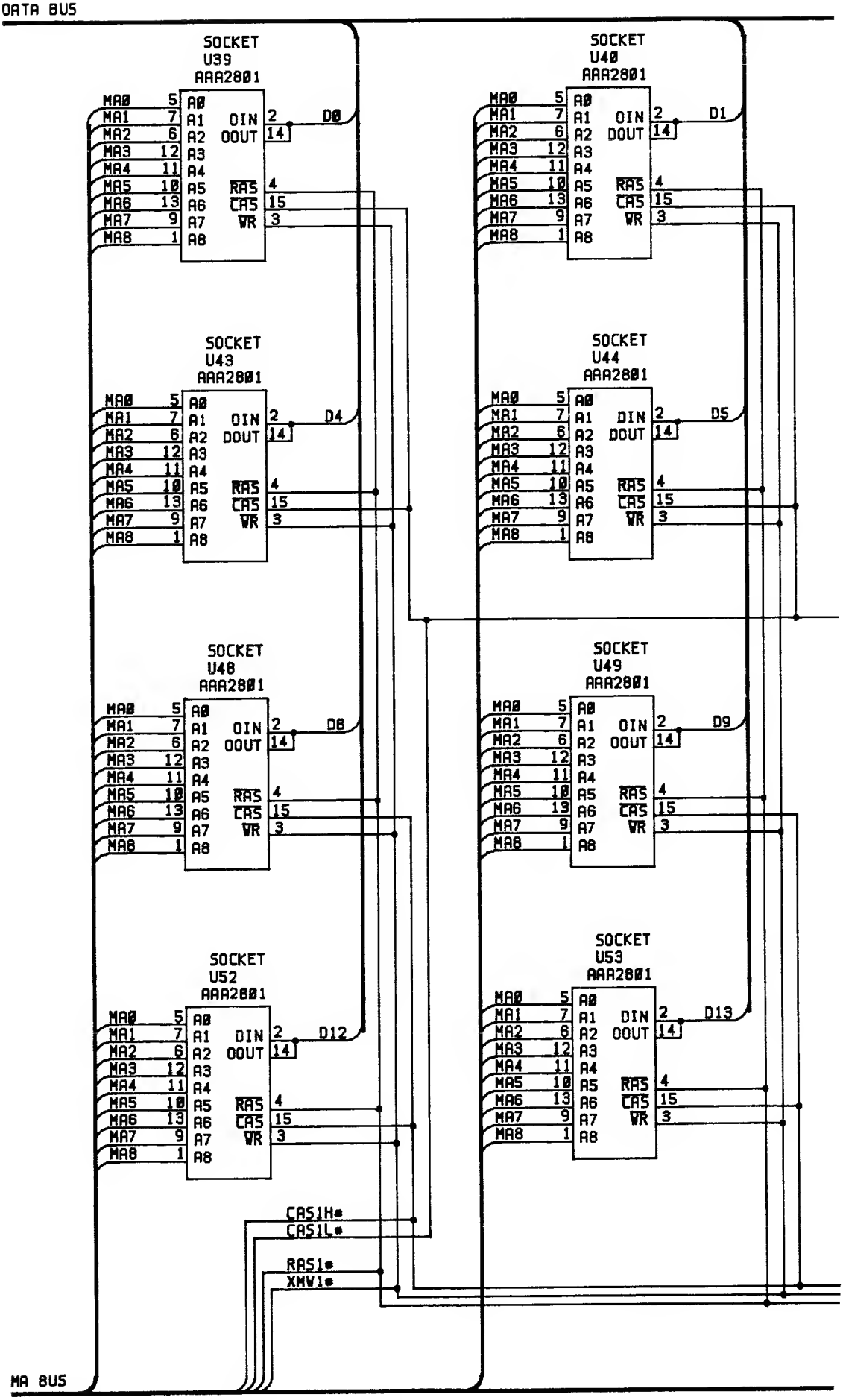


7

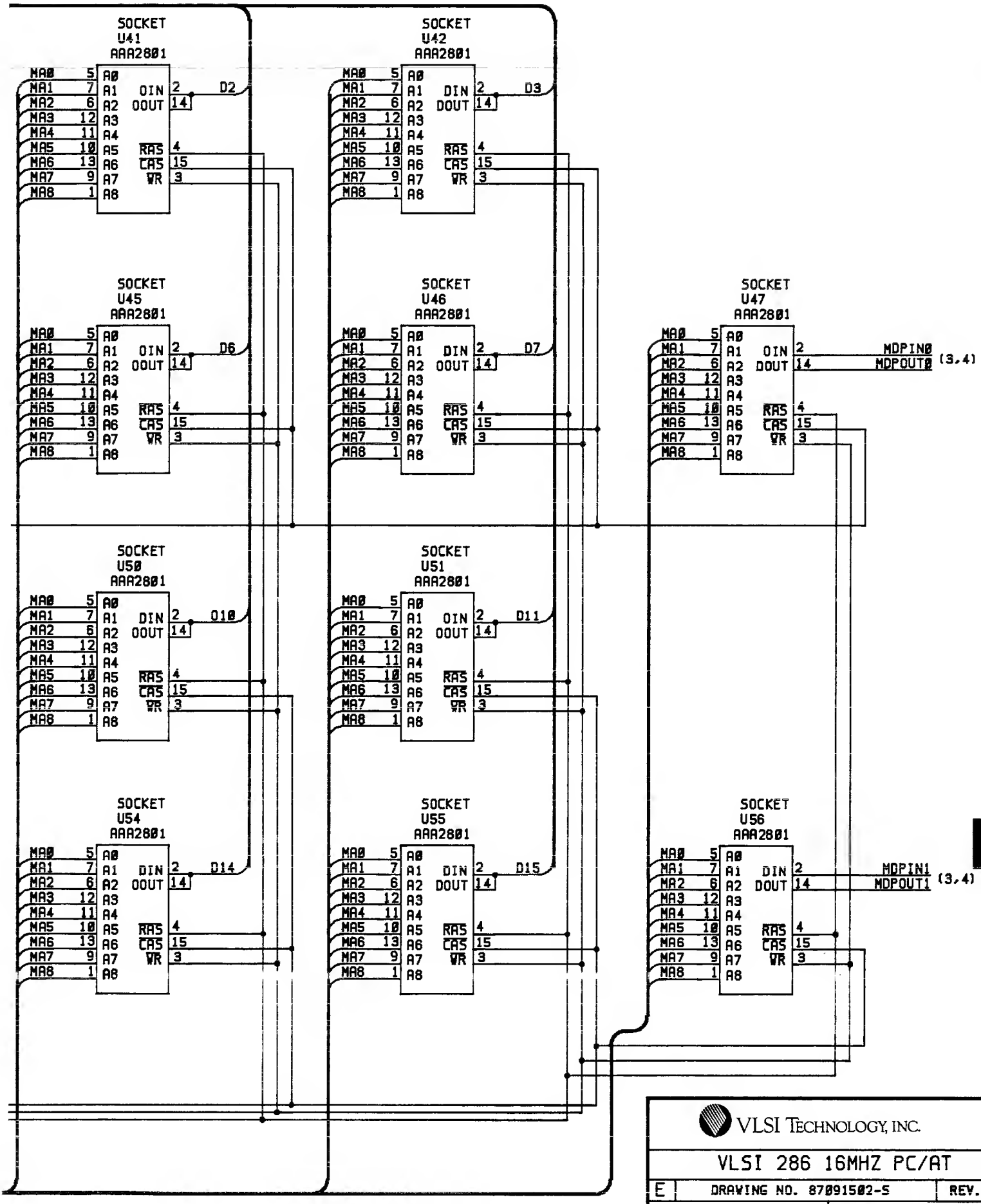
VLSI TECHNOLOGY, INC.

VLSI 286 16MHZ PC/AT

E	DRAWING NO. 87091502-S	REV. B
DATE: 1/03/89	SHEET 4 OF 8	


DATA BUS
SOCKET
U39
AAA2801
SOCKET
U40
AAA2801
SOCKET
U43
AAA2801
SOCKET
U44
AAA2801
SOCKET
U48
AAA2801
SOCKET
U49
AAA2801
SOCKET
U52
AAA2801
SOCKET
U53
AAA2801
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
A0
A1
A2
A3
A4
A5
A6
A7
A8
DIN
DOUT
RAS
CAS
WR
D0
D1
D4
D5
D8
D9
D12
D13
CA51H*
CA51L*
RA51*
XMW1*
MA BUS

MEMORY BANK 1

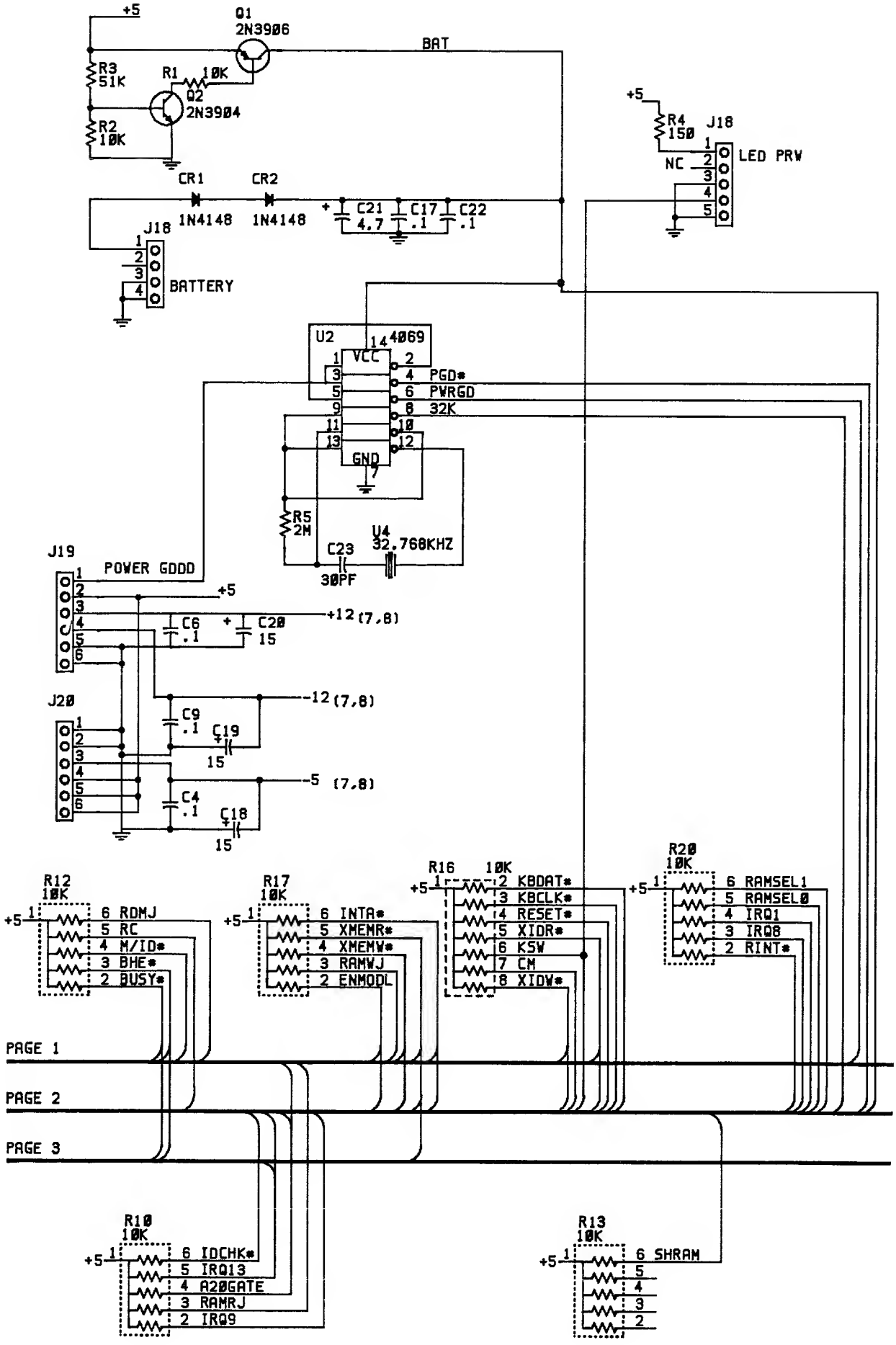


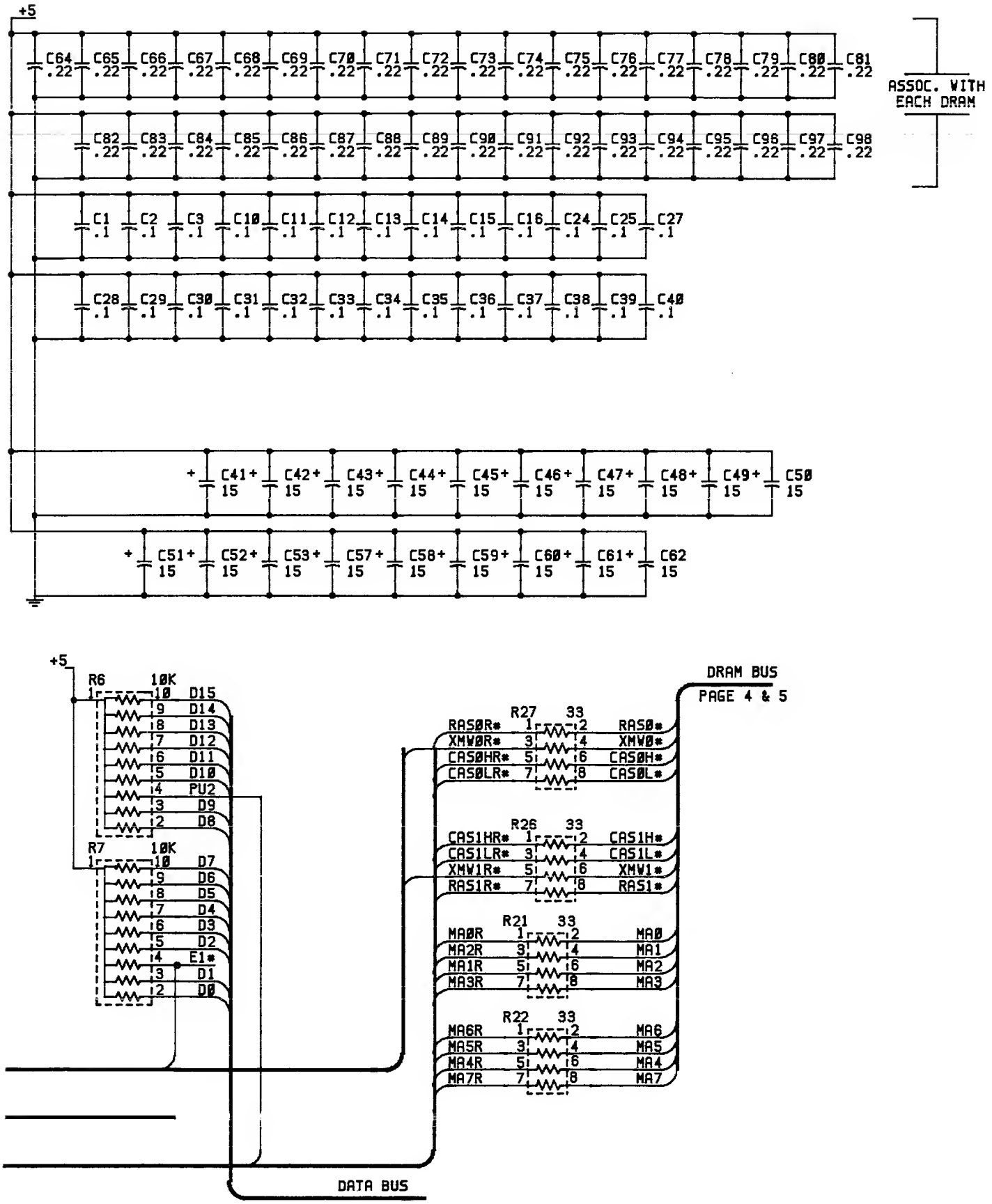
7

VLSI TECHNOLOGY, INC.

VLSI 286 16MHZ PC/AT

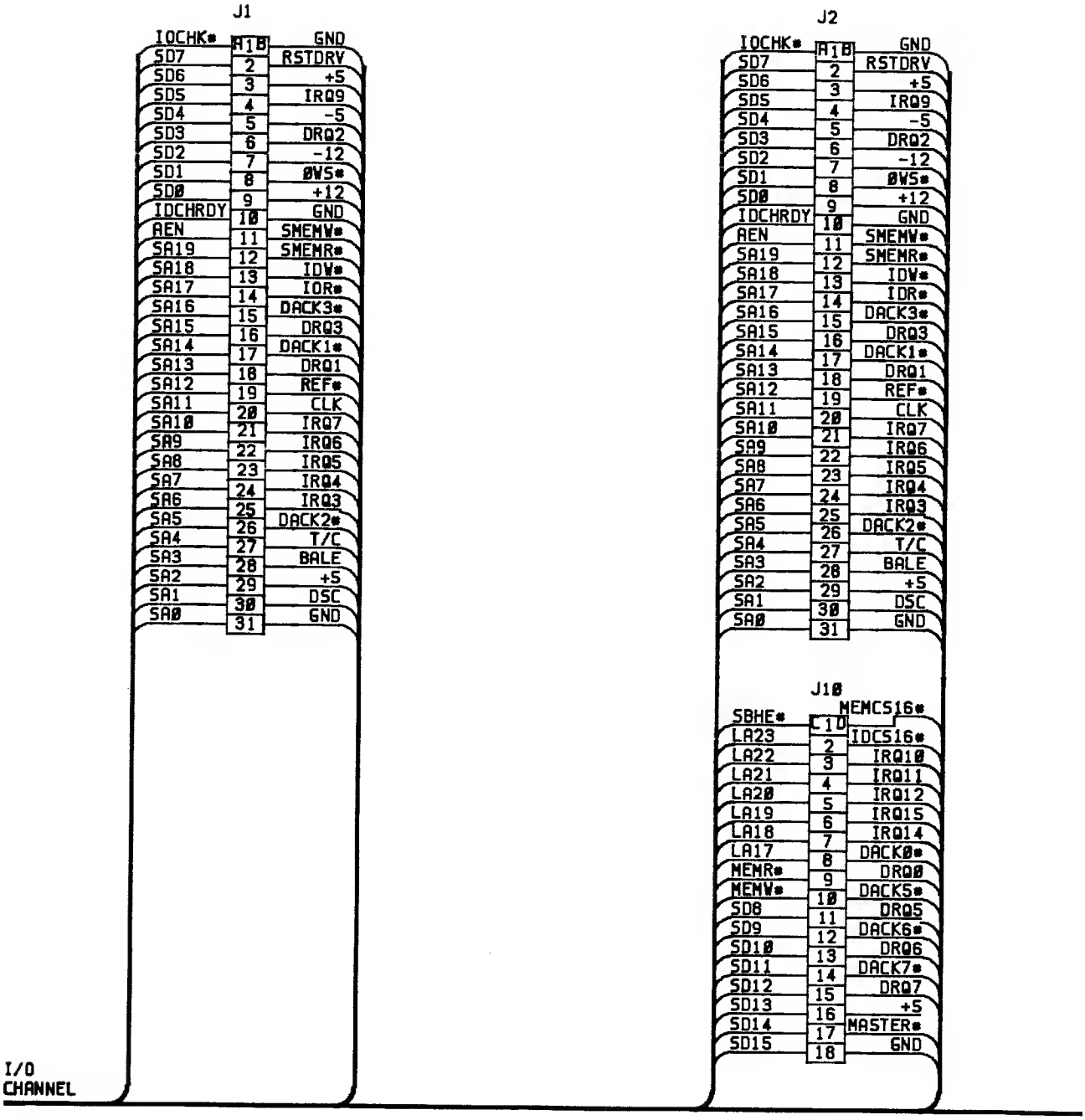
E	DRAWING NO. 87091502-S	REV. B
DATE: 1/03/89	SHEET 5 OF 8	

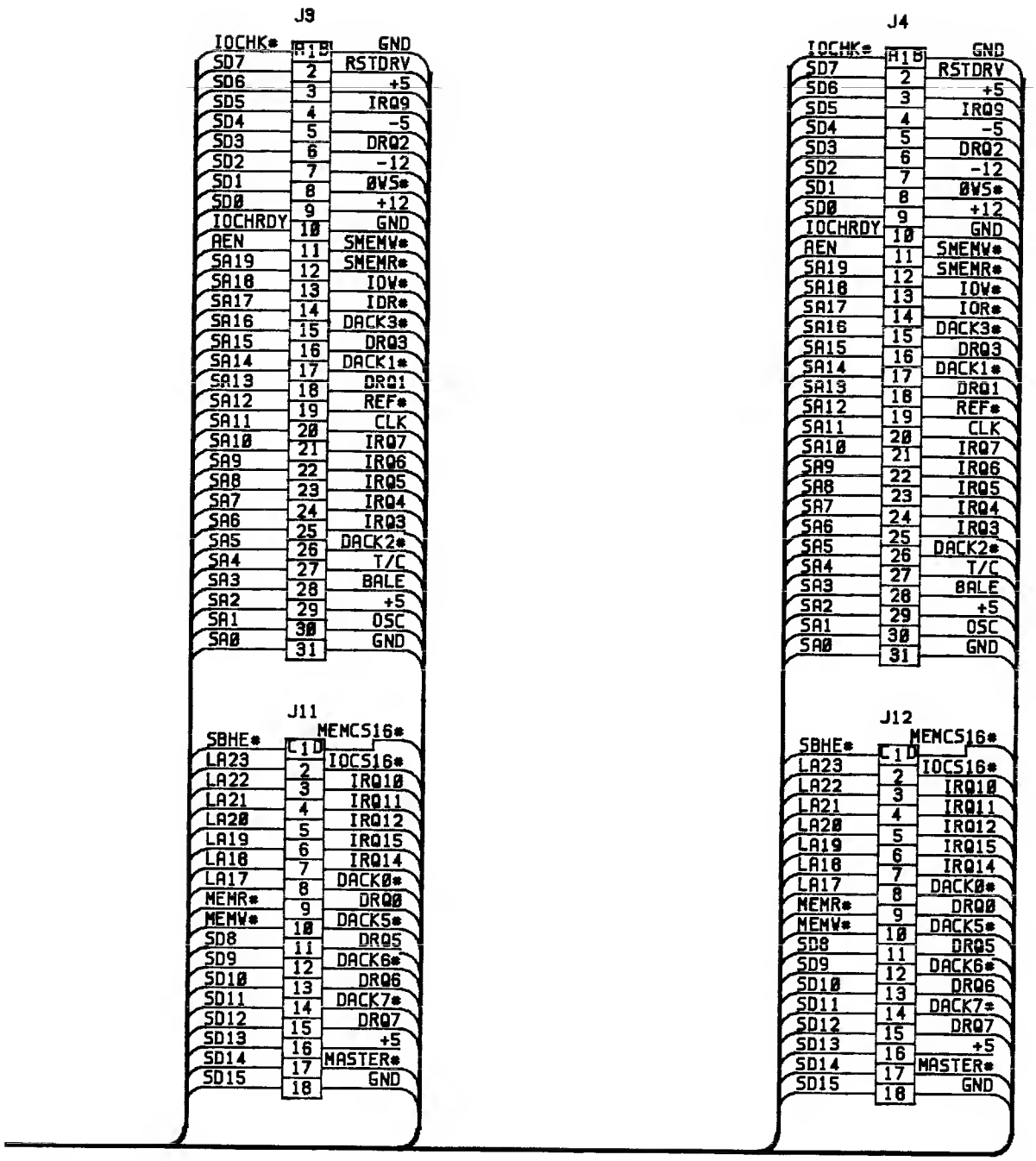

+5
Q1
2N3906
BAT
R3
51K
R1
10K
Q2
2N3904
R2
10K
CR1
CR2
1N4148
1N4148
C21
4.7
C17
.1
C22
.1
J18
BATTERY
+5
R4
150
J18
NC
LED PRW
U2
4069
VCC
PGD*
PWRGD
32K
GND
R5
2M
U4
32.768KHZ
C23
30PF
J19
POWER GDDD
+5
+12 (7,8)
C6
.1
C20
15
J20
-12 (7,8)
C9
.1
C19
15
-5 (7,8)
C4
.1
C18
15
R12
10K
6 RDMJ
5 RC
4 M/IO*
3 BHE*
2 BUSY*
R17
10K
6 INTA*
5 XMEMR*
4 XMEMW*
3 RAMWJ
2 ENMODL
R16
10K
2 KBDAT*
3 KBCLK*
4 RESET*
5 XIDR*
6 KSW
7 CM
8 XIDW*
R20
10K
6 RAMSEL1
5 RAMSEL0
4 IRQ1
3 IRQ8
2 RINT*
PAGE 1
PAGE 2
PAGE 3
R10
10K
6 IDCHK*
5 IRQ13
4 A20GATE
3 RAMRJ
2 IRQ9
R13
10K
6 SHRAM
5
4
3
2



VLSI TECHNOLOGY, INC.		
VLSI 286 16MHZ PC/AT		
E	DRAWING NO. 87091502-5	REV. B
DATE: 1/03/89	SHEET 6 OF 8	

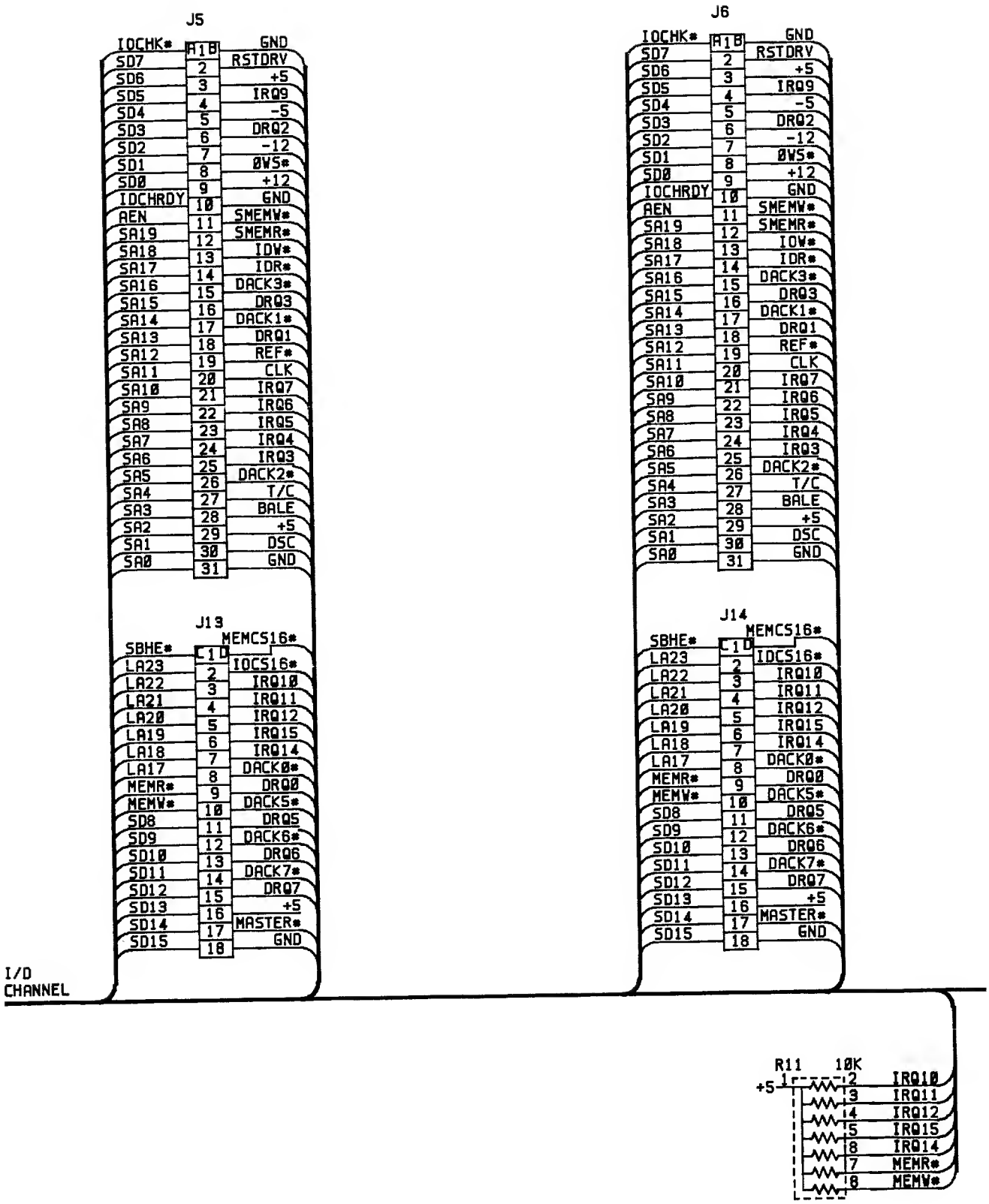
7

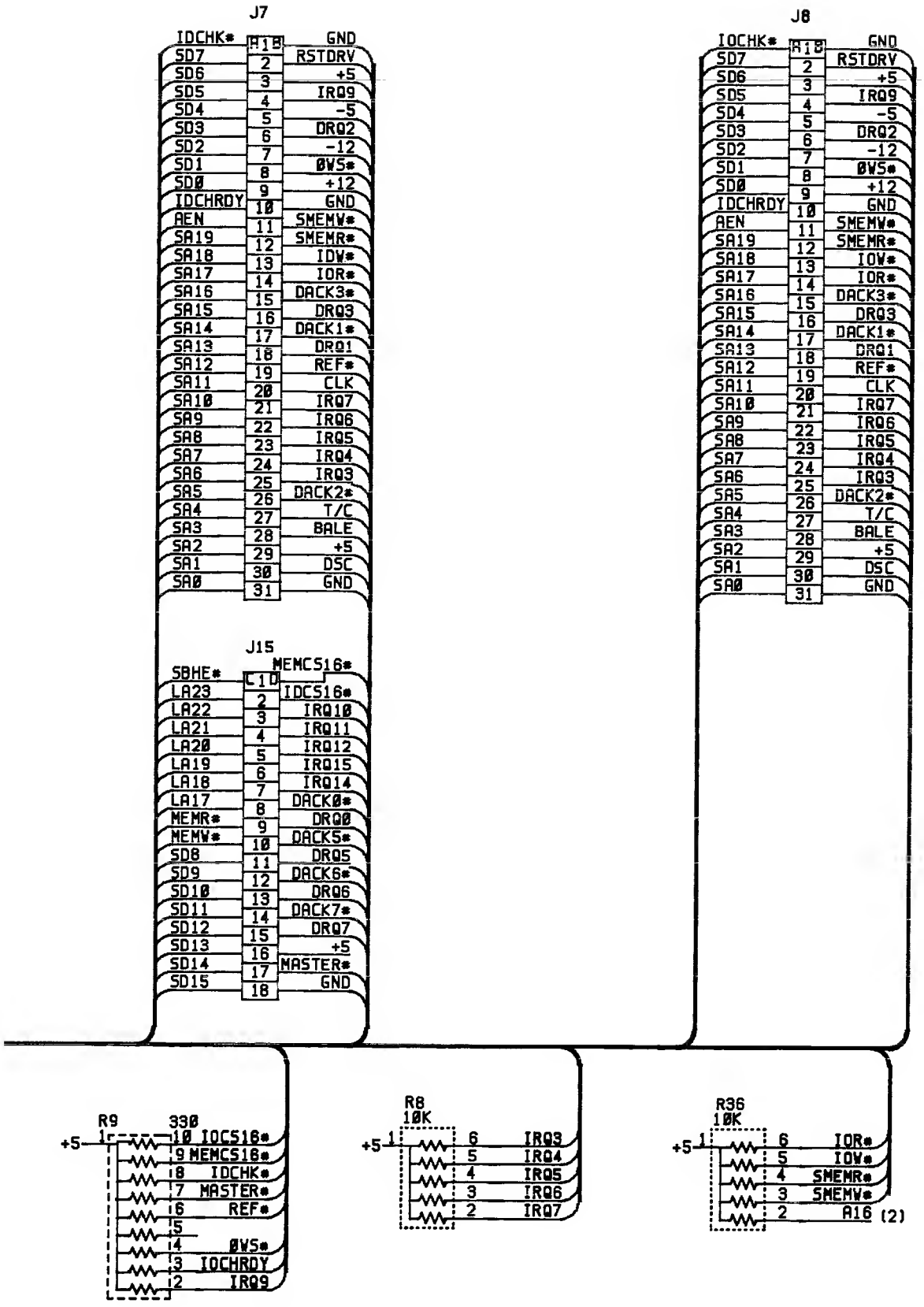

J1
IOCHK* A1 B1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 ØWS*
SDØ 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW*
SA19 12 SMEMR*
SA18 13 IOW*
SA17 14 IOR*
SA16 15 DACK3*
SA15 16 DRQ3
SA14 17 DACK1*
SA13 18 DRQ1
SA12 19 REF*
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2*
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SAØ 31 GND
J2
IOCHK* A1 B1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 ØWS*
SDØ 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW*
SA19 12 SMEMR*
SA18 13 IOW*
SA17 14 IOR*
SA16 15 DACK3*
SA15 16 DRQ3
SA14 17 DACK1*
SA13 18 DRQ1
SA12 19 REF*
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2*
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SAØ 31 GND
J1Ø
SBHE* C1 D1 MEMCS16*
LA23 2 IOCS16*
LA22 3 IRQ1Ø
LA21 4 IRQ11
LA2Ø 5 IRQ12
LA19 6 IRQ15
LA18 7 IRQ14
LA17 8 DACKØ*
MEMR* 9 DRQØ
MEMW* 10 DACK5*
SD8 11 DRQ5
SD9 12 DACK6*
SD1Ø 13 DRQ6
SD11 14 DACK7*
SD12 15 DRQ7
SD13 16 +5
SD14 17 MASTER*
SD15 18 GND
I/O CHANNEL



7

VLSI TECHNOLOGY, INC.		
VLSI 286 16MHZ PC/AT		
E	DRAWING NO. 87091502-S	REV. B


J5
IOCHK* A1 B1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 0WS*
SD0 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW*
SA19 12 SMEMR*
SA18 13 IOW*
SA17 14 IOR*
SA16 15 DACK3*
SA15 16 DRQ3
SA14 17 DACK1*
SA13 18 DRQ1
SA12 19 REF*
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2*
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SA0 31 GND
J6
IOCHK* A1 B1 GND
SD7 2 RSTDRV
SD6 3 +5
SD5 4 IRQ9
SD4 5 -5
SD3 6 DRQ2
SD2 7 -12
SD1 8 0WS*
SD0 9 +12
IOCHRDY 10 GND
AEN 11 SMEMW*
SA19 12 SMEMR*
SA18 13 IOW*
SA17 14 IOR*
SA16 15 DACK3*
SA15 16 DRQ3
SA14 17 DACK1*
SA13 18 DRQ1
SA12 19 REF*
SA11 20 CLK
SA10 21 IRQ7
SA9 22 IRQ6
SA8 23 IRQ5
SA7 24 IRQ4
SA6 25 IRQ3
SA5 26 DACK2*
SA4 27 T/C
SA3 28 BALE
SA2 29 +5
SA1 30 OSC
SA0 31 GND
J13
MEMCS16*
SBHE* C1 D1 IOCS16*
LA23 2 IRQ10
LA22 3 IRQ11
LA21 4 IRQ12
LA20 5 IRQ15
LA19 6 IRQ14
LA18 7 DACK0*
LA17 8 DRQ0
MEMR* 9 DACK5*
MEMW* 10 DRQ5
SD8 11 DACK6*
SD9 12 DRQ6
SD10 13 DACK7*
SD11 14 DRQ7
SD12 15 +5
SD13 16 MASTER*
SD14 17 GND
SD15 18
J14
MEMCS16*
SBHE* C1 D1 IOCS16*
LA23 2 IRQ10
LA22 3 IRQ11
LA21 4 IRQ12
LA20 5 IRQ15
LA19 6 IRQ14
LA18 7 DACK0*
LA17 8 DRQ0
MEMR* 9 DACK5*
MEMW* 10 DRQ5
SD8 11 DACK6*
SD9 12 DRQ6
SD10 13 DACK7*
SD11 14 DRQ7
SD12 15 +5
SD13 16 MASTER*
SD14 17 GND
SD15 18
I/O CHANNEL
R11 10K
+5 1 2 IRQ10
3 IRQ11
4 IRQ12
5 IRQ15
8 IRQ14
7 MEMR*
8 MEMW*



VLSI TECHNOLOGY, INC.		
VLSI 286 16MHZ PC/AT		
E	DRAWING NO. 87Ø915Ø2-5	REV. B
DATE: 1/23/89	SHEET 8 OF 8	

7

VLSI TECHNOLOGY, INC.

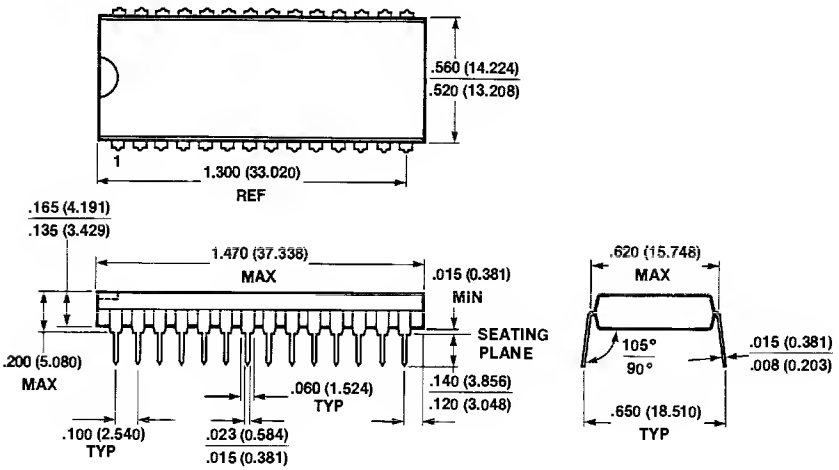
SECTION 8

PACKAGE OUTLINES

Logic Products Division

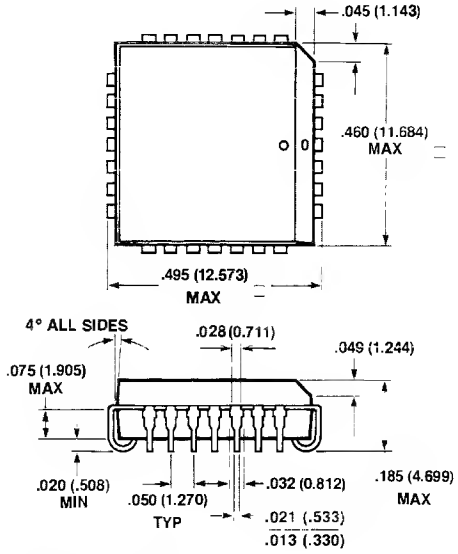

VLSI TECHNOLOGY, INC.

28-PIN PLASTIC DUAL IN-LINE



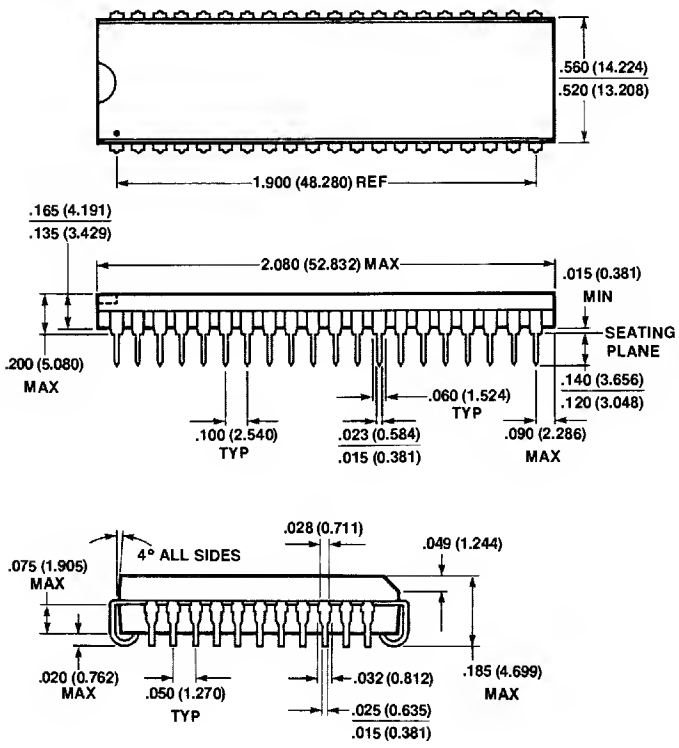
NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN PLASTIC LEADED CHIP CARRIER



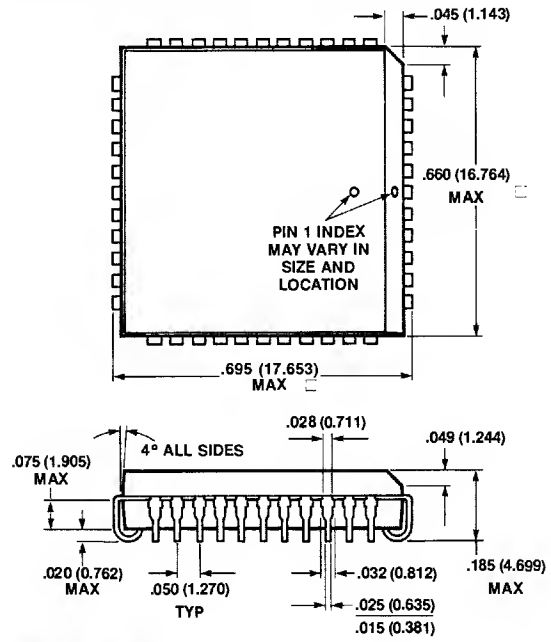
NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR Sn Pb SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

40- PIN PLASTIC DUAL IN-LINE



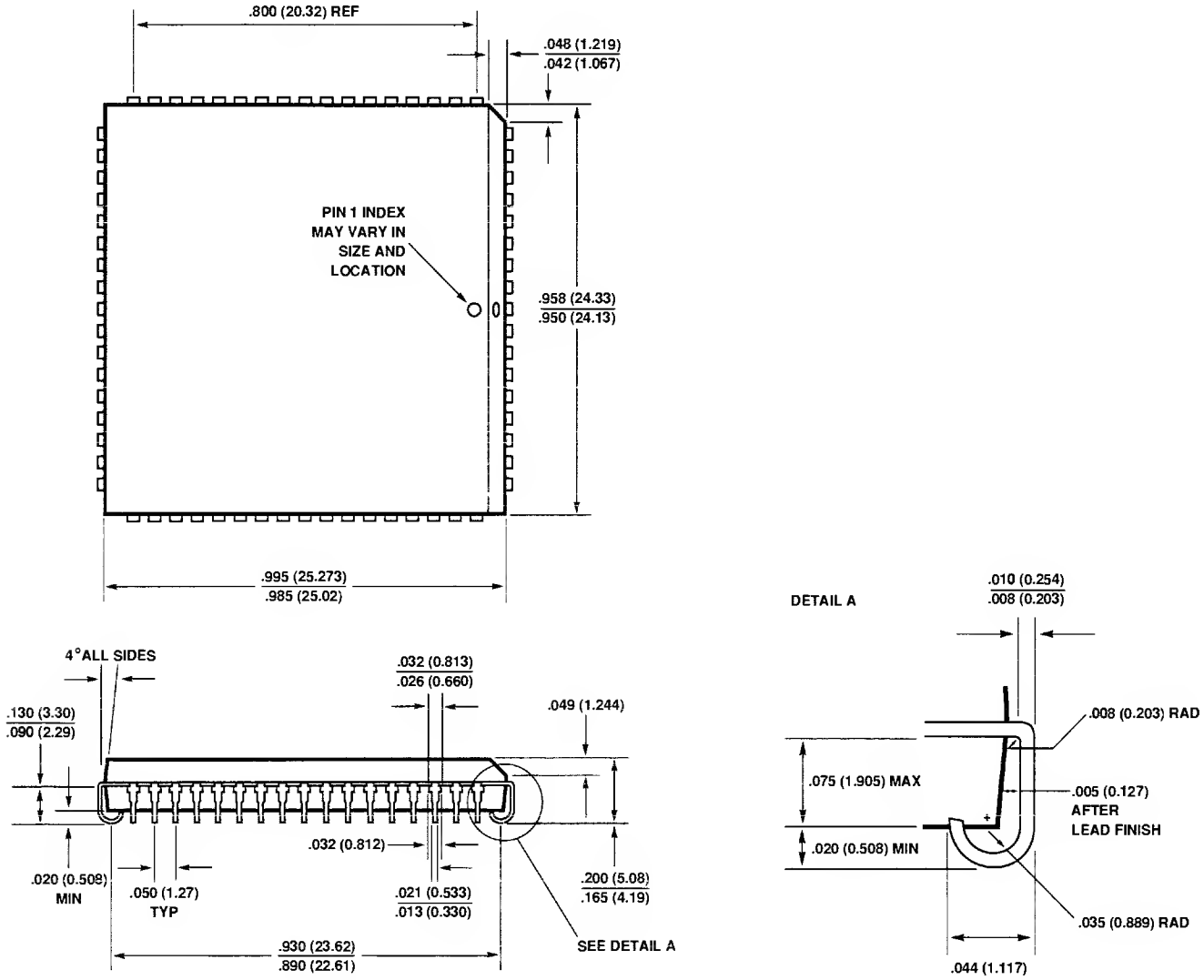
NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

44-PIN PLASTIC LEADED CHIP CARRIER



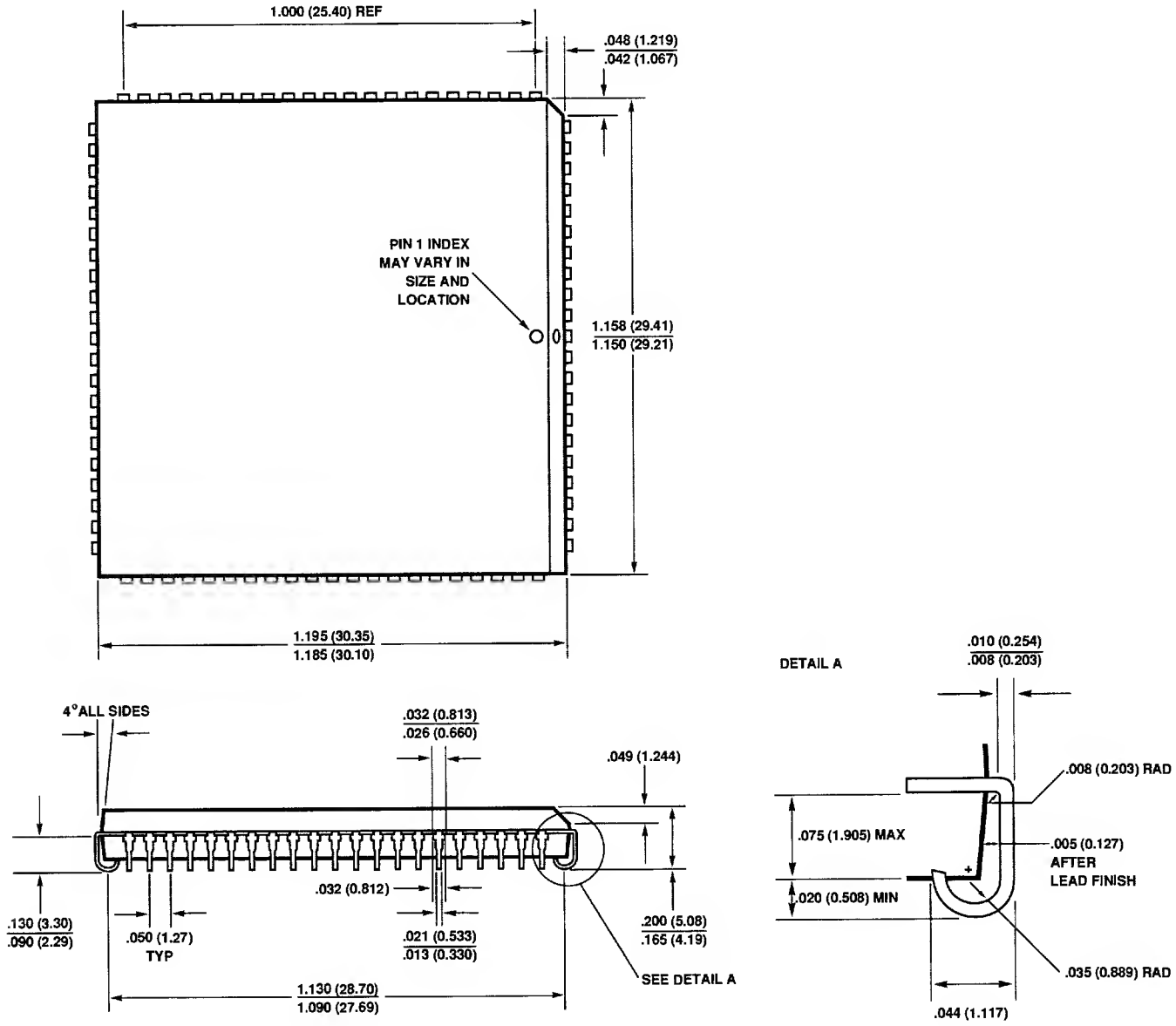
NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

68-PIN PLASTIC LEADED CHIP CARRIER



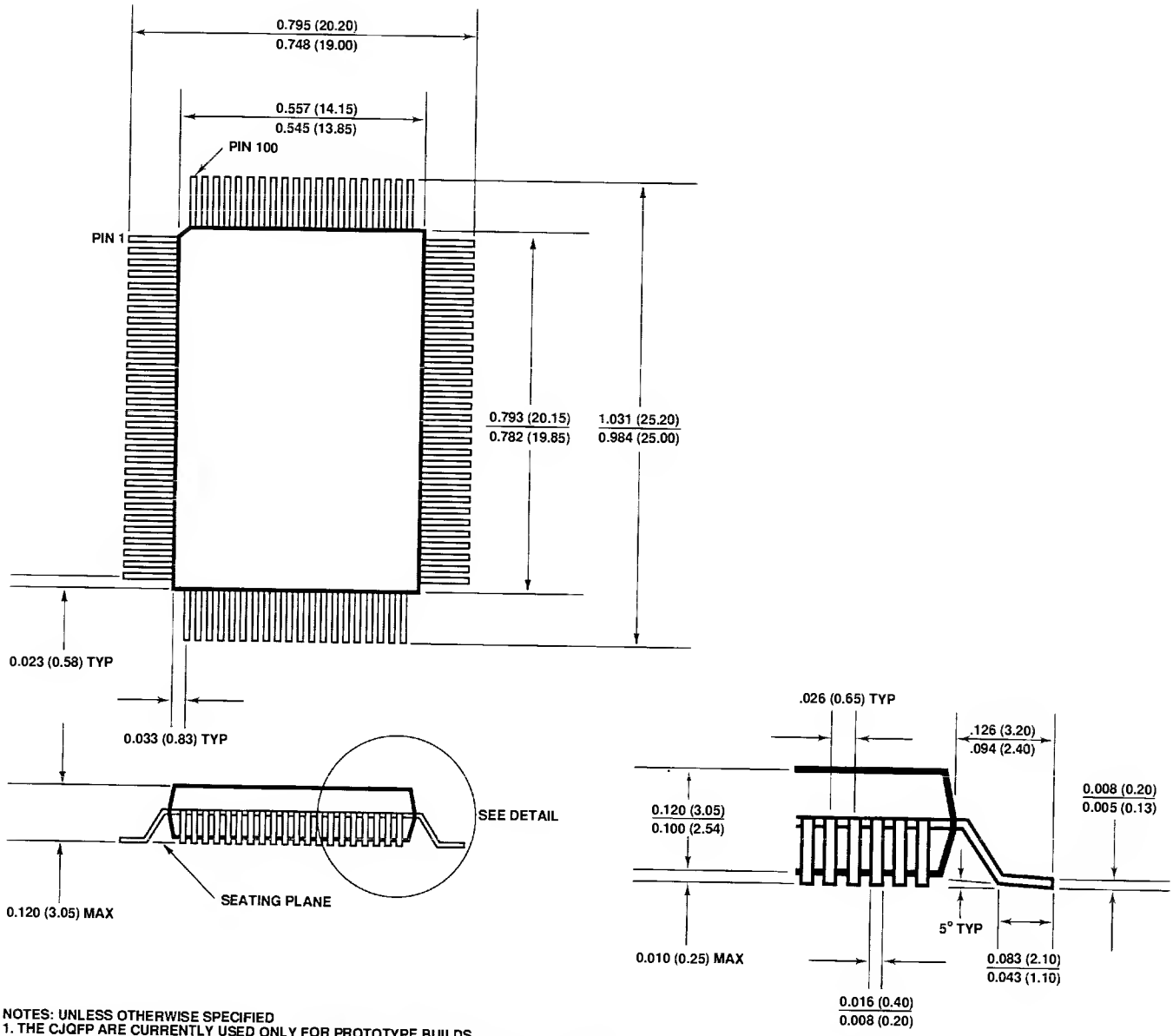
NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

84-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

100-PIN PLASTIC FLATPACK



NOTES: UNLESS OTHERWISE SPECIFIED
1. THE CJQFP ARE CURRENTLY USED ONLY FOR PROTOTYPE BUILDS.
2. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.
3. CJQFP ARE EPOXY DIE ATTACHED AND EPOXY SEALED.
4. LEADFRAME: ALLOY 42
   DIE ATTACH MATERIAL: HITACHI CHE EN-4000, KASEI EPINAR 4110
   MOLD COMPOUND: SUMITOMO 6300, KASEI CEL 4000

NOTES:

VLSI TECHNOLOGY, INC.

SECTION 9

SALES OFFICES, DESIGN CENTERS, AND DISTRIBUTORS

Logic Products Division


VLSI TECHNOLOGY, INC.

VLSI TECHNOLOGY, INC.

SALES OFFICES, DESIGN CENTERS, AND DISTRIBUTORS

VLSI CORPORATE OFFICES

CORPORATE HEADQUARTERS • ASIC AND MEMORY PRODUCTS • VLSI Technology, Inc. • 1109 McKay Drive • San Jose, CA 95131 • 408-434-3100
LOGIC AND GOVERNMENT PRODUCTS • VLSI Technology, Inc. • 8375 South River Parkway • Tempe, AZ 85284 • 602-752-8574

VLSI SALES OFFICES AND TECH CENTERS

CALIFORNIA
2235 Qume Dr.
San Jose, CA 95131
408-922-5200
FAX 408-943-9792
TELEX 278807
MAIL
1109 McKay Dr.
San Jose, CA 95131

30 Corporate Park, Stes. 100-102
Irvine, CA 92714
714-250-4900
FAX 714-250-9041

FLORIDA
2200 Park Central N., Ste. 600
Pompano Beach, FL 33064
305-971-0404
FAX 305-971-2086

ILLINOIS
1350 Remington Rd., Stes. A-D
Schaumburg, IL 60195
312-310-9595
FAX 312-310-9632

MASSACHUSETTS
261 Ballardvale St.
Wilmington, MA 01887
508-658-9501
FAX 508-658-0423

NEW JERSEY
101 Morgan Lane, Ste. 380
Plainsboro, NJ 08536
609-799-5700
FAX 609-799-5720

TEXAS
850 E. Arapaho Rd., Ste. 270
Richardson, TX 75081
214-231-6716
FAX 214-669-1413

FRANCE
2, Allee des Garays
F-91124 Palaiseau Cedex
France
1-6447.04.79
TELEX vlsifr 600 759 F
FAX 1-6447.04.80

GERMANY
Rosenkavalierplatz 10
D-8000 Munich 81
West Germany
69-9269050
TELEX 521 4279 vlsid
FAX 89-92690545

HONG KONG
Shui On Centre 28/12
8 Harbor Road
Hong Kong
852-5-865-3755
FAX 852-5-865-3159

JAPAN
Shuwa-Kioicho TBR Bldg., Room 101
5-7 Kojimachi, Chiyoda-Ku
Tokyo, Japan 102
81-3-239-5211
FAX 81-3-239-5215

UNITED KINGDOM
486-488 Midsummer Blvd.
Saxon Gate West, Central
Milton Keynes, MK9 2EQ
United Kingdom
09 08/66 75 95
TELEX vlsiuk 825 135
FAX 09 08/67 00 27

VLSI SALES OFFICES

ALABAMA
2614 Artie St., Ste. 36
Huntsville, AL 35805
205-539-5513
FAX 205-536-8622

ARIZONA
8375 South River Parkway
Tempe, AZ 85284
602-752-6450
FAX 602-752-8001

CONNECTICUT
60 Church St., Ste. 16
Yalesville, CT 06492
203-265-6698
FAX 203-265-3653

FLORIDA
601 Cleveland St., Ste. 400
Clearwater, FL 33515
813-443-5797
FAX 813-443-5674

5955 T.G. Lee Blvd., Ste. 170
Orlando, FL 32822
407-240-9604
FAX 407-855-2595

GEORGIA
2400 Pleasant Hill Rd., Ste. 200
Duluth, GA 30136
404-476-8574
FAX 404-476-3790

MARYLAND
P.O. Box 289
124 Maryland, Rte. 3 N.
Millersville, MD 21108
301-987-8777
FAX 301-987-8779

MINNESOTA
5871 Cedar Lake Rd., Ste. 9
St. Louis Park, MN 55416
612-545-1490
FAX 612-545-3489

NORTH CAROLINA
1000 Park Forty Plaza, Ste. 300
Durham, NC 27713
919-544-1891/92
FAX 919-544-6667

OHIO
4 Commerce Park Sq.
23200 Chagrin Boulevard, Ste. 600
Cleveland, OH 44122
216-292-8235
FAX 216-464-7609

OREGON
10300 S.W. Greenburg Rd., Ste. 365
Portland, OR 97223
503-244-9882
FAX 503-245-0375

TEXAS
9600 Great Hills Trail, Ste. 150W
Austin, TX 78759
512-343-8191
FAX 512-343-2759

VLSI AUTHORIZED DESIGN CENTERS

COLORADO
SIS MICROELECTRONICS, INC.
Longmont, 303-776-1667

MAINE
OUADIC SYSTEMS, INC.
South Portland, 207-871-8244

PENNSYLVANIA
INTEGRATED CIRCUIT SYSTEMS, INC.
King of Prussia, 215-265-8690

EIRE AND U.K.
PA TECHNOLOGY
Herts, 76-3-61222

FRANCE
CETIA
Toulon Cedex, 9-42-12005

SOREP
Chateaubourg, 99-623955

NORWAY
NORKRETS AS
Oslo, 47-2360677/8

SWEDEN
NORDISK ARRAYTEKNIK AB
Solna, 8-734 99 35

VLSI SALES REPRESENTATIVES

CALIFORNIA
CENTAUR CORP.
Irvine
714-261-2123

CENTAUR CORP.
Calabasas
818-704-1655

CENTAUR CORP.
San Diego
619-278-4950

EMERGING TECHNOLOGY
San Jose
408-433-9366

EMERGING TECHNOLOGY
Orangevale
916-988-4387

COLORADO
LUSCOMBE ENGINEERING
Longmont
303-772-3342

IOWA
SELTEC SALES
Cedar Rapids
319-364-7660

MARYLAND
DELTA III
Columbia
301-730-4700

MISSOURI
CENTECH, INC.
Raytown
816-358-8100

CENTECH, INC.
Bridgeton
314-291-4230

NEW YORK
bbd ELECTRONICS
Rochester
716-425-4101

OREGON
MICRO SALES
Beaverton
503-645-2841

UTAH
LUSCOMBE ENGINEERING
Salt Lake City
601-565-9885

WASHINGTON
MICRO SALES
Bellevue
206-451-0568

CANADA
bbd ELECTRONICS
Mississauga, Ontario
416-821-7800

bbd ELECTRONICS
Ottawa, Ontario
613-729-0023

bbd ELECTRONICS
Pointe Claire, Quebec
514-697-0804

ISRAEL
RDT ELECTRONICS
Tel Aviv
3-483211-9

SINGAPORE
DYNAMIC SYSTEMS PTE, LTD
Singapore
011-65-742-1986

VLSI DISTRIBUTORS

United States represented by **SCHWEBER ELECTRONICS** except where noted.

ALABAMA
Huntsville, 205-895-0480

ARIZONA
Phoenix, 602-997-4874

CALIFORNIA
Canoga Park, 818-999-4702
Gardena, 213-320-8090
Irvine, 714-863-0200
Sacramento, 916-929-9732
San Diego, 619-450-0454
San Jose, 408-432-7171

COLORADO
Englewood, 303-799-0258

CONNECTICUT
Danbury, 203-748-7080

FLORIDA
Altamonte Springs, 305-331-7555
Pompano Beach, 305-977-7511

GEORGIA
Norcross, 404-449-4600

ILLINOIS
Elk Grove Village, 312-364-3750

IOWA
Cedar Rapids, 319-373-1417

KANSAS
Overland Park, 913-492-2922

MARYLAND
Gaithersburg, 301-840-5900

MASSACHUSETTS
Bedford, 617-275-5100

MICHIGAN
Livonia, 313-525-8100

MINNESOTA
Edina, 612-941-5280

MISSOURI
Earth City, 314-739-0526

NEW HAMPSHIRE
Manchester, 603-625-2250

NEW JERSEY
Fairfield, 201-227-7880

NEW YORK
Rochester, 716-424-2222
Westbury, 516-334-7474

NORTH CAROLINA
Raleigh, 919-876-0000

OHIO
Beachwood, 216-464-2970
Dayton, 513-439-1800

OKLAHOMA
Tulsa, 918-622-8003

OREGON
ALMAC ELECTRONICS CORP.
Beaverton, 503-629-8090

PENNSYLVANIA
Horsham 215-441-0600
Pittsburgh, 412-782-1600

TEXAS
Austin, 512-458-8253
Dallas, 214-661-5010
Houston, 713-784-3600

WASHINGTON
ALMAC ELECTRONICS CORP.
Bellevue, 206-643-9992
Spokane, 509-924-9500

WISCONSIN
New Berlin, 414-784-9020

AUSTRALIA
ENERGY CONTROL
Brisbane, 61-7-376-2955

AUSTRIA
TRANSISTOR GmbH
Vienna, 222-8294010

BELGIUM AND LUXEMBURG
MCAtronix
Angleur, 41-674208

DENMARK
INTERELKO
Karlslunde, 3-140700

EIRE AND U.K.
HAWKE COMPONENTS
Sunbury-on-Thames, 1-9797799

QUARNDON ELECTRONICS
Derby, 332-32651

FINLAND
OY COMDAX
Helsinki, 0-670277

FRANCE
ASAP s.a.
Montigny-le-Bretonneux, 1-3043.82.33

GERMANY
DATA MODUL GmbH
Munich, 89-560170

BIT-ELECTRONIC AG
Munich, 89-4180070

SPEZIAL-ELECTRONIC KG
Bueckeburg, 5722-2030

HONG KONG
LESTINA INTERNATIONAL, LTD.
Tsimshatsui, 852-3-7231736

ITALY
INTER-REP S.P.A.
Torino, 11-2165901

JAPAN
ASAHI GLASS CO. LTD.
Tokyo, 81-3-218-5854

TEKSEL COMPANY, LTD.
Tokyo, 81-3-461-5311

TOKYO ELECTRON, LTD.
Tokyo, 81-423-33-8009

KOREA
ANAM VLSI DESIGN CENTER
Seoul, 82-2-553-2997

EASTERN ELECTRONICS
Seoul, 82-2-464-0399

NETHERLANDS
DIODE
Houten, 3403-91234

SWEDEN AND NORWAY
TRACO AB
Farsta, 8-930000

SOUTH AMERICA - BRAZIL
INTERNATIONAL TRADE DEVELOPMENT
Palo Alto, 415-856-6686

SPAIN AND PORTUGAL
SEMICONDUCTORES s.a.
Barcelona, 3-217 23 40

SWITZERLAND
FABRIMEX AG
Zürich, 1-2 5129 29

TAIWAN
PRINCETON TECH CORP.
Taipei, 886-2-717-1439

01/89

VLSI TECHNOLOGY, INC.

SALES OFFICES, DESIGN CENTERS, AND DISTRIBUTORS